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A 289-301 GHz amplifier with 18-dB gain in 28-nm CMOS

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Abstract: Traditional terahertz amplifiers are highly dependent on compound semiconductor processes such as InP, which suffer from high costs and limited integration ability. In contrast, CMOS processes offer advantages in low cost and high integration. However, they face multiple challenges in the terahertz band, resulting in a scarcity of reported high-performance CMOS terahertz amplifiers. To break through the bottleneck of terahertz chip design in CMOS processes, this paper proposes a terahertz amplifier architecture based on the periodic stabilization technique. This technique enhances the gain at high frequencies while moving the input impedance of each stage into the stable region of the preceding stage at lower frequencies. It also absorbs unavoidable conductor losses into the stabilization network, effectively boosting the overall system gain performance and guaranteeing the overall stability. Multiple amplifier variants were fabricated in a 28-nm CMOS process. AMP1 achieves a peak gain of 18 dB at 300 GHz with a 3-dB gain bandwidth of 289 - 301 GHz. To the authors' knowledge, this is the first reported amplifier implemented in a 28-nm bulk CMOS process operating at 300 GHz, demonstrating a competitive operating frequency.

Key words: Amplifier, CMOS, Gain-boosting, mm-Wave, Terahertz.
PACS:

Introduction

With the rapid evolution toward sixth generation (6G) wireless systems, the terahertz (THz) band (0. 1 - 10 THz) has emerged as a crucial frontier. The massive bandwidth available in this spectrum is indispensable for accommodating future applications such as ultra-high-speed terabit-per-second (Tbps) communications, high-resolution imaging, and integrated sensing [1-6]. However, overcoming the severe free-space path loss at these frequencies heavily relies on high-performance solid-state front ends. In the RF front-end, the power amplifier (PA) and low-noise amplifier (LNA) serve as the primary bottlenecks for system efficiency, communication range, and signal-to-noise ratio [3,7].

For years, terahertz amplifiers have primarily relied on advanced processes such as InP and GaN. While these technologies offer superior high-frequency capabilities and high output power, their inherent incompatibility with dense digital baseband circuits, coupled with exorbitant manufacturing costs, significantly hinders their potential for commercialization. Consequently, extensive research has shifted toward low-cost, highly integrated silicon-based solutions. Early silicon-based designs were severely constrained by the maximum oscillation frequency (f_{max}). A significant breakthrough occurred with the introduction of the high performance SiGe process [8], sparking a proliferation of high-performance THz SiGe chips. For example, a 200-255 GHz PA was reported [9] and the Doherty architecture was also successfully introduced to the THz band for the first time with high back-off efficiency [10]. With the latest SiGe process, recent works have demonstrated PAs [11] and LNAs [12] operating well beyond 300 GHz, exhibiting the tremendous potential of silicon at THz frequencies. Compared to SiGe, standard bulk CMOS processes offer unparalleled integration capabilities and much lower cost. Thus, extensive research has focused on developing low-cost CMOS-based THz amplifiers [13], [14], [15], [16], [17], [18] in recent years.

However, the limited f_{max} of CMOS transistors poses a major challenge in designing CMOS amplifiers over 200 GHz. The theoretical foundation for overcoming this gain limitation dates back to the 1950s, when S. Mason proposed the maximum unilateral gain (U) [19]:

$$U = \frac{\left|Y_{21} - Y_{12}\right|^2}{4\left[Re(Y_{11})Re(Y_{22}) - Re(Y_{12})Re(Y_{21})\right]}. \quad (1)$$

Subsequently, A. Singhakowinta and A. Boothroyd derived the maximum available gain (G_{MAX}) in 1964 by

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embedding the transistor in a passive, lossless, reciprocal network [20]:

$$G_{max} = 2U - 1 + 2\sqrt{U(U-1)}. \quad (2)$$

In 2013, based on the above gain-boosting theories, the operating frequency of CMOS amplifiers was first pushed to 260 GHz by embedding the transistor in a four-port passive, lossless, and reciprocal feedback network [21]. Over the subsequent decade, numerous studies focused on enhancing gain and bandwidth [13], [14], [15], [16], [17]. Despite these pioneering efforts, contemporary high-frequency CMOS amplifiers still face significant challenges. To guarantee stability, the conventional G_{MAX} approach rigidly enforces a stability factor (K_f) equal to 1. This enforcement inevitably results in a high quality-factor, which strictly limits the fractional operating bandwidth and introduces substantial insertion loss in the matching networks. Furthermore, most existing wideband designs still only cover a few tens of GHz, failing to fully exploit the ultra-wideband advantages of the THz spectrum. The conventional approach also focuses solely on the amplifier core, neglecting the loading effects of adjacent stages, and requires precise tuning that is highly sensitive to inaccurate transistor models at THz frequencies.

To address these challenges, this paper demonstrates a periodic stabilization technique that can reduce the stability factor in some frequency band of single stage amplifier core to below 1. Moreover, the bandwidth degradation associated with the conventional trade-off between gain and stability can also be relaxed. A 300 GHz prototype THz amplifier is demonstrated using a 28-nm bulk CMOS process. Four additional design variants with tuned parameters were included on the same die to assess sensitivity to model uncertainty.

Circuit Implementation

The architecture of the proposed periodically stabilized amplifier is shown in Figure 1, featuring a 12-stage periodically stabilized gain-boosting (PSGB) amplification core. A compact transformer balun at the input and a Marchand balun at the output provide broadband single-ended-to-differential conversion and matching. A low-impedance and ground-shielded bias feedline with shielding ground below M7 is used for bypassing in the feeding network.

Figure 2 shows the schematic of the single stage amplifier. Each stage employs four parallel asymmetric ULVT transistors [22], each with eight 0.4-μm fingers, to enhance the output power while providing reasonable interstage impedance for broadband matching. To boost the MSG, two 7.43 fF cross-coupled over-neutralization capacitors [22] are used for the amplifier core. Multiple matching branches ($TL_{d,diff}$, $TL_{g,diff}$, C_g, and L_d) are used for feeding and achieving broadband matching. To mitigate the impact of shunt inductor L_d, two distinct sizes (6.3 pH for AMP1 and 8 pH for AMP2) are designed for different amplifiers.

Figure 3(a) shows the simulated maximum stable gain (MSG) and stability factor K_f of the two amplifier cores. To maximize the gain at 300 GHz to about 1 dB per stage, the value of the cross-coupled over-neutralization capacitors should be large enough, but it will also reduce the stability factor for lower frequencies.

To guarantee the overall stability of the amplifier, a mismatching technique to move the load impedance to the stable region can be used when K<1. According to the basic two-port network theory, for a conditional stable linear two-port network, the center and radius of the stable circle are defined as:

$$C_L = \frac{(S_{22} - \Delta S_{11}^*)^*}{|S_{22}|^2 - |\Delta|^2},\ R_L = \left|\frac{S_{12}S_{21}}{|S_{22}|^2 - |\Delta|^2}\right|. \quad (3)$$

When the load impedance lies outside the unstable region, the input of the network remains stable. Moreover, after considering the loss of the matching network and the multi-stage periodic cascading, the overall stability can be further improved using the mismatching technique.

Figure 3(b) shows the simulated matching trajectory of the matching network from 200 GHz to 300 GHz. The unstable region at 250 GHz is also illustrated in the grey region. To maximize the gain at high frequency band, conjugate matching is employed around 300 GHz. Moreover, from 210 to 280 GHz, the load impedance is deliberately kept away from the unstable region to im-

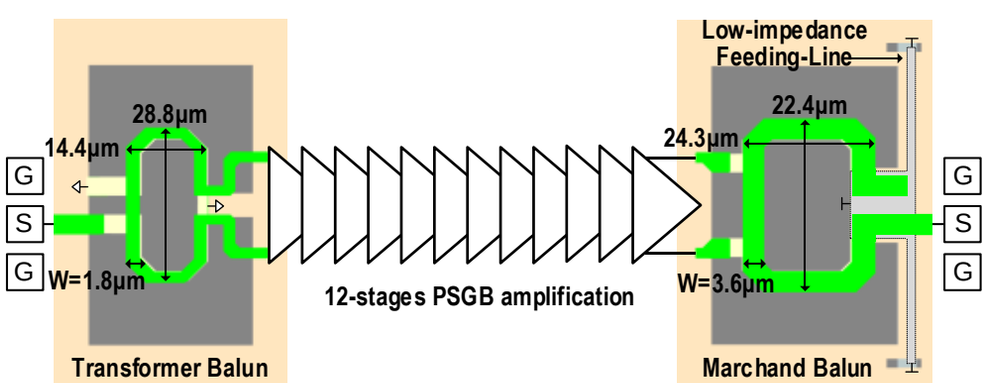
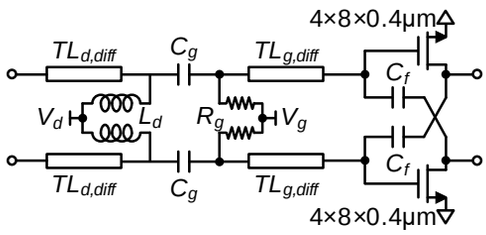


Fig. 1 Architecture of the THz amplifier
图1 太赫兹放大器芯片架构图



C_f	C_g	R_g	L_d	$Z_{TLd,diff}$	$\theta_{TLd,diff}$	$Z_{TLg,diff}$	$\theta_{TLg,diff}$
7.43 fF	184 fF	43 kΩ	6.3 pH (AMP1) 8 pH (AMP2)	66 Ω	28°@300G	66 Ω	16°@300G

Fig. 2 Schematic of a single stage amplifier.
图2 太赫兹放大器单级原理图

prove the stability after cascading.

The 3D layout of the single-stage amplifier core is depicted in **Figure 4**. The parallel transistor fingers are placed within a compact shared guard-ring layout to reduce parasitic capacitance and area as shown in the top right of **Figure 4**. Compared with the default interconnect configuration of the 28-nm CMOS PDK transistor cell, the customized layout routes the drain directly to the upper M7 layer and brings the source terminals out through M2 and M3 on both sides, reducing the gain degradation caused by parasitic parameters.

Measurement Results

The chip photograph is shown in Figure 5. The width of a single THz amplifier is only 0.1 mm, and its length is less than 1 mm. Due to the sensitivity of THz amplifiers to model parameters, in addition to the two amplifiers mentioned in this article, four redundant amplifiers were also designed with tuned parameters.

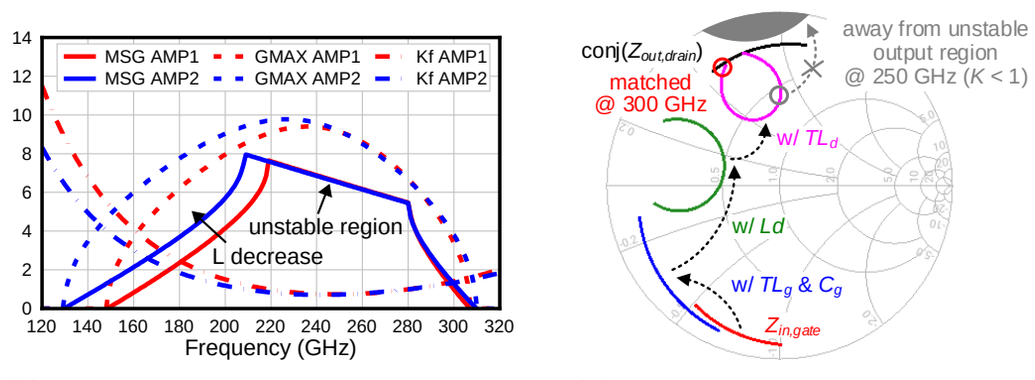
The measured S-parameters are shown in Figure 6. The gate and drain biases are 0.6 V and 1 V, respectively, to maximize f_{max}. The power consumption is 95 mW for each amplifier.

The S-parameters were measured using a Keysight N5245A PNA-X vector network analyzer in conjunction with OML V03VNA2 frequency-extension modules operating from 220 to 325 GHz. On-wafer measurements were performed using microwave probes. Prior to measurement, a SOLT (short-open-load-thru) calibration was carried out using a calibration substrate, with the measurement reference planes established at the probe tips to remove the effects of the external measurement setup and accurately characterize the chip performance.

The AMP1 achieves a peak gain of 18 dB at 300 GHz as shown in Figure 6(a). The 3-dB gain bandwidth spans 289-301 GHz. The gains are lower around 260 GHz because the proposed stabilization technique introduces impedance mismatch at this frequency range. By using a larger shunt inductor, the AMP2 achieves a peak gain of 18 dB at 300 GHz, and its 3-dB gain bandwidth spans 290-300 GHz, as shown in Figure 6(b).

Figure 7(a) shows the measured stability factor. Although the isolated gain-boosting stage is intentionally designed with $K_f < 1$ over part of the band, no free-running oscillation was observed during the small-signal and large-signal measurements at the nominal bias condition. Figure 7(b) shows the measured saturation power (P_{sat}). AMP1 achieves about -4 dBm at 250 GHz and -15 dBm at 300 GHz, while AMP2 achieves about -5 dBm at 250 GHz and -14 dBm at 300 GHz.

Table I shows the comparison with the reported THz amplifiers in CMOS process. To the authors' knowl-



(a) (b)

Fig. 3 Simulated performance of single stage: (a) gain and stability; (b) matching trajectory
图3 太赫兹放大器单级特性仿真结果:(a)增益与稳定性系数;(b)阻抗匹配轨迹

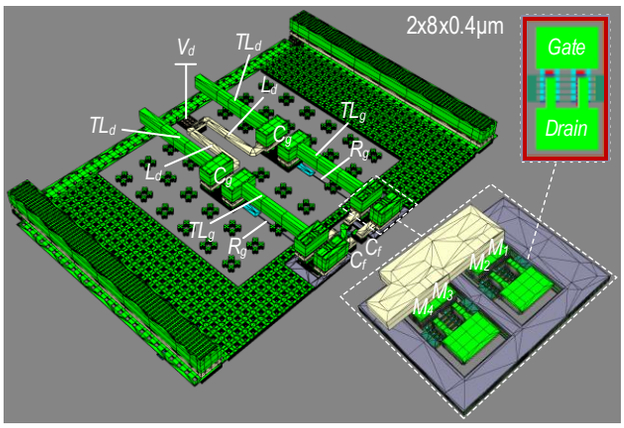


Fig. 4 3D layout of a single stage amplifier.
图4 太赫兹放大器单级版图

edge, this work represents the first reported 28-nm CMOS amplifier operating at 300 GHz. With the increasing demand for the high-integration RF systems in the future, the deep sub-micron technology represented by 28nm CMOS can provide more powerful baseband signal processing capabilities and higher integration density. Therefore, this work demonstrates the potential of integrating high-performance terahertz systems into high-performance deep sub-micron SOCs.

Conclusions

In this paper, a novel periodic stabilization gain-boosting technique is proposed to address the fundamental gain and bandwidth limitations of standard bulk CMOS processes operating near f_{max}. By intentionally relaxing the single-stage stability constraint ($K_f < 1$) at specific frequency band and fully accounting for the loading effects of adjacent stages, the severe limitation on gain and bandwidth of the conventional G_{MAX} approach is effectively mitigated. To validate the concept, multiple prototype THz amplifiers have been designed. The AMP1 achieves a 3-dB gain bandwidth of 289 – 301 GHz and a peak gain of over 18 dB at 300 GHz. The proposed amplifiers offer a highly integrated, cost-effective solution for emerging applications, such as THz radars and 6G integrated sensing and communication (ISAC) systems.

Table 1 Comparison With Recently Reported CMOS THz Amplifiers
表1 与已报导的基于CMOS工艺的太赫兹放大器的性能对比

	This Work (AMP1)	This Work (AMP2)	[13]	[14]	[15]	[16]	[17]	[18]
Technology	28-nm bulk CMOS		65-nm CMOS					
Topology	12-stage Common-Source (CS)		10-CS	3-CS	6-CS	2-CS	16-CS	10-CS
Frequency (GHz)	289-301	290-300	225-264	294-310	245	272	273-301	302.5
Gain (dB)	18 @300GHz	18 @300GHz	12±2.9	≈3	28	15	21	30.9
BW_{3dB} (GHz)	12 @300GHz	10 @300GHz	N.A.	16	N.A.	3.7	N.A.	N.A.
P_{sat} (dBm)	-15 @300GHz	-14 @300GHz	-1.9	N.A.	9.2	-2.36	N.A.	-5.3
PDC (mW)	95	95	36.4	N.A.	217	21.5	35.4	35.4
Core Area (mm^2)	0.1 (single channel w/o DC pad)	0.1 (single channel w/o DC pad)	0.37	N.A.	0.48	0.28	≈0.3	0.15

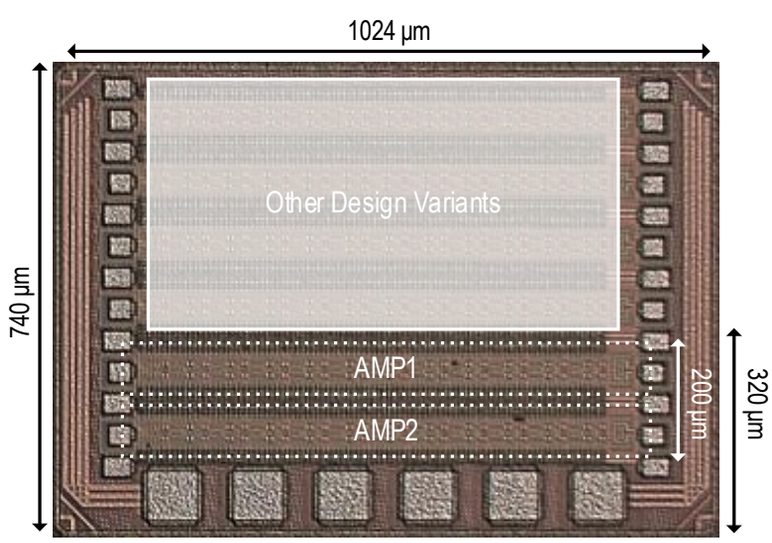
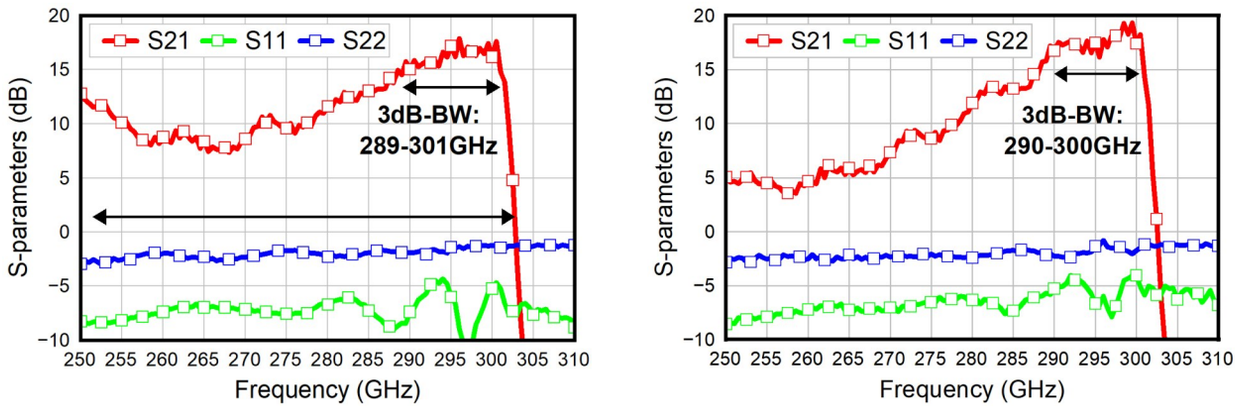
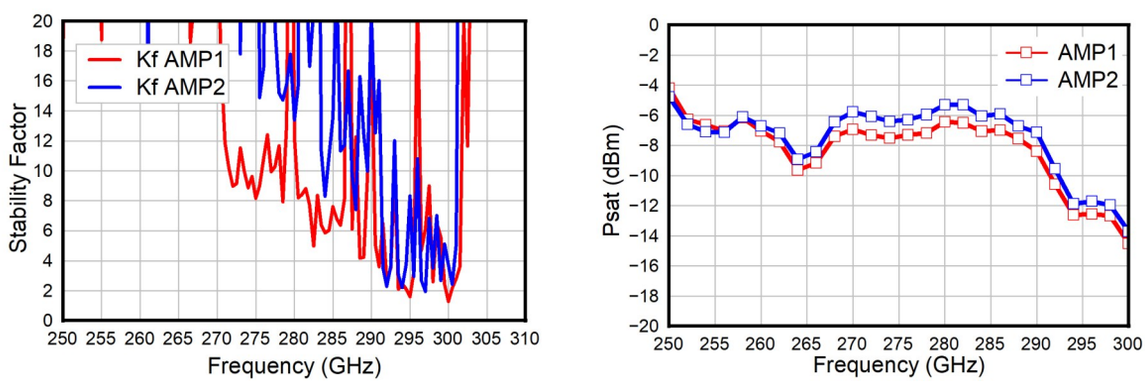


Fig. 5 Chip photograph of the proposed amplifier
图5 太赫兹放大器芯片照片



(a) (b)

Fig. 6 Measured S-parameters of the amplifiers: (a) amplifier 1; (b) amplifier 2
图6 太赫兹放大器芯片S参数测试结果:(a)太赫兹放大器1;(b)太赫兹放大器2



(a) (b)

Fig. 7 Measured stability and output power performance: (a) stability factor; (b) saturated output power
图7 太赫兹放大器芯片稳定性与输出功率测试结果:(a)稳定性因子测试结果;(b)饱和输出功率测试结果

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基于28nm CMOS工艺的18-dB增益289-301 GHz太赫兹放大器

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摘要：传统太赫兹放大器高度依赖于磷化铟(InP)等化合物半导体工艺，面临高昂成本且难以与大规模数字电路集成。相比之下，硅基CMOS工艺具备低成本和高集成度优势，但在太赫兹频段却面临着晶体管固有增益低、高频寄生效应严重以及无源网络损耗巨大等多重挑战，导致目前鲜有高性能CMOS太赫兹放大器报道。为突破CMOS工艺下的太赫兹芯片设计瓶颈，本文创新提出一种基于周期性稳定化技术的太赫兹放大器芯片架构，通过将各级输入阻抗匹配到前级网络的稳定负载区域有效实现了电路的级联稳定性，同时将不可避免的导体损耗吸收至稳定网络内部，在保障增益的同时，进一步提升了电路稳定性。基于该创新架构，本文基于28-nm CMOS工艺，成功研制多款硅基太赫兹放大器芯片。第一款芯片在300 GHz频点仍能保持18 dB增益，并实现了289-301 GHz的3dB工作频带。据作者所知，这是目前已报道的首个采用28-nm bulk CMOS工艺实现的工作频率达到300 GHz的太赫兹放大器，为实现低成本、高集成太赫兹系统提供了器件支撑。

关 键 词：放大器；互补金属氧化物半导体；增益增强；毫米波；太赫兹

中图分类号：TN454 **文献标识码**：A