

Design of readout circuit for pyroelectric infrared detectors based on dual-CTIA structure

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Abstract: To achieve the detection of extremely weak signals from pyroelectric infrared detectors and to meet the demands of high-sensitivity applications, this paper proposes a dual-capacitor transimpedance amplifier (CTIA) readout structure featuring a variable array size. Additionally, a bandgap reference and a low dropout regulator (LDO) are designed as the bias circuit to provide voltage bias, in order to meet the requirements of low noise, low power consumption, large dynamic range and portability. The circuit is designed in TSMC 0.18 μm 1P6M CMOS process under a 3.3V supply. For the layout implementation, advanced techniques, including dummy structures and guard rings, are employed to improve device matching, overall layout symmetry, as well as the noise immunity and electrical stability of the analog circuitry.

Key words: pyroelectric, readout circuit, dual-CTIA, variable array size, bias circuit

Introduction

Any object with a temperature above absolute zero will emit infrared radiation. The core function of infrared detectors is to capture and analyze the infrared radiation emitted by objects to achieve the purposes of detection and identification. According to the electromagnetic spectrum, infrared rays cover a wide range from visible light to microwaves. Based on the distribution of wavelengths, infrared rays can be divided into short-wave, medium-wave, long-wave, and far-infrared bands. Different infrared bands have different functions in specific applications. Currently, infrared detection technology has been widely applied in several cutting-edge fields, such as in the field of space remote sensing. Infrared remote sensing can penetrate the atmosphere to conduct surveys of the Earth, detect forest fires, and make weather forecasts; The initial major development of infrared technology was driven by the need for night combat dur-

ing the First and Second World Wars, so infrared technology is more widely used in the military field, such as for precise guidance, night vision reconnaissance, and target detection; In the field of spectral analysis, infrared spectrometers can perform non-destructive detection by using the absorption characteristics of substances to specific wavelengths of infrared. For example, a handheld infrared spectrometer can be used to quickly measure the sugar content of fruits. Infrared technology, with its unique thermal sensing ability, plays an indispensable and important role in research, military, and industrial production^[1-3].

As a type of uncooled infrared detector, pyroelectric infrared detectors operate at room temperature and do not require additional cooling systems. Pyroelectric infrared detectors have a wide spectral response range and are relatively low in cost. These characteristics give them a strong competitive edge in the field of infrared detectors.

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The principle of pyroelectric infrared detectors is based on the pyroelectric effect of the device, which means that when the temperature changes, the intensity of spontaneous polarization within the material also changes. This effect will cause a redistribution of charges on the device's surface, which will generate a voltage or charge, as illustrated in Fig. 1. The response of the pyroelectric detector is proportional to the rate of temperature change (dT/dt), rather than the absolute temperature itself. Therefore, in practical applications, pyroelectric infrared detectors must be used in conjunction with an optical chopper. The chopper modulates the continuous incoming infrared radiation into an alternating (AC) signal, which is necessary for effective detection^[4-5].

Pyroelectric infrared devices can be electrically equivalent to a parallel capacitor structure. And this structure leads to an extremely high output impedance, typically in the gigaohm ($G\Omega$) range^[6]. At the same time, the pyroelectric effect generates only a very small current, usually on the order of fA-pA. As a result, pyroelectric infrared detection faces two major practical challenges: the first one is extremely low signal amplitude and the other is very high equivalent output resistance. These issues severely compromise signal integrity and represent the fundamental problems that must be addressed by the readout circuit.

Common readout architectures such as the source follower per detector (SFD), resistive transimpedance amplifier (RTIA), CTIA, and charge sensitive amplifier (CSA) have been widely used^[6-9]. However, each exhibits certain limitations when applied to pyroelectric infrared detectors. Therefore, the design of a readout circuit capable of efficiently extracting weak pyroelectric signals while maintaining a high signal-to-noise ratio is both scientifically meaningful and practically valuable. In this paper, we have completed the following work:

1. Fabricated a linear array device using a $28\mu\text{m}$

thick Polyvinylidene Fluoride (PVDF) film and tested its pyroelectric performance.

2. Innovatively proposed a dual-CTIA circuit structure for the pyroelectric infrared detector readout circuit.

3. A multi-mode architecture is adopted to implement switching between different array scales.

4. Designed an on-chip bias circuit to realize the miniaturization and portability of the detector.

5. Employed process corner simulations and Monte Carlo simulations to ensure circuit robustness and completed the circuit layout.

1 Pyroelectric device equivalent model

Linear array devices with a parallel capacitor structure were fabricated using a $28\mu\text{m}$ thick PVDF film. The dimensions of the devices are $50\mu\text{m}$, $100\mu\text{m}$, $150\mu\text{m}$ and $200\mu\text{m}$, respectively. The top electrode uses gold (Au), and the bottom electrode uses nichrome (NiCr) alloy. These devices are used to test pyroelectric performance. Figure 2 below shows the photolithography mask pattern and the fabricated PVDF devices.

The PVDF device is electrically equivalent to a capacitor, a resistor, and a current source connected in parallel. Based on previous calculations, test results of the PVDF device, and literature reports, the values of the equivalent resistance and capacitance are $180 G\Omega$ and 90 fF , respectively, while the value of the current source corresponds to the pyroelectric current^[6,10-11]. The current source in the circuit represents the pyroelectric current generated by the device due to temperature variations, and its magnitude can be expressed as:

$$i_d = A_d \cdot \frac{dP_s}{dT} \cdot \frac{dT}{dt} = A_d \gamma \frac{dT}{dt}, \quad (1)$$

Among them, P_s is the polarization vector of the pyroelectric material, γ is the pyroelectric coefficient, and A_d is the device area of the pyroelectric infrared detector. This study adopts a dynamic measurement method to de-

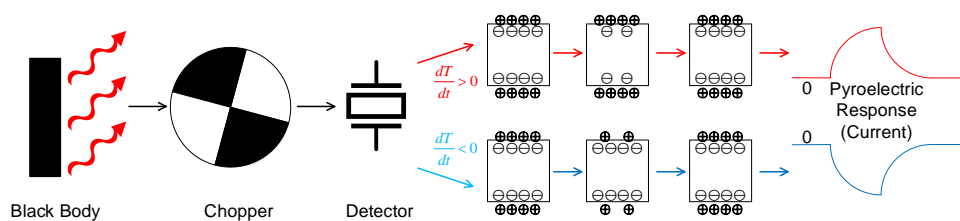


Fig. 1 Schematic diagram of the pyroelectric effect.

图1 热释电效应示意图

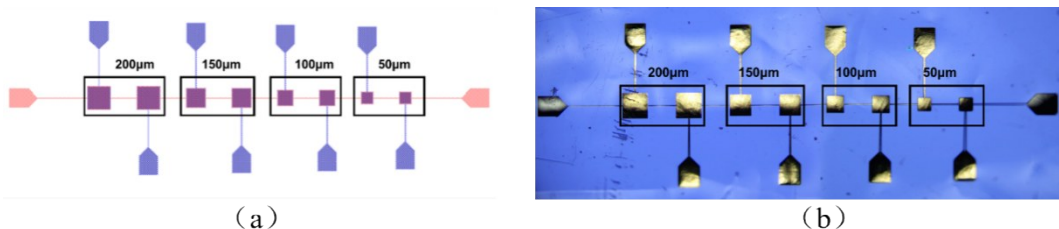


Fig. 2 (a) Photolithographic mask pattern (b) Fabricated PVDF device (top electrode).

图2 (a)光学掩膜版图形 (b)PVDF实物器件(顶电极)

termine the pyroelectric coefficient, with results obtained using a pyroelectric coefficient tester. The principle involves applying a periodic temperature oscillation to the sample via a thermistor, thereby generating a pyroelectric current. The formula for calculating the pyroelectric coefficient can be expressed as follows:

$$\gamma = \frac{dP_s}{A_d \cdot dT} = \frac{1}{A_d} \frac{dP_s}{dt} \frac{dt}{dT} = \frac{i_d(\omega)}{j\omega A_d \cdot T(\omega)} = \frac{\alpha}{j\omega A_d} \frac{i_d(\omega)}{R(\omega)} \quad (2)$$

Here, ω is the test frequency, i_d is the measured current curve, $R(\omega)$ is the measured platinum resistance curve, and $\alpha=0.390 \Omega/K$ is the temperature coefficient of the platinum resistor. Figure 3 shows the test results for the pyroelectric coefficient of the PVDF device, in Fig. 3, (a) shows the curve of thermistor resistance versus temperature, and (b) shows the pyroelectric current variation curve. The temperature period is 20 s, the peak-to-peak value of the temperature resistance is 0.660Ω , the peak-to-peak current is 0.8 pA , and the sample area is $60 \mu\text{m} \times 60 \mu\text{m}$. The pyroelectric coefficient can then be calculated using Equation (2). By taking only the component at the frequency ω , the PVDF pyroelectric coefficient is determined to be $39 \mu\text{C}/(\text{m}^2 \cdot \text{K})$. Therefore, taking the $50 \mu\text{m} \times 50 \mu\text{m}$ PVDF device as an example, the pyroelectric current is $39 \frac{\mu\text{C}}{\text{m}^2 \cdot \text{K}} \cdot 2.5 \times 10^{-9} \cdot \text{m}^2 \cdot \frac{dT}{dt}$ which is on the order of fA-pA. For convenience of calculation in the circuit simulation, and to highlight the circuit's processing capability, the pyroelectric current is set to a value of 1 fA. .

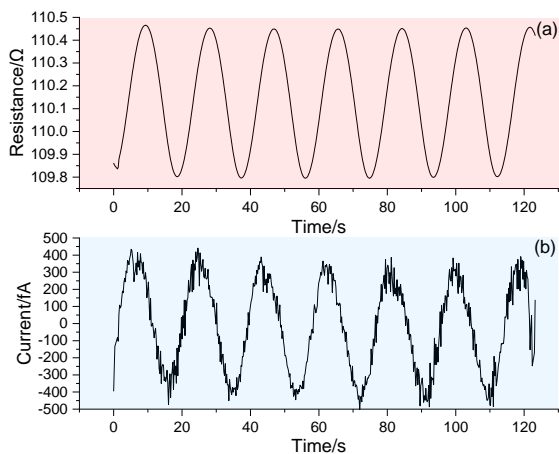


Fig. 3 Pyroelectric Coefficient Measurement Results. (a) Resistance variation with time (b) Current variation with time.
图3 热释电系数测试结果(a)电阻值随时间变化曲线 (b)热释电电流随时间变化曲线

2 Circuit design and simulation results

In the circuit design of this paper, an innovative dual-CTIA structure readout circuit is proposed, adopting a multi-modal architecture design. A Bandgap Reference voltage source and a LDO circuit were also designed. Furthermore, the design includes row and column control

circuits for pixel readout and column-level buffers at the output. Figure 4 shows the overall architecture of the designed chip. The reference voltage V_{ref} and reference current I_{ref} generated by the Bandgap circuit provide the core biasing for the entire chip system. Specifically, V_{ref} is input to the LDO to generate a high-precision and stable $V_{\text{in+}}$, which serves as the common-mode voltage for the non-inverting input of the CTIA operational amplifier. Meanwhile, I_{ref} is fed into the bias generation circuit to produce the bias voltages V_{g1} , V_{g2} required for the op-amp operation, as well as to provide the static bias current. The unit readout circuit utilizes a dual-CTIA structure with selection switches. After being integrated and amplified by the CTIA, the signal is input to the Correlated Double Sampling (CDS) circuit. It then passes through a buffer circuit composed of a source follower and is transmitted to the column buffer for sequential output under the control of timing signals. The row and column control circuit consists of an array of D flip-flops, governing the readout timing of the entire chip.

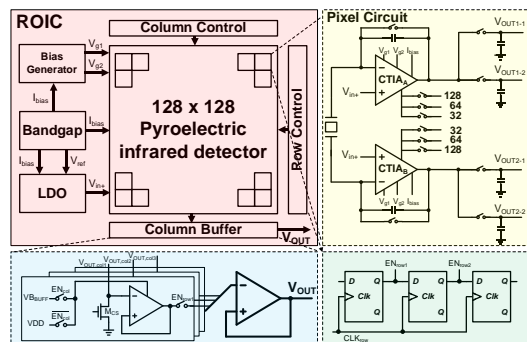


Fig. 4 Chip architecture block diagram. Including overall architecture, unit cell structure, column buffers, and row/column control circuits.

图4 芯片架构示意图,包括整体架构、单元电路、列缓冲器、行/列控制电路

2.1 Pixel-level dual-CTIA circuit

Due to the special properties of pyroelectric devices, common types of readout circuits have drawbacks in their application. For example, with schemes like the RTIA, CSA, and SFD, the equivalent resistance of the pyroelectric device is typically as high as tens of $\text{G}\Omega$. To achieve ideal signal readout on an integrated circuit chip, the circuit end would need to match an input impedance of the same magnitude. However, such a high-value resistor is extremely difficult to implement accurately in actual IC manufacturing. The CTIA is a widely used and mature circuit. However, when applied to pyroelectric infrared detectors, the DC leakage current generated by the device's high equivalent resistance is continuously accumulated by the integration capacitor. This causes the output signal to be dominated by DC noise, thereby overwhelming the weak AC valid signal. Therefore, during the design process of the pyroelectric infrared detector readout circuit, considering the DC noise introduced by the high-value equivalent resistance of the pyroelectric device itself, and incorporating the concept

of a differential circuit, a dual-CTIA structure readout circuit scheme was chosen for the unit cell design. Compared to structures like single-CTIA, SFD, and RTIA, this structure overcomes the drawback where those circuits cannot remove the DC current generated by the pyroelectric device's equivalent resistance. It effectively eliminates the influence of the DC current from the equivalent resistance, achieving a more precise and high-stability readout of the pyroelectric detector signal.

The dual-CTIA readout circuit structure consists of two independent CTIA circuits (denoted as CTIA-A and CTIA-B, respectively) within a single pixel to achieve amplification and subtraction processing of the signal. Specifically, the non-inverting inputs of both CTIA operational amplifiers are connected to a DC reference voltage (V_{in+}), while their inverting inputs are connected to the positive and negative terminals of the pyroelectric device, respectively.

The dual-CTIA circuit structure is shown in Figure 5. The signal output by the CTIA further passes through a CDS circuit, which eliminates reset noise and suppresses $1/f$ noise and offset. Subsequently, it goes through a source follower to complete the buffer output. Finally, a subtraction operation is performed on the signals from the CTIA-A and CTIA-B channels. This process effectively doubles the valid signal amplitude.

Assuming the output signal amplitude for a single-ended CTIA readout is S , and the Root Mean Square (RMS) average value of the noise is N , then the dual-CTIA differential readout signal, which is the difference between the two paths, is:

$$S_{diff} = S_1 - S_2 = S - (-S) = 2S, \quad (3)$$

The RMS noise of the differential output is the root mean square of the noise from the two paths:

$$N_{diff} = \sqrt{N_1^2 + N_2^2} = \sqrt{N^2 + N^2} = \sqrt{2}N, \quad (4)$$

The Signal-to-Noise Ratio (SNR) of the signal output by the dual-CTIA is:

$$SNR_{diff} = \frac{S_{diff}}{N_{diff}} = \frac{2S}{\sqrt{2}N} = \sqrt{2} SNR_{single}, \quad (5)$$

Therefore, the output signal value is increased to 2 times that of a single CTIA, while the noise only increases to $\sqrt{2}$ times that of a single channel's noise. This im-

proves the signal-to-noise ratio by a factor of $\sqrt{2}$, i. e., $20\log\sqrt{2} \approx 3\text{dB}$, enhancing the performance and reliability of the pyroelectric infrared detector readout circuit.

For the design of the CTIA, controlling noise becomes the top priority because the pyroelectric signal is extremely weak. The primary noise source in the CTIA is kT/C noise, which mainly originates from the reset operation of the feedback capacitor, C_{fb} . Secondly, since pyroelectric signals are typically in the low-frequency range where the op-amp's $1/f$ noise is dominant, CDS technology is employed at the output of the CTIA op-amp to suppress both kT/C noise and $1/f$ noise. Furthermore, thermal noise is introduced by the op-amp's input transistors and feedback elements. Consequently, the design requires selecting an appropriate op-amp architecture and feedback capacitor size to balance factors such as noise, power consumption, and bandwidth^[12]. In this design, the telescopic cascode amplifier was chosen as the op-amp structure. Benefiting from its extremely high gain, the virtual short node between the op-amp's inverting and non-inverting inputs is sufficiently stable. This ensures a small input offset, allows for complete charge transfer, and significantly enhances charge injection efficiency and linearity.

The telescopic cascode amplifier also features a high Gain-Bandwidth Product (GBW) and Slew Rate (SR). This enables the CTIA to have a fast response and quick settling times, preventing the response from being hindered by the op-amp's own speed limitation. And we chose PMOS transistors as the input stage to suppress low-frequency noise. Additionally, single-stage amplifier has only one dominant pole, with other poles at very high frequencies^[13]. This makes it easier to maintain the stability within CTIA's negative feedback loop and eliminates the need for complex frequency compensation network. The telescopic cascode amplifier also has a drawback: its output voltage swing is somewhat limited. But when applied to pyroelectric infrared detectors, the signals are relatively weak, so, the telescopic cascode amplifier is an excellent choice for use in the CTIA.

2.2 Multi-modal Design

Because we used two CTIA structures in the pixel,

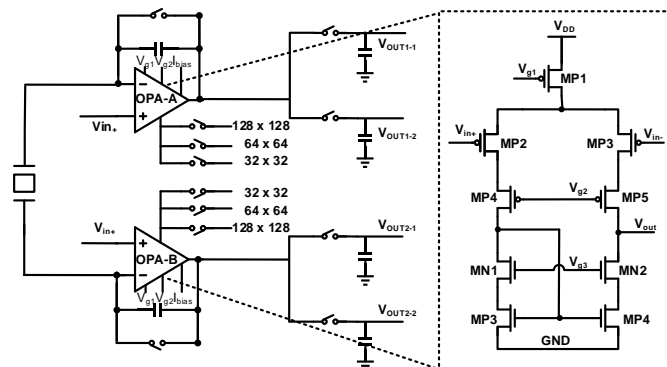


Fig. 5 Dual-CTIA Pixel Diagram and OPA Circuit Diagram.
图 5 双CTIA单元示意图及运算放大器电路结构

the power consumption of the chip is relatively high when operating in a large array mode. Therefore, we proposed a multi-modal readout circuit architecture based on 128×128 array scale. This architecture integrates a multi-modal static Region of Interest (ROI). By controlling switches via external digital logic, it can toggle between three different array scales: 128×128 , 64×64 , and 32×32 .

When the detector is not tracking a target, it can be set to standby mode, operating in the 32×32 low-power mode, actively shutting down or placing the analog circuits in non-working areas into a low-power standby state. When an anomaly is detected or high-precision recognition is required, it can switch to the full-frame mode. This design directly addresses the power consumption issue of large-scale arrays and provides the system with the flexibility to adapt to different task requirements.

At the same time, because the cost of tape-out is very high, a readout circuit that is compatible with different array scales is highly significant. This chip can be adapted to infrared detector arrays of different physical sizes. This significantly amortizes the design and tape-out costs for multiple product models during the device functional verification stage.

The circuit implementation is achieved through switches controlled by external signals. This multi-modal static ROI design, while ensuring maximum detection capability, offers a flexible and effective solution to the power consumption bottleneck in large-scale ROIC^[14-15].

2.3 Peripheral circuit design

Most of the current research and design solutions for pyroelectric infrared detector readout circuits still rely on external power sources to provide the bias voltage and bias current required by various modules. For example, in CTIA structure, the bias input of the operational amplifier is typically supplied by an external power source. This design approach leads to low overall circuit integration, making it difficult to meet the demands for miniaturization, portability, and ease of use.

To solve the problem that mentioned above, we conducted in-depth research and optimized design on the circuit bias. In the initial design, we attempted to use simple on-chip power sources and resistive divider networks to generate bias voltage and current, aiming to achieve stable power supply for each circuit module. However, because the op-amp's positive input (V_{in+}) is used as the

system's reference voltage, it demands high absolute precision. Consequently, the simple on-chip bias solution employed initially failed to achieve the desired precision and stability.

To overcome these shortcomings, we completely redesigned the overall on-chip bias structure, ultimately adopting a solution combining a Bandgap Reference and a LDO. The Bandgap voltage reference generates a precise temperature-compensated voltage by cleverly combining a voltage with a positive temperature coefficient (V_{PTAT}) and a voltage with a negative temperature coefficient (V_{CTAT}). Its output reference voltage can be expressed as:

$$V_{ref} = V_{BE} + K \cdot V_T, \quad (6)$$

generating a stable reference voltage of approximately 1.2 V and V_{ref} is largely independent of temperature and supply voltage.

The LDO circuit monitors the output voltage (V_{out}) via a resistive divider, compares it with the Bandgap's output reference voltage ($V_{ref} \approx 1.2$ V), and dynamically adjusts the gate voltage of the pass transistor. This process converts the fluctuating input voltage into a stable and low-noise DC output voltage, providing a stable power supply for the noise-sensitive modules in the readout circuit. At the same time, to satisfy the bias current requirements for the op-amps and LDO modules within the circuit, our design cleverly generates a current proportional to absolute temperature (I_{PTAT}) and a current inversely proportional to absolute temperature (I_{CTAT}) within the Bandgap module. These are suitably combined to produce a stable $2 \mu\text{A}$ bias current (I_{bias}) with a zero temperature coefficient^[16-19]. This approach effectively enhances the stability and integration of the entire chip. Figures 6 shows the on-chip bias circuit.

2.4 Circuit noise analysis

The primary noise sources in a pyroelectric infrared focal plane array system can be categorized into the intrinsic noise of the detector and the noise introduced by the readout circuit. To perform a noise analysis of the circuit, a noise equivalent model for a single CTIA is established, as shown in Fig. 7. In this model, I_{sig} represents the signal current of the pyroelectric device; C_{det} and R_{det} denote the equivalent capacitance and resistance of the detector, respectively; C_t is the integration capacitance; C_L is the equivalent output capacitance; g_m is the transconductance of the operational amplifier within the

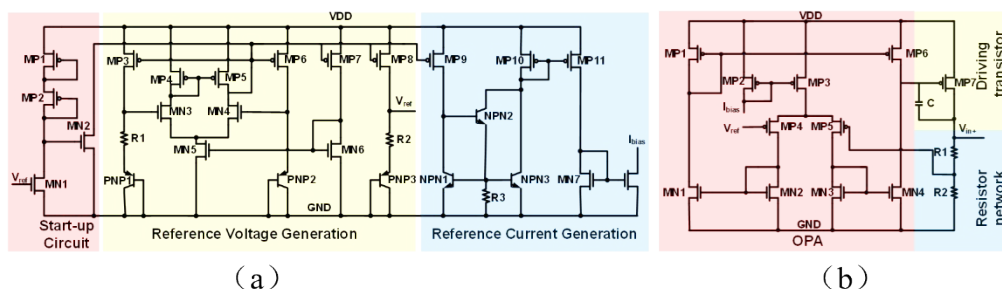


Fig. 6 Biasing circuit diagram: (a) bandgap circuit diagram. (b) LDO circuit diagram.

图6 偏置电路 (a)带隙基准 (b)低压差线性稳压源

CTIA; V_{node} corresponds to the virtual ground node of the operational amplifier; and the output current is represented by the controlled source $g_m V_{\text{node}}$ [20].

The model incorporates two lumped noise sources, representing the aggregate current and voltage noise, respectively. The total equivalent current noise is modeled as a current source connected in parallel with the input. It primarily consists of the thermal noise generated by the detector's equivalent resistance and the input bias current noise of the operational amplifier. Its power spectral density (PSD) can be expressed as:

$$\overline{i_{n,\text{total}}^2} = \frac{4kT}{R_{\text{det}}} + \overline{i_{n,\text{op}}^2}, \quad (7)$$

where k is the Boltzmann constant and T is the absolute temperature. Due to the extremely high equivalent resistance of pyroelectric detectors, this noise term often dominates in the low-frequency range.

The total equivalent voltage noise is modeled as a voltage source connected in series with the input of the operational amplifier. This represents the input-referred voltage noise of the operational amplifier, which primarily consists of the thermal noise and $1/f$ noise (flicker noise) of the MOS transistors. Its power spectral density can be expressed as:

$$\overline{v_{n,\text{total}}^2} = \frac{16kT}{3g_m} + \frac{K_f}{C_{ox}WLf}, \quad (8)$$

$I_{n,\text{total}}$ flows through the integration capacitor C_f . Assuming ideal integration, the transfer function to the output voltage noise is $1/sC_f$. $V_{n,\text{total}}$ is located within the feedback loop and is amplified by the operational amplifier's noise gain. Based on the principle of capacitive voltage division, this noise gain is approximately $1+C_{\text{det}}/C_f$. Therefore, by applying the principle of superposition and taking into account the finite bandwidth effects introduced by the transconductance g_m and the load capacitance C_L , the total output noise voltage spectral density of the circuit can be expressed as:

$$S_{v,\text{out}}(f) \approx \left[\frac{\overline{i_{n,\text{total}}^2}}{\omega^2 C_f^2} + \overline{v_{n,\text{total}}^2} \left(1 + \frac{C_{\text{det}}}{C_f} \right)^2 \right] \cdot |H_{\text{LPF}}(f)|^2, \quad (9)$$

Where $|H_{\text{LPF}}(f)|$ represents the low-pass transfer function determined by the transconductance g_m of the operational amplifier, the load capacitance C_L , and the feedback net-

work. It can be observed from the output noise spectral density formula that the voltage noise of the operational amplifier is amplified in the high-frequency range, with an amplification factor proportional to (C_{det}/C_f) .

This design adopts the CDS technique. CDS extracts the signal by subtracting two samples ($V_{\text{out}} = V_{\text{sig}} - V_{\text{rst}}$), thereby suppressing the noise. In the time domain, at the instant the reset switch turns off, the reset noise is sampled onto the integration node. During the integration process, the DC offset of this noise remains constant. Therefore, through the subtraction operation, CDS can eliminate the fixed kT/C reset noise and the DC offset voltage of the operational amplifier.

From a frequency-domain perspective, the CDS operation is equivalent to a high-pass filter. Given a time interval of T_{CDS} between the two samples, its power transfer function is:

$$|H_{\text{CDS}}(f)|^2 = 4 \sin^2(\pi f T_{\text{CDS}}), \quad (10)$$

It can be observed that at DC ($f=0$), the gain is zero, and the system exhibits significant attenuation characteristics in the low-frequency range. Consequently, CDS can effectively suppress low-frequency $1/f$ noise.

Fig. 8 illustrates the operating timing diagram of the readout circuit and the corresponding output results. Upon the completion of the reset phase, the signal VSH1 is activated to perform the first sampling, yielding VCDS1. Near the end of the integration period, VSH2 is activated to perform the second sampling, yielding VCDS2. The response voltage is then obtained by calculating VCDS2 - VCDS1. With the pyroelectric current set to zero, the comparative response results with and without CDS are presented in Fig. 9, demonstrating the efficacy of the CDS technique in noise reduction.

2.5 Circuit Stability Analysis

Stability is a critical aspect of closed-loop integrator circuit design. As the operational amplifier serves as the core component of the CTIA, its stability dictates the stability of the overall system. A significant advantage of the telescopic cascode amplifier employed in this design is that its frequency response is dominated by a single pole. This dominant pole is located at the high-impedance output node of the operational amplifier, and its frequency is determined by the total output resistance R_{out} and the total load capacitance C_L . It can be expressed as:

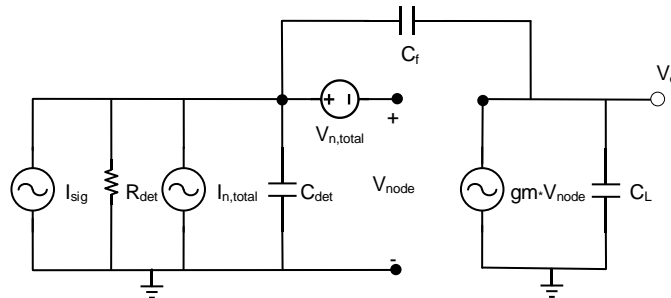


Fig. 7 Small-signal noise equivalent circuit model of a single channel (half-circuit). For the complete differential readout chain, the total noise power is the sum of the noise powers of the two uncorrelated channels.

图7 单通道(半边电路)的小信号噪声等效电路模型。对于完整的差分读出链路,总噪声功率为两个互不相关通道的噪声功率之和。

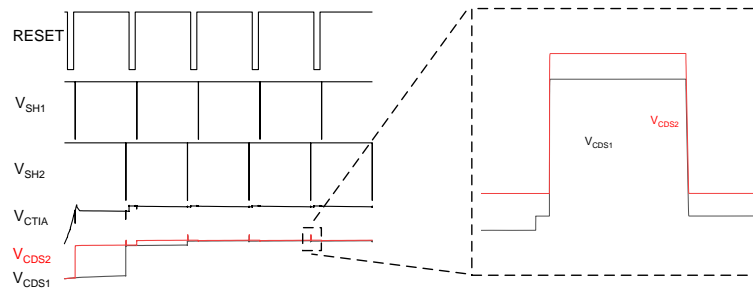


Fig. 8 Circuit Timing and CDS Operating Principle.
图 8 电路时序及 CDS 工作原理

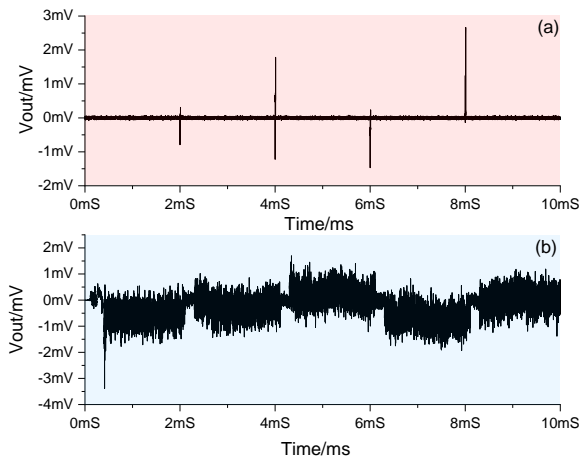


Fig. 9 Comparison of the noise reduction capability of Correlated Double Sampling.
图 9 相关双采样噪声去除能力对比

$$p_1 \approx \frac{1}{2\pi R_{out} C_L}, \quad (11)$$

The non-dominant poles are primarily associated with the source nodes of the cascode transistors (e. g., the source terminals of MP4 and MP5 in Fig. 5). Since the impedance at these nodes is approximately $1/g_m$ (which is relatively low), the frequencies of these non-dominant poles are significantly higher than the unity-gain bandwidth (GBW). In this design, the CTIA is loaded with a large CDS sampling capacitance, which inherently shifts the dominant pole to a lower frequency. This creates sufficient frequency separation between the dominant and non-dominant poles, effectively achieving load compensation.

Based on the Spectre stability (stb) simulation analysis. Simulation results indicate that under typical load capacitance, the operational amplifier achieves a Phase Margin (PM) of 50.13° , which exceeds 45° , and a Gain Margin (GM) of 18.24 dB, which is greater than 10 dB. For the CTIA, the phase margin is 56.46° and the gain margin is 30.16 dB. Consequently, the proposed amplifier architecture ensures excellent stability for the CTIA under closed-loop negative feedback operation, eliminating the risk of oscillation. Furthermore, the settling time satisfies the system timing requirements. Additionally, the Bandgap reference exhibits a phase margin of 67.12°

and a gain margin of 14.21 dB, while the LDO demonstrates a phase margin of 53° and a gain margin of 14.35 dB; thus, the stability of both circuits is guaranteed. In addition, Power Supply Rejection Ratio (PSRR) simulations were conducted, showing that the PSRR at the LDO output is better than -45.5 dB, and the Bandgap reference achieves a PSRR superior to -51 dB. This indicates that the circuit can effectively isolate the pixel bias points from supply voltage fluctuations. Regarding start-up characteristics, the designed LDO and reference circuits exhibit excellent dynamic response; all bias nodes reach steady state within $6 \mu\text{s}$ after the 3.3 V supply is established, with no observed sustained oscillations or start-up failures.

3 Test Result Analysis and Layout Design

The voltage output of a single CTIA circuit can be expressed by the following formula:

$$It = CV \rightarrow V = It/C, \quad (12)$$

The output voltage of the dual-CTIA architecture is twice that of a single CTIA circuit. Under the conditions of an integration time of 1.65mS, an integration capacitance of 100fF, and a pyroelectric current of 1fA, the theoretical output voltage is calculated to be $33 \mu\text{V}$. As demonstrated in Figure 10, the simulated output shows a mean value of $33.77 \mu\text{V}$, resulting in an error of approximately 2.3%, which indicates close agreement between simulation and theoretical analysis.

Since the circuit design and verification process in this study were completed based on Electronic Design Automation (EDA) simulation tools, a certain amount of process deviation between the simulation results and the actual tape-out test results is unavoidable. This study conducted an in-depth evaluation of the circuit's robustness using process corner simulations and Monte Carlo analysis methods to ensure the design's reliability and practicality in a real manufacturing environment.

Our circuit design was verified through simulations across all process corners. Furthermore, to quantify the impact of process mismatch, we conducted 1000 Monte Carlo simulations. Figure 11 and table I shows the Monte Carlo simulation results and the Q-Q plot. The mean value of the test results is $-33.75 \mu\text{V}$, which deviates from the theoretical value by approximately 2.3%. The stan-

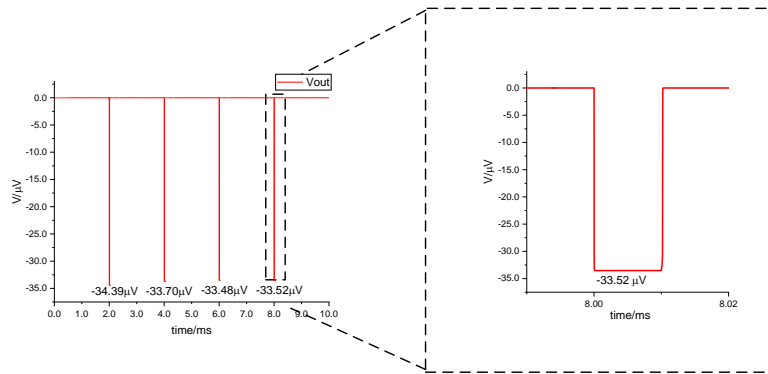


Fig. 10 Output Voltage Simulation Results.
图 10 输出电压仿真结果

dard deviation (σ) is $1.70 \mu\text{V}$. Standard deviation quantifies the dispersion and stability of the parameters. A smaller standard deviation indicates that the circuit has a better robustness against process variations. Under the assumption of the normal distribution, approximately 99.73% of the chips will have parameters falling within the $\mu \pm 3\sigma$ range, which is the core basis for evaluating yield.

The curve on the right is the Normal Q-Q Plot, which further examines the data's distribution characteristics. The data points are very tightly aligned around the diagonal dashed line, i. e., the theoretical normal distribution line. However, the result of the Shapiro-Wilk test shows a p-value of 0.0003, rejecting the hypothesis that the data follows a Gaussian distribution ($p < 0.001$). This is a common phenomenon in engineering practice with a large sample size ($N=1000$). A large sample size makes statistical tests extremely sensitive to minor deviations from an ideal normal distribution.

We can visually observe from the Q-Q plot that the data points are highly consistent with the theoretical nor-

mal distribution's reference line, with a correlation coefficient ($r=0.9964$), indicating a strong linear correlation between the data and the theoretical normal distribution. The Skewness is about -0.147 , and its absolute value is close to 0, which demonstrates a high degree of symmetry. Therefore, in engineering analysis and yield estimation, approximating this distribution as a Gaussian distribution is reasonable and effective. This simulation verification fully substantiates the feasibility and robustness of this design under manufacturing process fluctuations. The specification of the ROIC is shown in Table 2.

After completing the circuit simulation and design optimization, the layout design phase can be initiated. In this layout design, the Operational Amplifier, as the core module of the CTIA structure, has its performance critically determining the gain, noise, linearity, and stability of the entire readout circuit.

Therefore, during the layout design process of the OPA, we used dummy transistors to address the matching and symmetry requirements of the input differential pair transistors. These dummy transistors do not participate in the actual operation of the circuit. The role of dummy transistors is to place the active devices in a non-boundary region by adding equivalent layout structures on both sides of the input pair transistor array to mitigate edge effects. This approach effectively mitigates perfor-

Table 1 Monte Carlo simulation results
表 1 蒙特卡洛仿真数据结果

Model	Number	Mean	Std Dev	Skewness	Kurtosis	Jarque-Bera
Gauss	1000	$-33.75 \mu\text{V}$	$1.70 \mu\text{V}$	-0.147	0.674	22.56

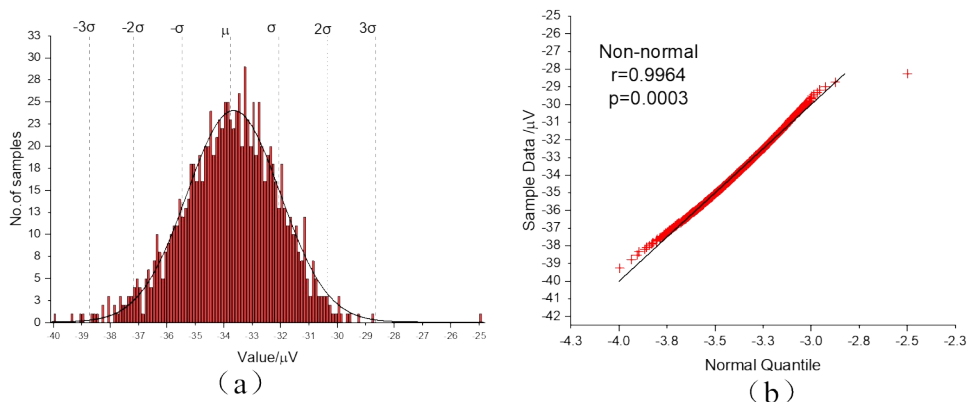


Fig. 11 Simulation results: (a) Monte Carlo simulation; (b) Q-Q plot.
图 11 仿真结果: (a)蒙特卡洛仿真结果; (b)Q-Q图

Table 2 Specification of the ROIC
表 2 读出电路参数

Parameters	Values	Remarks
Array Size	128 × 128 / 64 × 64 / 32 × 32	Reconfigurable by demand
Pixel Size	50 μm × 50 μm	
Supply Voltage	3.3 V	
Pixel Static Current	4.007 μA	
Pixel Power	13.2231 μW	
Total Array Power	13.64 mW / 54.16 mW / 216.64 mW	32 × 32 / 64 × 64 / 128 × 128
Intrinsic Noise(Pixel)	66.16 uV _{rms}	Integrated background noise
Equivalent Input Noise Charge	41.3 e ⁻	Calculated with C _f = 100fF
Transient Noise(Pixel)	2.17 mV _{rms}	Including switching spikes
Transient SNR	23.86 dB	Including switching spikes

mance deviations caused by process imperfections (such as uneven doping, asymmetric stress distribution, etc.), and significantly enhances the matching between devices and the overall symmetry of the layout.

To enhance the anti-interference capability and electrical stability of the analog circuit, we used guard ring structures around the periphery of critical analog regions in the OPA layout. The guard ring is formed by metal and p/n diffusion regions, and it is connected to ground or a specific bias potential. It serves to suppress substrate-coupled noise and stray charge injection, reduce the crosstalk resistance of parasitic PN junctions to suppress the Latch-up effect, and, by creating a low-impedance discharge path, effectively mitigate charge injection and clock feedthrough effects generated during the switching process of MOS devices^[21-22].

The aforementioned layout optimization measures significantly enhance the reliability and operational consistency of the OPA within a complex System-on-Chip (SoC) environment, providing a solid physical imple-

mentation foundation for the entire pyroelectric infrared detector readout circuit. These techniques were also applied to the layout of the remaining circuit blocks. Although the adoption of these techniques results in an increased layout area, it ensures superior signal integrity and precision, reflecting the inherent trade-offs in circuit design. Figure 12 shows the layouts for the unit cell, Bandgap, LDO and Column-Level Circuit.

4 Conclusions

As a highly cost-effective uncooled technology, pyroelectric infrared detectors have been widely applied, but the extraction of weak signals remains a key issue hindering performance improvement. The design process of the readout circuit in this paper reflects the trade-offs and compromises made in analog circuit design. Given that ROIC performance directly determines the detection capability of infrared systems, the market demand for high-performance readout chips is urgent. While current ROIC can satisfy many application scenarios, next-genera-

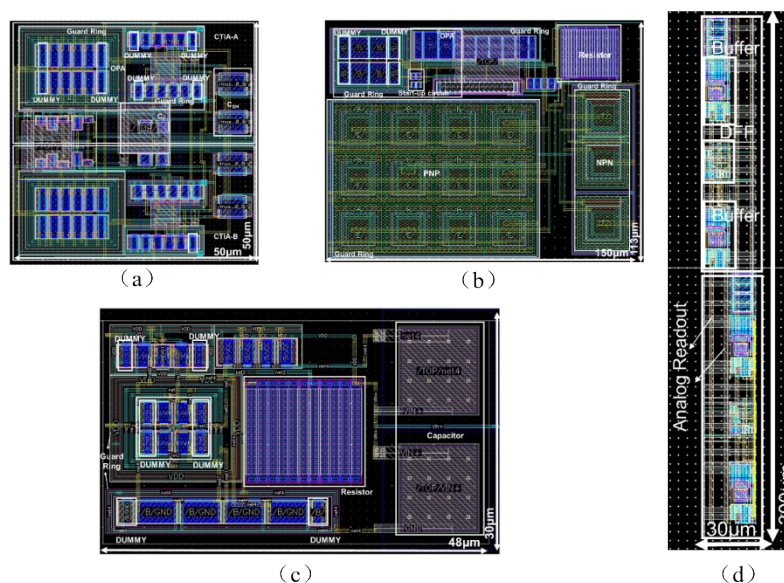


Fig. 12 Layout implementation. (a) the pixel circuit. (b) the bandgap reference. (c) the LDO regulator. (d) column-level circuit.
图 12 版图布局: (a)单元电路版图; (b)带隙基准版图; (c)低压差线性稳压源版图; (d)列级电路版图

tion intelligent optoelectronic systems demand that readout circuits possess capabilities for ultra-large-scale integration, sensing-computing fusion, and software-hardware co-design^[23-24]. Integrating dedicated processing units directly into the ROIC architecture has now emerged as a key development trend. This trend aims to enhance the detector's real-time data processing capability and offers new solutions for target recognition and tracking in complex environments. With the maturation of AI algorithms and hardware computing power, the strategic importance of intelligent ROIC technology in future optoelectronic systems is set to continually increase.

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基于双 CTIA 的热释电红外探测器读出电路设计

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摘要: 为了实现对热释电红外探测器极弱信号的检测和高灵敏度应用场景中的需求, 提出了一种具有可变阵列规模的双电容跨阻放大器(CTIA)读出结构, 并设计了带隙基准(Bandgap)、低压差线性稳压源(LDO)作为偏置电路提供电压偏置, 以满足低噪声、低功耗、大动态范围和便携式的需求。采用 TSMC 0.18 μm 1P6M 工艺设计电路, 电源电压为 3.3V, 并对其版图进行绘制, 采用伪晶体管(Dummy)结构、保护环(Guard Ring)结构, 以提升器件之间的匹配度和版图整体的对称性以及模拟电路的抗干扰能力与电气稳定性。

关键词: 热释电; 读出电路; 双 CTIA; 可变阵列规模; 偏置电路

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