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664 GHz sub harmonic mixer based on "T" anode GaAs SBD membrane circuit

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Abstract: 664 GHz sub harmonic mixer for ice cloud detection was designed and fabricated, based on 0. 5 μm "T" anode GaAs SBD membrane integrated process with thickness of 5 μm. Parasitic parameters of "T" anode design were analyzed and membrane process was developed to improve high frequency performance. The mixer was characterized in 664 GHz receiver setup. Double side band conversion loss of the mixer was 9. 9 dB at 664 GHz room temperature.

Key words: GaAs SBD, membrane circuit, sub harmonic mixer

基于T形阳极GaAs肖特基二极管薄膜集成电路工艺的664 GHz次谐波混频器

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摘要:报道了用于冰云探测的基于0.5 μm T形阳极砷化镓肖特基二极管薄膜集成电路工艺664 GHz次谐波混频器。为降低器件寄生参数,提升太赫兹频段电路性能,设计并分析了了T形阳极GaAs SBD器件结构,开发了厚度仅5 μm的薄膜电路工艺。混频器芯片组装成664 GHz接收模块,经测试室温下664 GHz最小双边带变频损耗达到9.9 dB。

关 键 词:砷化镓肖特基二极管;薄膜电路;次谐波混频器

中图分类号:TN304.2;TN315+.3;TN773 **文献标识码**:A

Introduction

As an important application area of terahertz technology, monitoring ice clouds from airplane or satellite with terahertz heterodyne receivers can provide data for atmosphere water cycle research and precise weather report. It has been supported by several airplane or satellite payload programs such as NASA's CoSSIR[1], ESA's ISMAR[2] and ICI[3]. 664GHz is one of the ice particle sensitive channels included by above programs. GaAs SBD mixer is usually considered as a compact, low noise technique for 664GHz airborne heterodyne receiver[4].

As a basic element of terahertz mixer, GaAs SBD has been developed for decades from the early dot-matrix

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whisker-contacted style to planar type [5]. With the commercial success, structural improvement reports of GaAs SBD become rare, while research focus has shifted to the new materials such as GaN SBD [6] and InP SBD [7]. However, GaAs SBD maintain its status as high cutoff frequency, low noise, low cost device ready to meet higher and higher frequency demand of varies terahertz application. Therefore, a GaAs SBD is still needed to be evolved both at device structure and integrated process constantly.

For working frequency at 664GHz, traditional circuits on 25~50μm GaAs or quartz substrate are not suitable because substrate mode effect and transition loss become severer[8]. To alleviate substrate effects in high terahertz circuit, GaAs membrane integrated process has been developed and demonstrated to sustain SBD circuit of frequency up to 2.7 THz [9].

In this paper, a 664 GHz sub-harmonic mixer based on 5μm membrane GaAs SBD process was presented. "T" shape anode contact was designed and analyzed to indicate a new way to improve cutoff frequency f_t. The membrane mixer chip was packaged in a waveguide module for measurement. Double side band (DSB) conversion loss of 9.9 dB at 664 GHz was achieved.

1 Device design and fabrication

Analogous to HEMT T gate [10], a circular "T" shape anode contact metal of GaAs SBD was designed. Compared with contact metal deposited in SiO_2 anode well [11], "T" anode could provide a smaller junction parallel capacitance C_{jp} (in some paper denoted as part of C_{fp}) while scaling down anode diameter into sub micron anode area, and maintaining a large contact area with air bridge metal. C_{jp} of "T" anode mainly originates from metal "cap" (see Fig. 1(a)). Therefore, increasing "post" metal height could directly reduce C_{jp}.

In order to have a higher performance at 664 GHz, epitaxy material was optimized (as shown in Table1). Additional undoped GaAs layer and an etch-stop AlGaAs layer was inserted beneath n+GaAs layer, worked as the membrane substrate instead of the original GaAs substrate.

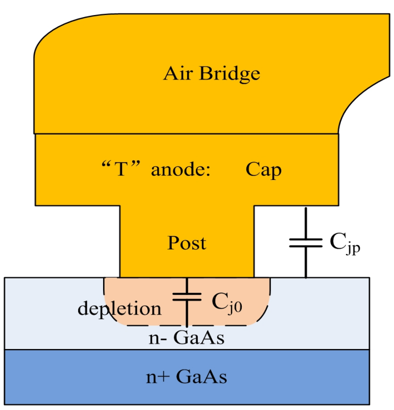
Table 1 Epitaxy layer structure of GaAs SBD membrane circuit

表1 GaAs SBD薄膜电路的外延层结构

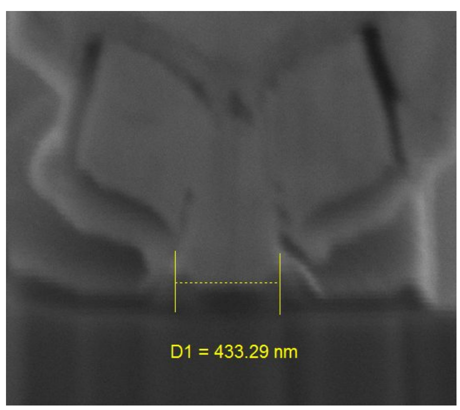
Layer function	Material	Doping	Thickness
Schottky contact	GaAs	n−, 1e17cm^{-3}	100nm
Ohmic contact	GaAs	n+, 7e18cm^{-3}	1μm
Membrane	GaAs	nid	5μm
Etch−stop	AlGaAs	nid	50nm
Substrate	GaAs	S. I.	/

To investigate the relationship between diode performance and anode dimension, "T" anode GaAs SBD with different anode diameter from 0.5 μm (shown in Fig. 1(b)) to 2.1 μm were fabricated. R_s was extracted through IV curves. C_{j0} and C_{jp} as a total junction capacitance was extracted through *S* parameters. In order to distinguish C_{jp} from C_{j0}, C-V measurement were carried out on large anode (diameter range from 50 μm to 200 μm) SBD devices on the same wafer. While C_{jp} could be neglected compared with C_{j0} of these large diodes, the extracted capacitance per anode area was 2.4fF/μm^2, which could be used to calculated the intrinsic C_{j0} of small anode diodes.

Extracted R_s, C_{j0} and C_{fp} were compared in Fig. 2(a). While scaling down anode area, $1/R_s$ deviated from linear with anode area because of complicated current distribution in n-/n+ GaAs beneath anode. Particularly, in the anode area region below 1μm^2, the slope of $1/R_s$ shown a flattening tread, which helped increase intrinsic cutoff frequency f_t calculating with only R_s and C_{j0}, as shown in Fig. 2(b). It indicated a smaller anode area would have a higher f_t. For the 0.5μm diameter diode, intrinsic f_t reached 10.5 THz. However, C_{jp} didn't show a linear relationship with anode area, which stopped f_t' calculated with R_s and $C_{j0}+C_{jp}$ increasing while reducing anode area. The highest f_t' reached 7.7 THz. There-



(a)



(b)

Fig. 1 "T" shape anode of GaAs SBD: (a) schematic picture with C_{jp} and C_{j0}; (b) SEM picture of 0.5 μm anode metal section.

图1 T形阳极GaAs SBD:(a)包含Cjp与Cj0的示意图;(b)0.5 μm阳极金属剖面扫描电子显微镜图。

fore, in odder to improve f_t' by scaling down anode area below 1 μm^2, efforts should be paid on decreasing C_{jp}. For "T" anode design, increasing "post" metal height would be a direct way.

2 Mixer design and fabrication

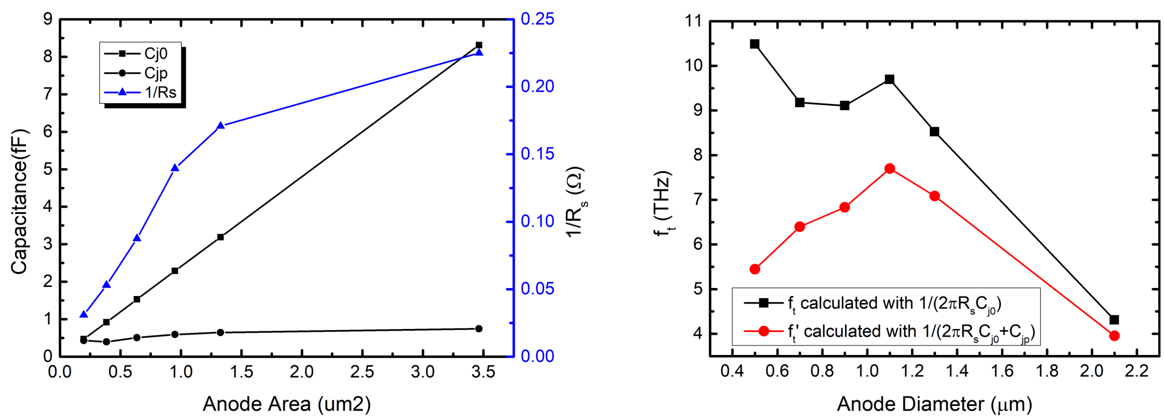
As depicted in fig. 3(a), to halve LO frequency require, sub harmonic mixer structure was adopted based on our 5 μm GaAs membrane process. Compared with hybrid integrated quartz circuit, monolithic integrated membrane circuit is virtually immune from alignment error and substrate mode effect. Anti parallel SBD structure was used to suppress odd order harmonic component and increase the sub harmonic component. Suspended micro strip probes were designed to connect RF/LO waveguide with CPW main circuit. Edge of CPW's ground metal and DC ground connect component was fabricated as suspended beamlead in chip process, and welded on the metal cavity. In order to sustain membrane chip's mechanical strength, several breaks along CPW's ground line were inserted to release stress between metal and GaAs membrane which originated from chip process.

0.5 μm anode diameter diode was chosen for mixer design instead of 1.1 μm diode which has a better f_t' because when designing the mixer circuit, estimation of different SBD had not finished. 0.5 μm was expected to have a better performance when C_{jp} was under-evaluation.

Fabrication process started with cathode contact deposition and annealing. Then "T" shape anode contact was vaporized, followed by air bridge electroplating. After mesa etching, CPW and beamlead metal was electroplated on the membrane layer surface. When finished the front side processes, the wafer substrate was mechanically thinned, polished and etched completely, leaving back side of the membrane layer exposed. Finally membrane process were finished by removing gap area between chips through backside lithography and etching. The sub harmonic mixer of "T" anode GaAs SBD membrane process was finished and welded in the metal housing as shown in Fig. 3(b).

3 Receiver module demonstration

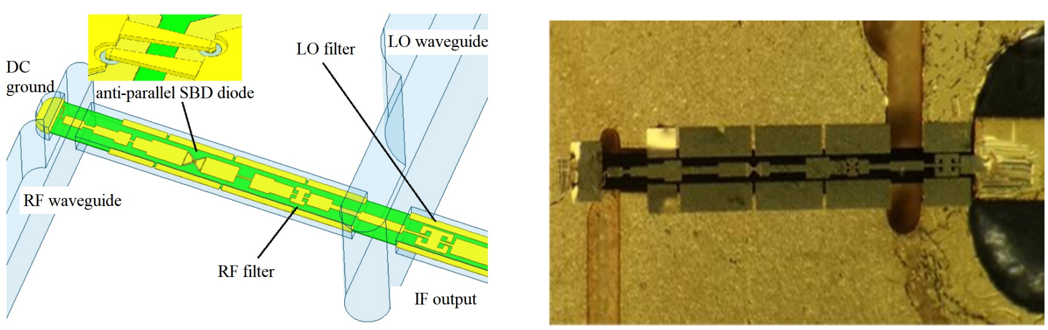
A 664 GHz receiver was assembled based on our membrane sub harmonic mixer, as shown in Fig. 4(a).



(a) (b)

Fig. 2 Characteristics of "T" shape anode GaAs SBD with different anode size: (a)C_{j0}, C_{jp} and $1/R_s$ versus anode area; (b)f_t versus anode diameter.

图2 不同阳极接触尺寸的T形阳极GaAs SBD特性:(a)Cj0,、Cjp及1/Rs与阳极面积关系;(b)ft与阳极直径关系。



(a) (b)

Fig. 3 GaAs membrane sub harmonic mixer design: (a) 3D design diagram; (b) microscope picture of the finished mixer.

图3 GaAs薄膜次谐波混频器设计:(a)三维设计结构图;(b)制作完成的混频器显微镜照片

24x multiplier chain module was connected to the LO waveguide, provided 3 mW LO power. IF port was connected with a low noise amplifier (LNA). To estimate double side band conversion loss, measurement setup was established as shown in Fig. 4(b). A black body radiation source was used as cold and hot noise source. Frequency synthesizer provided fundamental frequency for the multiplier chain. Spectrum analyzer was used to monitor IF output.

Y factor measurement[12] was conducted under 77 K and 290 K. IF frequency was fixed at 3GHz. Subtracting LNA and antenna's noise figure, double side band (DSB) conversion loss of the mixer was attained. As shown in Fig. 5, DSB conversion loss was less than 11dB in 654~675 GHz range, and less than 14 dB in 646~677 GHz range. Optimum value was 9.9 dB attained at 664 GHz.

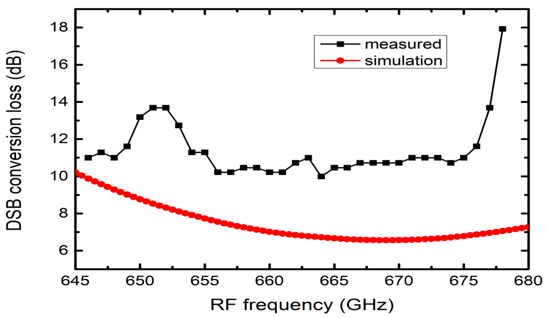


Fig. 5　Measured and simulated DSB conversion loss of the membrane mixer
图5　薄膜混频器双边带变频损耗测试与仿真曲线

The simulated DSB conversion loss was also depicted in Fig. 5, showed 4~5 dB lower than measured data, indicating potentials of “T” anode GaAs SBD membrane process has not been fully developed.

4 Conclusion

Sub micron “T” anode GaAs SBD and 664GHz sub harmonic membrane mixer were reported. Performance of “T” anode GaAs SBD with different anode area was investigated to further improve f_t in sub micron anode region. 664 GHz sub harmonic mixer based on 0.5 μm GaAs SBD with 5μm GaAs membrane chip was designed and fabricated. DSB conversion loss of 9.9 dB at 664GHz was achieved.

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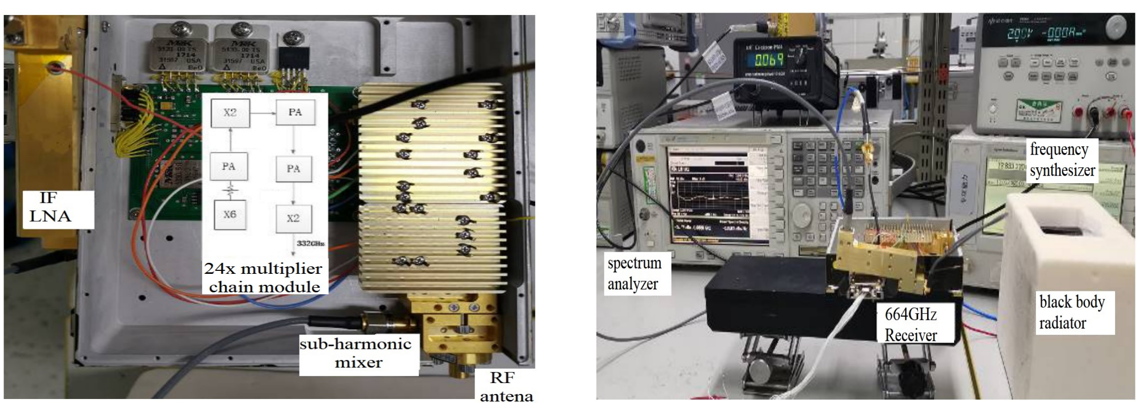

(a)　　(b)

Fig. 4　Pictures of 664GHz receiver (a) and measurement setup (b)
图4　664GHz接收机照片(a)与测试装置(b)