Cavity-backed on-chip patch antenna in 0.13 μm SiGe BiCMOS technology

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Abstract: This letter presents a 340 GHz cavity-backed on-chip patch antenna design and fabrication using standard 0.13 μm SiGe BiCMOS technology. The patch placed at AM layer is fed by a stripline at LY layer through via holes from LY to AM layer. The via holes are built between the top metal layer (AM layer) and the ground plane (M1 layer) to form a cavity which improves the impedance matching bandwidth and the radiation performances of the antenna. The proposed antenna shows a simulated impedance bandwidth of 9.2 GHz from 335.6 to 344.8 GHz for S11 less than -10 dB. The simulated gain of the antenna at 340 GHz is 3.2 dBi. The total area of the antenna is 0.5 × 0.56 mm².

Key words: 0.13 μm SiGe BiCMOS technology, cavity-backed patch antenna, on-chip antenna

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Introduction

In recent years, with the high development of CMOS and BiCMOS integrated circuit (IC) technologies, silicon-based ICs at mm-wave and THz frequencies have opened up opportunities for many applications such as short range imaging and medical applications. As the key component in a communication system, an antenna has independent properties that affect the system as a whole. Fully integrated on chip antennas (OCAs) can eliminate the need for off-chip connection and packaging processes which would introduce extra loss and make the overall size bulky. Moreover, fully integrated OCAs reduce the overall form-factor of the system and facilitate assembly as high precision mm-wave interconnects are eliminated. Many CMOS/BiCMOS OCAs have been fabricated and studied based on slot dipole, folded dipole, Yagi patch and inverted-F. However, most OCAs perform poor radiation efficiency due to the low resistivity and high permittivity of the losy silicon substrate. Several techniques have been...
reported to improve the radiation performance of OCAs including micromachining dielectric resonators antennas (DRAs) artificial magnetic conductor (AMC) concept. However, these design methods increase the design complexity and are usually costly. Substrate integrated waveguide (SIW) technique has been widely used in printed circuit board antenna designs. SIW cavity-backed antenna is a good candidate for silicon-based integrated systems [1]. In Ref. [3], a 340 GHz single antenna and a 2 x 2 antenna array are designed using SIW cavity-backed slot-loaded magnetic loop structure in 0.13 μm SiGe BiCMOS technology. The maximum gains of the antenna element and array are 3.3 dBi and 7.7 dBi respectively. In Ref. [11], an SIW slot antenna is designed in 0.13 μm SiGe BiCMOS technology and achieves a gain of ~0.5 dBi at 410 GHz.

In this paper, a 340-GHz cavity-backed on-chip patch antenna is presented. The proposed antenna is fabricated using standard 0.13-μm SiGe BiCMOS technology without any postprocesses. The patch is fed by a strip line placed at LY layer and some rows of vias from LY to AM layer. A backed cavity is designed to improve the impedance bandwidth and the radiation performances of the antenna. The cavity is formed by the top metal layer (AM) connected to the bottom metal layer (M1) through vias in between. The proposed antenna shows a simulated impedance bandwidth of 9.2 GHz from 335.6 to 344.8 GHz for S11 less than –10 dB. The simulated gain of the antenna at 340 GHz is 3.2 dBi.

1 Antenna Design

Fig. 1 illustrates the chip environment used in this design. There are seven metal layers over the silicon substrate. The inter-metal dielectric is SiO2 with a relative permittivity of 4.1 and a loss tangent of 0.0023 at 340 GHz [12]. The total thickness from the top metal layer (AM) to the bottom metal layer (M1) is around 17.12 μm. The silicon substrate has the thickness of 250 μm. Above AM there is a passivation layer with a thickness of 4.3 μm. The geometry of the proposed OCA is presented in Fig. 2. The patch is placed on the topmost metal layer (AM). An annular ring slot is etched on AM layer. The M1 layer is used as ground plane. A coplanar waveguide (CPW) structure is designed for antenna measurement. The feeding strip line placed at LY layer is connected to the CPW input by a transition as shown in Fig. 2 (c). At the end of the strip line eleven rows of vias from LY to AM are designed to feed the patch which improves the impedance matching of the antenna. The SIW cavity is formed by the top metal layer (AM) connected to the bottom metal layer (M1) through vias in between.

Fig. 3 illustrates three different antennas: (1): patch antenna; (2): patch antenna with annular slot; (3): patch antenna with annular slot and backed cavity (proposed antenna). The simulated results of reflection coefficient for these three antennas are shown in Fig. 4. It can be observed that another higher resonant frequency at 343.7 GHz is generated by introducing the SIW backed cavity structure. The additional higher frequency resonance in combination with the original lower one at 337.6 GHz of the patch mode broadens the bandwidth.
of the antenna. E-field distributions of the proposed antenna at 337.6 GHz and 343.7 GHz are illustrated in Fig. 5. Fig. 5 (a) and (c) show the E-field distributions at 337.6 GHz on planes $z = 17 \mu m$ and $z = 10 \mu m$ respectively. It is observed that the field distributions at the lower resonant frequency is actually the TM$_{10}$ mode of the patch antenna. Fig. 5 (b) and (d) show the E-field distributions at 343.7 GHz on planes $z = 17 \mu m$ and $z = 10 \mu m$ respectively. The field distributions at the higher resonant frequency is the TE$_{110}$ mode of the cavity.

The width of the cavity $W_{\text{SIW}}$ and the gap between annular ring slot and SIW side wall along x-direction $L_{\text{RS}}$ are two key parameters for tuning the antenna. Fig. 6 (a) and (b) present the behaviors of the two resonances as $W_{\text{SIW}}$ and $L_{\text{RS}}$ change respectively. As shown in Fig. 6 (a) the higher resonant frequency shifts down to lower frequency while $W_{\text{SIW}}$ increases (other parameters keeping unchanged) which degrades the impedance matching at the lower resonant frequency. Similar conclusion can be got from Fig. 6 (b) as $L_{\text{RS}}$ increases. The above simulated results and analyses prove that we can optimize the dimensions of the backed cavity structure to tune the higher frequency resonance. It’s noted that the width of the annular slot $W_g$ is also a key parameter to tune the two resonances and the impedance bandwidth in antenna design.
and without feeding vias. It is observed that these feeding vias improve the impedance matching of the antenna. It is noted that the positions of two resonances are hardly influenced by the existence of the feeding vias. Fig. 8 shows antennas with \( N = 1 \), \( 2 \), \( 6 \) rows of feeding vias. The illustration for \( N = 11 \) can be seen in Fig. 2(c).

Antennas with different \( N \) are simulated and the simulated reflection coefficient results are shown in Fig. 9. The impedance matching of the antenna improves as the number of rows increases. The optimized dimensions of the proposed antenna are listed in Table 1.

![Reflection coefficients of antennas with and without feeding vias](image)

**Fig. 7** Reflection coefficients of antennas with and without feeding vias

<table>
<thead>
<tr>
<th>( N ) rows of feeding vias</th>
<th>( N = 1 )</th>
<th>( N = 2 )</th>
<th>( N = 6 )</th>
</tr>
</thead>
<tbody>
<tr>
<td>(a)</td>
<td>(b)</td>
<td>(c)</td>
<td></td>
</tr>
</tbody>
</table>

![Antennas with \( N \) rows of feeding vias](image)

**Fig. 8** Antennas with \( N \) rows of feeding vias. (a) \( N = 1 \), (b) \( N = 2 \), (c) \( N = 6 \)

Table 1 Optimized dimensions of the proposed antenna (unit: \( \mu m \))

<table>
<thead>
<tr>
<th>Parameters</th>
<th>( W )</th>
<th>( L )</th>
<th>( W_{\text{off}} )</th>
<th>( L_{\text{off}} )</th>
<th>( L_{m} )</th>
<th>( W_{y} )</th>
<th>( L_{y} )</th>
<th>( W_{x} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>Value</td>
<td>500</td>
<td>560</td>
<td>455.5</td>
<td>429.5</td>
<td>109.7</td>
<td>70</td>
<td>200</td>
<td>35</td>
</tr>
</tbody>
</table>

2 Results and discussions

Fig. 10 presents the micrograph of the proposed antenna. The antenna was measured with the setup shown in Fig. 11. The fabricated antenna is measured based on the Cascade Microtech Elite-300 probe station and Keysight PNA-X (N5247A) with the VDI extender providing the signal source from 220 ~ 330 GHz. Due to the limitations of the highest measurement range of the vector network analyzer (VNA) which reach to 330 GHz only the frequencies of \( S_{11} \) lower than 330 GHz were obtained.

The measured and simulated reflection coefficients of the proposed antenna are presented in Fig. 12. It is observed that the simulated -40 dB impedance bandwidth are 9.2 GHz from 335.6 to 344.8 GHz. The measured -10 dB impedance bandwidth starts from 327.8 GHz while the simulated one starts from 335.6 GHz. Considering such a high operating frequency \( a 2.3% \) deviation of about 7.8 GHz between the simulated starting frequency and the measured starting frequency is acceptable. It can be estimated that the measured result agrees well with the simulated one based on the available data. The discrepancy between the simulated results and measured results mainly results from measurement setup and the deviation of the silicon substrate characteristics setting in the simulation from its actual values. Fig. 13 shows the simulated gain patterns in \( xoz \)-plane and \( yoz \)-plane at 340 GHz. The simulated gain at 340 GHz is 3.2 dBi. As shown in Fig. 14, the maximum simulated radiation effi-

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Table 2 Performance comparison with reported works

<table>
<thead>
<tr>
<th>Ref</th>
<th>Type</th>
<th>Process</th>
<th>BW (AR BW)</th>
<th>Freq. (GHz)</th>
<th>Gain (dBi)</th>
<th>Radiation efficiency</th>
<th>Area (mm$^2$)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>AMC</td>
<td>0.18 ( \mu m ) CMOS</td>
<td>28.3%</td>
<td>65</td>
<td>-4.4 (Measured)</td>
<td>n.a.</td>
<td>1.8 x 1.8</td>
</tr>
<tr>
<td>2</td>
<td>Cavity-backed slot loop</td>
<td>0.13 ( \mu m ) SiGe BiCMOS</td>
<td>4%</td>
<td>340</td>
<td>3.7</td>
<td>48% (Simulated)</td>
<td>0.7 x 0.7</td>
</tr>
<tr>
<td>3</td>
<td>Slot</td>
<td>0.09 ( \mu m ) CMOS</td>
<td>15.8%</td>
<td>60</td>
<td>-2.1 (Simulated)</td>
<td>19.6% (Simulated)</td>
<td>1.3 x 1.1</td>
</tr>
<tr>
<td>4</td>
<td>Dipole</td>
<td>0.13 ( \mu m ) SiGe BiCMOS</td>
<td>&gt;25%</td>
<td>160</td>
<td>-7.6 (Simulated)</td>
<td>n.a.</td>
<td>0.5 x 0.5</td>
</tr>
<tr>
<td>5</td>
<td>Yagi</td>
<td>0.18 ( \mu m ) CMOS</td>
<td>16.7%</td>
<td>60</td>
<td>-10.6 (Measured)</td>
<td>10% (Simulated)</td>
<td>1.1 x 0.95</td>
</tr>
<tr>
<td>6</td>
<td>Patch</td>
<td>0.045 ( \mu m ) CMOS</td>
<td>n.a.</td>
<td>410</td>
<td>5 (Simulated)</td>
<td>50% (Simulated)</td>
<td>0.2 x 0.2 (Patch size)</td>
</tr>
<tr>
<td>7</td>
<td>Inserted-F</td>
<td>Post-back-end-fed-line</td>
<td>20.4%</td>
<td>61</td>
<td>-19 (Measured)</td>
<td>3.5% (Simulated)</td>
<td>n.a.</td>
</tr>
<tr>
<td>8</td>
<td>SIW slot</td>
<td>0.13 ( \mu m ) SiGe BiCMOS</td>
<td>n.a.</td>
<td>400</td>
<td>-5.5 (Simulated)</td>
<td>49.4%</td>
<td>n.a.</td>
</tr>
<tr>
<td>This work</td>
<td>Cavity-backed Patch</td>
<td>0.13 ( \mu m ) SiGe BiCMOS</td>
<td>2.7%</td>
<td>340</td>
<td>3.2 (Simulated)</td>
<td>56.7% (Simulated)</td>
<td>0.5 x 0.56</td>
</tr>
</tbody>
</table>
ciency is 56.7% at 340 GHz.

Table 2 lists the performance comparison of the proposed antenna with the reported works. It can be seen that the proposed antenna enhanced the gain and radiation efficiency using SIW backed cavity without any post process. The proposed antenna also achieves higher gain and radiation efficiency.

3 Conclusions

This paper presents a study of the performance of an on-chip cavity-backed patch antenna designed and fabricated with 0.13 μm SiGe BiCMOS process. The square patch is placed at AM layer fed by a strip line placed at LY layer and some rows of vias from LY to AM layer. An SIW backed cavity is designed to improve the impedance bandwidth and the radiation performances of the antenna. The proposed antenna shows a simulated impedance bandwidth of 9.2 GHz from 335.6 to 344.8 GHz for S11 less than -10 dB. The simulated gain of the antenna at 340 GHz is 3.2 dBi. The total area of the antenna is 0.5 × 0.56 mm².

References


References


