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Correlation between the whole small recess offset and electrical performance of InP-based HEMTs

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Abstract: In this work, we investigate the impact of the whole small recess offset on DC and RF characteristics of InP high electron mobility transistors (HEMTs). L_g = 80 nm HEMTs are fabricated with a double-recessed gate process. We focus on their DC and RF responses, including the maximum transconductance (g_{m_max}), ON-resistance (R_{ON}), current-gain cutoff frequency (f_T), and maximum oscillation frequency (f_{max}). The devices have almost same R_{ON}. The g_{m_max} improves as the whole small recess moves toward the source. However, a small gate to source capacitance (C_{gs}) and a small drain output conductance (g_{ds}) lead to the largest f_T, although the whole small gate recess moves toward the drain leads to the smaller g_{m_max}. According to the small-signal modeling, the device with the whole small recess toward drain exhibits an excellent RF characteristics, such as f_T = 372 GHz and f_{max} = 394 GHz. This result is achieved by paying attention to adjust resistive and capacitive parasitics, which play a key role in high-frequency response.

Key words: InP high-electron-mobility transistor (InP HEMT), InGaAs/InAlAs, DC/RF characteristic, small-signal modeling, double-recessed gate process

InP基HEMT的整体小凹槽偏移与电学性能的相关性

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摘要:在这项工作中,我们研究了整个小凹槽偏移对InP高电子迁移率晶体管(HEMT)的直流和射频特性的影响。L_g=80 nm HEMT采用双凹栅极工艺制造。我们重点关注它们的直流和射频响应,包括最大跨导($g_{m,max}$)、导通电阻(R_{ON})、电流增益截止频率(f_T)和最大振荡频率(f_{max})。这些设备具有几乎相同的R_{ON}。随着整个小凹槽向源移动,$g_{m,max}$会提高。然而,尽管整个小栅极凹槽向漏极移动会导致较小$g_{m,max}$,但较小的栅源电容(C_{gs})和较小的漏极输出电导(g_{ds})会导致最大的f_T。根据小信号建模,整个小凹槽朝向漏极的器件表现出优异的射频特性,例如f_T=372 GHz和f_{max}=394 GHz。这一结果是通过注意调整电阻和电容寄生效应来实现的,这些寄生效应在高频响应中起着关键作用。

关键词:InP高电子迁移率晶体管(InP HEMT);InGaAs/InAlAs;DC/RF特性;小信号建模;双凹栅工艺

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Introduction

III-V compound semiconductors, represented by InP, have recently emerged as a technology of choice for Tera-Hz (THz) applications due to their low noise, low power consumption and high gain performance[1]. Northrop Grumman Space Technology first implemented the device with maximum oscillation frequency (f_{max}) exceeding 1 THz in 2007[2]. In addition, their group successfully pushed the InP HEMT amplifier technology to 850 GHz for the first time in 2014[3]. Currently, the record for current-gain cutoff frequency (f_T) is 750 GHz @ gate length (L_g) = 20 nm[4] and f_{max} is 1.5 THz @ L_g = 25 nm[5]. Therefore, it is imperative to scale the physical gate length (L_g) to improve the frequency response of the device. However, the L_g cannot be reduced indefinitely. According to delay-time analysis[6], as the L_g decreases, the transit time under the gate τ_{text} decreases sharply, resulting in a sharp increase in the proportion of extrinsic channel-charging delay τ_{text}. Therefore, reducing τ_{text} is another means to improve the device performance.

τ_{text} is related to the parasitic resistance and parasitic capacitance. For the parasitic resistance, in addition to use multiple heavily doped cap layers[7,8], it is to reduce the width of the gate recess to minimize parasitic series resistances, such as the source and drain resistance (R_S and R_D)[9]. The extrinsic capacitance can be decreased by increasing the spacing of gate recess or making a cavity structure[10].

The gate recess process is the most critical process for InP HEMTs manufacturing, which has a significant impact on parasitic series resistances and capacitance. Kim *et al.* studied the effects of the side-recess spacing (L_{side}), reporting that increasing L_{side} has a large impact on the subthreshold characteristics of the device due to a significant reduction of the gate leakage current and an improvement in its electrostatic integrity[11]. Both Samnoun *et al.* [12] and Shinoharal *et al.* [13] investigated the asymmetric gate recess technology, reporting that increase of the drain side recess (L_{RD}) improves the f_{max} due to the reduction of output conductance g_{ds} and capacitance C_{gd}. In addition, Suemitsu *et al*[14]. and Kim *et al*[15]. developed a two-step-recessed gate process that improves high-speed performance.

However, seldom people have studied the impact of the asymmetric gate recess technology on two-step-recessed gate process. Therefore, it is imperative to carefully investigate the impact of the whole small recess offset in a double-recessed gate process on improving the high-frequency characteristics of InP HEMTs.

1 Process technology

Table 1 shows the Gas Source Molecular Beam Epitaxy (GSMBE)-grown epitaxial layer structure on 3 inch semi-insulating InP (100) substrates that is used in this paper. In order to suppress the kink effect, the channel features a lattice-matched $In_xGa_{1-x}As$ with an indium content of 53%. In addition, a multi-layer cap structure that combines a heavily Si-doped multi-layer cap ($In_{0.65}Ga_{0.35}As/In_{0.53}Ga_{0.47}As/In_{0.52}Al_{0.48}As$) were used to minimize a tunneling resistance associated with the barrier layer between the cap and channel layer. The concentration of Si-doping to a multi-layer cap is 3.0×10^{19}, 1.0×10^{19}, and 1.0×10^{19} cm^{-2} respectively. The 4-nm InP layer acts as an effective gate recess etch-stopper. Hall measurements were carried out at room temperature, showing the carrier mobility of over 10 000 $cm^2/(Vs)$ and the two-dimensional (2-DEG) sheet density of 3.26×10^{12} cm^{-2}.

Table 1 Epitaxial layer structures of the InGaAs HEMTs that are fabricated in this paper
表1 本文所做的InGaAs HEMT的外延层结构

N++ Cap	InGaAs, x = 0.65	10 nm
N+ Cap	InAlAs, x = 0.53	15 nm
N+ Cap	InAlAs, x = 0.52	15 nm
Stopper	InP	4 nm
Barrier	InAlAs, x = 0.52	8 nm
δ-doping	Si	–
Spacing	InAlAs, x = 0.52	3 nm
Channel	InGaAs, x = 0.53	15 nm
Buffer	InAlAs, x = 0.52	500 nm
3 Inch Semi-insulating InP (100) Substrate		

In order to avoid the degradation of the epitaxial structure by high temperature, the temperature of wafer in the whole fabrication process is lower than 300 ℃. Similar to our pervious work[16], mesa isolation is achieved by using multiple acids to successively etch the epitaxial layer to the buffer layer. After device isolation, source-drain metal electrodes are formed by Ti/Pt/Au (15 nm/15 nm/50 nm) with thermal annealing. The distance between source and drain electrode was designed to be 2.4 μm. The double-recessed gate process used to fabricate the T-shaped gates was as follows. Firstly, a SiO_2 thin film was deposited by plasma-enhanced chemical vapor deposition (PECVD) to improve adherence of photoresist. And the opening size of the SiO_2 mask was used to control the width of large gate recess. Next, the SiO_2 mask was etched by reactive ion etching (RIE) using CF_4 plasma after defining the gate-recess region by electronic beam lithography (EBL). After RIE, the InGaAs cap layer was removed by a mix solution of citric acid ($C_6H_8O_7$) and hydrogen peroxide (H_2O_2) to form the large gate recess, where it was measured about 500 nm.

To abtain a small gate recess, a e-beam gate process was developed, which is shown in Table 1. The PMMA/Al/UVIII e-beam stack layers were used to define the gate and small gate recess. In order to avoid the miscible of the two photoresist layers, the metal Al layer is used for isolation, and it is easily soluble in alkaline developer. The top UVIII resist was exposed by a small dose and wide line. After that, the gate head was determined by TMAH development and rinsed in DI water. Subsequently, the gate foot was defined on a single layer of PMMA resist and was exposed by a big dose and narrow line. The InAlAs cap layers were etched by H_3PO_4-solution

down to the InP layer acting as an etch-stopped layer, where the small recess was measured about 100 nm. After the formation of the small recess, Ti/Pt/Au (3 nm/25 nm/350 nm) metals were evaporated and lifted off to form the T-shaped gate. The length of gate foot was 80 nm, and the gate stem was adjusted to be 250 nm to alleviate parasitic capacitances.

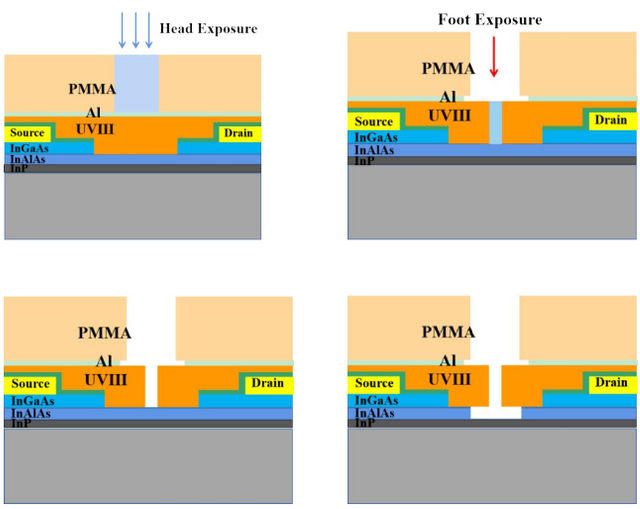


Fig. 1 The EBL process for T-gate fabrication and small gate recess (The layers below the InP etch-stopped layer are not shown)
图1 用于T栅极制造和小栅极凹槽的EBL工艺(未显示InP蚀刻停止层下方的层)

The whole small recess could be located at the large recess center, or with an offset toward source/drain, where the position of gate metals was in the middle of the small recess. The offsets from large recess center were 0.0 μm (type A), -0.1 μm (type B), and +0.1 μm (type C).

Finally, these devices were covered with a 20-nm-thick Si_3N_4 dielectric film by PECVD (280 ℃). The SEM image of the cross section of the fabricated device is shown in Fig. 1, which is the whole small recess toward source.

2 DC & microwave characteristics

DC characteristics of devices were measured by an HP4142 semiconductor parameter analyzer. Figure 3(a) shows the typical output characteristics of the InP-based InGaAs/InAlAs HEMTs with 80-nm gate length and 50 μm × 2 gate width. These devices exhibit good pinchoff and excellent current saturation characteristics up to V_{DS} = 1.2 V. The type A device exhibits a better drain current driving capability (I_{D_max}). These devices exhibit the almost same ON-resistance (R_{ON}), which is about 0.70 Ω·mm. This is because the ohmic contact and access resistance components are the same during the whole small recess offset. The drain and source resistances (R_D and R_S) are estimated from dc-measurements ($R_S + R_D \approx 0.546$ Ω·mm), it can be also extracted from

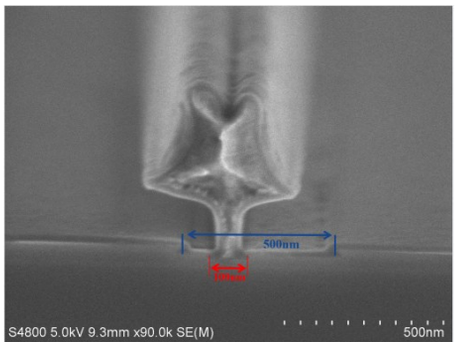


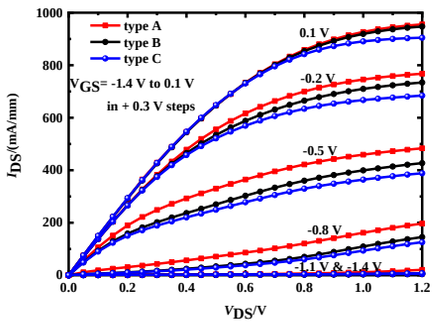
Fig. 2 SEM image of the cross section of the fabricated device with the whole small recess toward source (type B), where the large gate recess was measured about 500 nm and the small recess was measured about 100 nm
图2 所制造器件横截面的SEM图像,整个小凹槽朝向源极(B型),其中大栅极凹槽测量值约为500 nm,小凹槽测量值约为100 nm

small signal equivalent circuit (SSEC) using a cold FET method [16].

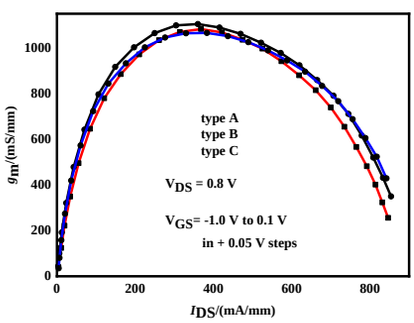
Figure 3(b) shows the measured transconductance (g_m) of the L_g = 80 nm devices as a function of I_{DS} at a drain bias of 0.8 V. As the I_{DS} increases, the g_m increases firstly up to the g_{m_max} and than decreases gradually. The type B device with the whole small recess toward source exhibits the largest g_{m_max}, which is 1105 mS/mm. The best characteristic arises from the smaller R_S.

Figure 4 shows the dependence of the DC drain conductance (g_{ds_dc}) on appiled V_{DS}. The V_{GS} takes the voltage value corresponding to the g_{m_max}. When V_{DS} increases, the g_{ds_dc} of these devices decreases sharply at first and then decreases slowly. When V_{DS} is greater than 0.6 V, the g_{ds_dc} of type C always keeps a trend of being less than that of type A and type B. Because g_{ds_dc} is obtained from $\partial I_{DS}/\partial V_{DS}$ and g_{ds} is obtained from Re(Y22) in the S-parameters, g_{ds} and g_{ds_dc} are related, which is consistent with the result of the parameters extraction below. From Eq. (2), a smaller g_{ds} will contribute to improving the f_{max}.

The microwave characteristics of our representative L_g = 80 nm $In_{0.53}Ga_{0.47}As/In_{0.52}Al_{0.48}As$ HEMTs are characterized from 0.1 to 50 GHz, using an Agilent precision network analyzer (PNA) system with off-wafer calibration. Pad parasitics are subtracted from the measured S-parameters using on-wafer OPEN and SHORT pads with identical geometry to the device pads. Figure 5 shows measured (symbols) and small-signal modeled (solid lines) H_{21}, MAG/MSG, and U versus frequency for these devices with the whole small recess offset. Using the de-embedded S-parameters, we build a conventional small-signal model, based on our previous research [17]. The bias condition is at V_{DS} = 0.8 V. And V_{GS} takes the voltage value corresponding to the g_{m_max}. From the de-embedded S-parameters, the values of f_T could be obtain by extrapolating H_{21} with a slope of -20 dB/decade and the values of f_{max} are estimated from the small signal model. It is good that such a combination of f_T = 372 GHz and f_{max} = 394 GHz is demonstrated from the type C device with the whole



(a)



(b)

Fig. 3 Partial DC and RF characteristics of InP HEMT: (a) DC characteristics of the InGaAs/InAlAs HEMTs with the whole small recess offset, and (b) the measured transconductance (g_m) of the devices as a function of I_{DS}, for the value of V_{DS} = 0.8 V (L_g = 80 nm, W_g = 50 μm × 2)

图 3 InP HEMT 的部分直流以及射频特性:(a)具有整个小凹槽偏移的 InGaAs/InAlAs HEMT 的直流特性,以及(b)测量到的器件跨导(gm)作为 IDS 的函数,其中 V_{DS} = 0.8 V(L_g = 80 nm, W_g = 50 μm × 2)

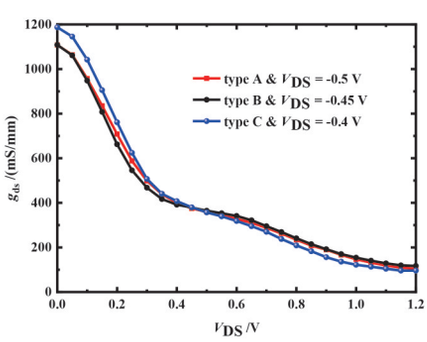
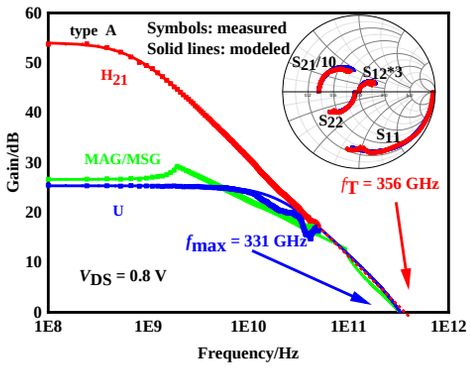


Fig. 4 Dependence of DC drain conductance on applied V_{DS} with different structures

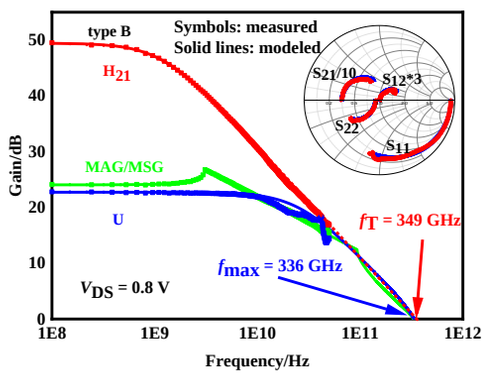
图 4 不同结构的直流漏极电导对所加 V_{DS} 值的变化

small recess toward drain, at a relatively small value of V_{DS} = 0. 8 V and V_{GS} = - 0. 4 V.

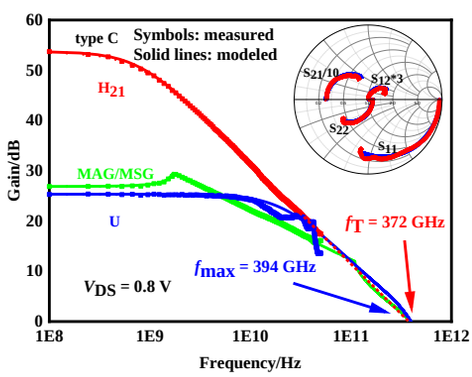
Figure 6 plots the extracted f_T as a function of I_{DS} for these devices at V_{DS} = 0. 8 V, which consists with the g_m



(a)



(b)



(c)

Fig. 5 Measured (symbols) and small-signal modeled (lines) RF gains [$|h_{21}|$, U and maximum available gain (MAG/MSG)] versus frequency with the L_g = 80 nm InGaAs/InAlAs HEMTs . The offsets from large recess center were 0.0 μm (type A), - 0.1 μm (type B), and + 0.1 μm (type C). The bias conditions were near the g_m peak gate voltage and at V_{DS} = 0.8 V

图 5 使用 L_g = 80 nm InGaAs/InAlAs HEMT 测量的和小信号建模 RF 增益 [$|h_{21}|$、U 和最大可用增益 (MAG/MSG)] 与频率的关系。距大凹槽中心的偏移量为 0.0 μm(A 型)、- 0.1 μm(B 型)和 + 0.1 μm(C 型)。偏置条件接近 g_m 峰值栅极电压且 V_{DS} = 0.8 V

against I_{DS} in Fig. 3(b). The type C device have the largest f_T of all f_T - I_{DS} characteristics. At an I_{DS} of approxi-

mately 100 mA/mm which is a typical choice of the bias condition for most of the LNA designs, the type C device displays f_T over 275 GHz.

The f_T and f_{max} can be expressed as:

$$f_T = \frac{g_{mi}}{2\pi\{(C_{gs}+C_{gd})[1+g_{ds}(R_s+R_d)]+C_{gd}g_{mi}(R_s+R_d)\}}, \quad (1)$$

$$f_{max} = \frac{f_T}{\sqrt{4g_{ds}(R_g+R_i+R_s)+\frac{2C_{gd}}{C_{gs}}\left(\frac{C_{gd}}{C_{gs}}+g_{mi}(R_i+R_s)\right)}}. \quad (2)$$

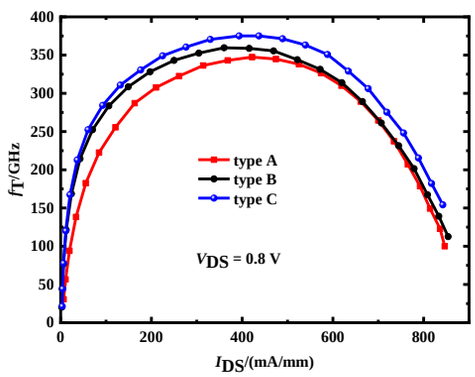


Fig. 6 Extracted f_T against I_{DS} of L_g = 80 nm InGaAs/InAlAs HEMTs at V_{DS} = 0.8 V with different structures

图 6 不同结构的 L_g = 80 nm InGaAs/InAlAs HEMT 在 V_{DS} = 0.8 V下针对IDS提取的f_T

Table 2 shows the small-signal modeling parameters for different structures, including R_S, R_D, g_{mi}, C_{gs}, C_{gd}, and g_{ds}. Compared with type A and type B, type C has the smallest capacitance C_{gs}. This is because the type C device with the whole small recess toward drain results in smaller extrinsic capacitance. At the same time, according to Table 2 and Fig. 4 shows that the type C has the smallest g_{ds}. Although the g_{mi} of type C is the smallest, the parasitic resistance of the three devices is almost the same, and combined with the influence of other parameters, the type C finally obtains the largest f_T. In terms of f_{max}, it depends on the combined infulence of several parameters. The type C device obtains the largest f_{max} due to the small g_{ds} and large f_T. Therefore, it should be finally emphasized that the device with the whole small recess toward drain in a double-recessed gate process could improve the high-frequency characteristics.

3 Conclusion

In summary, we experimentally investigate the impact of the whole small recess offset on the lattice-matched InP-based HEMTs in a double-recessed gate process, where L_g = 80 nm. These devices exhibit the same R_{ON}, and the device with the whole small recess toward source has the largest g_{m_max} due to a smaller R_s. For RF responses of these devices, the device with the whole small recess toward drain achieves an excellent characteristic of f_T = 372 GHz, and f_{max} = 394 GHz. In the following research, the g_m of the device will be further improved to increase the f_T by using a channel with Indium-rich composition.

Table 2 Small-signal model parameters of the L_g=80 nm InGaAs/InAlAs HEMTs at V_{DS}=0.8 V, with different structures.

表 2 不同结构的 L_g=80 nm InGaAs/InAlAs HEMT 在 V_{DS} = 0.8 V时的小信号模型参数

Symbol	Type A	Type B	Type C
V_{GS} [V]	−0.50	−0.45	−0.40
C_{gs} [fF/mm]	418	432	388
C_{gd} [fF/mm]	103	97	99
R_S [Ω·mm]	0.159	0.149	0.169
R_D [Ω·mm]	0.387	0.397	0.377
g_{ds} [mS/mm]	305.5	304.5	240
g_{mi} [mS/mm]	1 513	1 566	1 487
f_{T_meas} [GHz]	356	349	372
f_{max_model} [GHz]	331	336	394

Table 3 Related device performance comparison

表 3 相关器件性能对比

L_g(nm)	$g_{m,max}$(mS/mm)	f_T(GHz)	f_{max}(GHz)	Time	Ref
75	1 950	270	910	2017	[19]
100	1 700	300	700	2022	[20]
70	1 600	310	540	2014	[21]
75	1 331	260	800	2021	[12]

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