第 43 卷第 2 期
2024 年 4 月

红 外 与 毫 米 波 学 报
J. Infrared Millim. Waves

Vol. 43, No. 2
April,2024

文章编号：1001-9014(2024)02-0268-11

DOI：10. 11972/j. issn. 1001-9014. 2024. 02. 017

Low noise ROIC integrated with correlated double sampling with adjustable intervals for hyperspectral applications

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Abstract: Low noise is a key requirement of readout integrated circuit (ROIC) in hyperspectral applications for its low radiation. Correlated double sampling (CDS) is commonly used to suppress noise. In this paper, CDS is improved by adjusting the time interval between the clamp and sample-and-hold (SH), which can filter low-frequency noise flexibly. A 640×512, 15 μm pixel pitch ROIC is designed and fabricated in 180 nm CMOS process. The input stage consists of low-noise capacitive trans-impedance amplifier (CTIA) and CDS with adjustable intervals (AICDS). A timing generator is proposed to extend the CDS reset time from 0 to 270 clock cycles. By extending the reset time to decrease the time interval, the noise electrons are significantly decreased from 39 e^- to 18.3 e^-. The SPECTRE simulation and the experimental results corroborate that the proposed structure AICDS can optimize noise performance of hyperspectral ROIC, thus can be widely used.

Key words: hyperspectral imaging, readout integrated circuit (ROIC), adjustable interval, capacitive trans-impedance amplifier (CTIA), correlated double sampling (CDS), low noise

高光谱应用的带可调复位时间CDS的低噪声红外焦平面读出电路

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摘要：低辐射量的高光谱应用对红外焦平面读出电路(ROIC)提出了低噪声的设计要求。相关双采样(CDS)是常用的减少噪声的结构。本文通过调节钳位和采样保持之间的时间间隔来改进CDS，可灵活消除低频噪声。采用180 nm CMOS工艺设计和制造了640×512规模、15 μm像元中心距的读出电路。输入级集成了低噪声CTIA与本文提出的可调复位时间CDS(AICDS)，所设计的时序产生器使CDS复位时间可以延长0~270个时钟周期。通过延长复位时间减少这个时间间隔，噪声电子数可以由39 e^-减少到18.3 e^-。SPECTRE仿真结果和实验测试结果证实了提出的AICDS结构可以提升高光谱应用读出电路的噪声性能，因此可以广泛应用。

关　键　词：高光谱成像；读出电路；可调时间间隔；CTIA；CDS；低噪声

中图分类号：O47　　**文献标识码**：A

Introduction

Hyperspectral technologies have played a great role in vegetation monitoring, water resource management, geology and land cover[1]. It acquires continuous, narrow-band image data with a high spectral resolution as shown in Fig. 1(a). On one hand, it "captures" most of the subtle changes in the spectrum of a feature[2], which can be used to identify, classify, or quantitatively analyze substances. On the other hand, the light radiation dispersed and focused on hyperspectral infrared focal plane arrays (IRFPA), as presented in Fig. 1(b), is extremely low, resulting in high requirements for low noise. Table 1[3-6] shows the comparison of several hyper-

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Received date: 2023- 08- 23, **revised date**: 2023- 12- 26　　**收稿日期**：2023- 08- 23，**修回日期**：2023- 12- 26

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spectral sensors launched in recent years. The readout noise of readout integrated circuit (ROIC) is one of the key requirements for hyperspectral applications.

Different ROIC input stages are designed depending on the wavelength of infrared radiation. Capacitive transimpedance amplifier (CTIA) can achieve high sensitivity, high linearity, and high injection efficiency[7-8]. It's commonly used for hyperspectral shortwave IRFPA ROIC input stage as shown in Table 1. However, its complex op-amp structure and reset switch not only occupy a large area, but also introduce thermal and KTC noise.

To suppress the low-frequency noise (1/*f* noise) and KTC noise, the correlated double sampling (CDS) has been widely studied in the field of IRFPA ROIC. The principle of CDS is to store 1/f noise on one clock phase and then subtract it from subsequent clock phases. The utilization of CDS in the column pitch or common output stage of IRFPA are reported in Refs. [9-12]. In recent years, to pursue the objective of increasing the frame rate, the CDS is integrated in the pixel as presented in Refs. [13-15]. As for the noise analysis, a method to evaluate the signal and noise of imagers with CTIA-CDS ROICs is developed by Jerris F. Johnson[16], and a cyclostationarity-based analytical model of charge amplification with CDS is proposed in Ref. [17]. The analytical study of CDS KTC noise is presented in Refs. [18-19]. These analyses provided designers with efficient solutions to noise assessment and ROIC optimization.

However, to enhance the CDS noise immunity, the influence of time interval between the clamp and sample-and-hold (SH) processes of CDS needs analysis and verification.

For this purpose, we first expound the noise mechanism of CDS with adjustable intervals (AICDS). Then, the noise power spectral density (PSD) function of combined CTIA-CDS is calculated. Next, to verify the theory, a low-noise pixel circuit is designed, which integrates low-noise CTIA and AICDS controlled by a timing generator. In section 3, the circuit performance is simulated and the noise electron number is calculated. Finally, we draw conclusions.

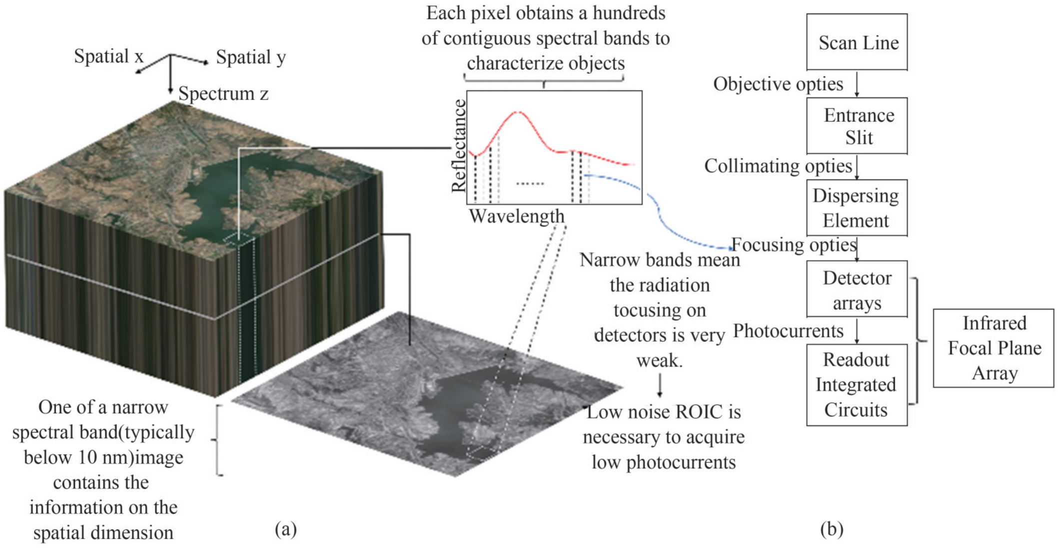

Fig. 1 Acquisition of hyperspectral data: (a) hyperspectral data cube; (b) schematic diagram of a hyperspectral imaging system
图1 高光谱数据获取:(a)高光谱数据立方;(b)高光谱成像系统原理图

Table 1 Comparison of specifications of CRISM, PRISMA, Gaofen−5(GF−5), MAJIS and HyspIRI
表1 CRISM, PRISMA, Gaofen−5(GF−5), MAJIS 和 HyspIRI项目指标比较

Instrument	CRISM	PRISMA	GF−5 AHSI	MAJIS	HyspIRI
Platform name	MRO	PRISMA	SAST3000	JUICE	HyspIRI
country	USA	Italy	China	Europe	USA
Launched year	2005	2018	2018	2022	2023
Spectral bands	−	249	330	−	220
Spectral range/μm	0. 36~3. 9	0. 4~2. 5	0. 4~2. 5	0. 4~5. 7	0. 38~2. 5
Spectral/nm	6. 55	10	5~10	3~7	10
Format	640×480	1 000×256	512×512	1 024×1 024	−
detectors	HgCdTe	HgCdTe	HgCdTe	−	−
Pixel pitch/μm	27	30	30	15	−
ROIC input stage	CTIA	CTIA	CTIA	CTIA	−
Readout noise/e−	<100	<150/<350	60/275	<170	−

1 Noise analysis

This section introduces the noise mechanism of CDS and combined CTIA-CDS as functions of time interval between the clamp and SH.

1.1 Noise mechanism of CDS

The proposed CDS circuit is depicted in Fig. 2(a), which consists of the sample capacitor C_0, reset switch S_2, sample-hold switch S_4, sample-hold capacitor C_{sh} and its reset switch S_3. The processed result is output to the column stage through the source-follower with a switch.

Referring to the operating timing shown in Fig. 2 (b), the equivalent circuits of different steps are shown in Figs. 2 (c), 2(d), and 2(e). The input signal is first sampled on C_0. Secondly, when S_2 is off at t_2, the right plate of C_0 floats, clamping the charge stored in C_0. Lastly, the redistribution of stored charge on C_0 and C_{sh} achieves when S_4 turns on. As a consequence, the signals at different times are subtracted. The specific analysis of noise in a working cycle is as follows.

We consider $v_{n,i}(t)$ as the noise of time t, whose RMS is the square root of the sum of the independent noise powers. At the moment t_2, the noise charge stored on C_0 is:

$$Q_n = C_0 \cdot v_{n,i}(t_2) \quad . \quad (1)$$

At the moment t_4, the noise voltage input to the left pole plate of C_0 becomes $v_n(t_4)$. According to the principle of charge conservation, the charges at the two moments correspond to:

$$C_0 \cdot v_{n,i}(t_2) = C_0 \cdot \left[v_{n,i}(t_4) - v_{n,o}(t) \right] - C_{sh} \cdot v_{n,o}(t). \quad (2)$$

The output noise voltage is:

$$v_{n,o}(t) = \frac{C_0}{C_0 + C_{sh}} \left[v_{n,i}(t_4) - v_{n,i}(t_2) \right] \quad . \quad (3)$$

Applying the Laplace transform to Eq. (3):

$$v_{n,o}(s) = \frac{C_0}{C_0 + C_{sh}} v_{n,i}(s) \cdot \left(1 - e^{-sT_d}\right) \quad . \quad (4)$$

Converting this to the frequency domain, the modulus of the transfer function is:

$$\left| H_D(\omega) \right| = \frac{C_0}{C_0 + C_{sh}} \sqrt{2\left(1 - \cos \omega T_d\right)} = 2\frac{C_0}{C_0 + C_{sh}} \left| \sin(\ \omega T_d/2) \right| \quad . \quad (5)$$

The red curve in Fig. 3 (a) is the amplitude-frequency plot of the flicker noise, represented as:

$$\overline{V_n} = \sqrt{\frac{K}{C_{ox}WL} \cdot \frac{1}{f}} \quad , \quad (6)$$

where K is a quantity related to the manufacturing process, C_{ox} is the gate-oxide capacitance per unit area and WL is the channel area. Here, we assume $\sqrt{\frac{K}{C_{ox}WL}} =$ 1nV to simplify calculations.

The transfer function of two different CDS is shown in Fig. 3 (b), one is $\sin(\ \omega T_d/2)$, the other is $\sin(\ \omega\left(2T_d\right)/2)$. Here, we ignore the influence of capacitance and set $T_d = 0.5\ \mu s$. The input noise is reshaped through CDS to the output noise presented in Fig. 3(c). By reducing T_d to lengthen the transfer function's period, it can be determined that the noise power in the low-frequency section may be decreased.

1.2 Output noise PSD of combined CTIA-CDS circuit

The subtraction step of CDS can be considered as a delay-subtractor [20] as analyzed in the previous section. The CTIA, which is a switched-capacitor integrator, is equal to a first-order low-pass filter. The unit circuit structure model is shown in Fig. 4.

The noise power density of first-order low-pass filter:

$$S_0(\omega) = \frac{S_w}{1 + \left(\omega\tau_0\right)^2} \quad , \quad (7)$$

where the time constant $\tau_0 = RC$.

The noise power spectrum after the delayed subtractor is:

$$S_D(\omega) = S_0(\omega) \left| H_D(\omega) \right|^2 \quad . \quad (8)$$

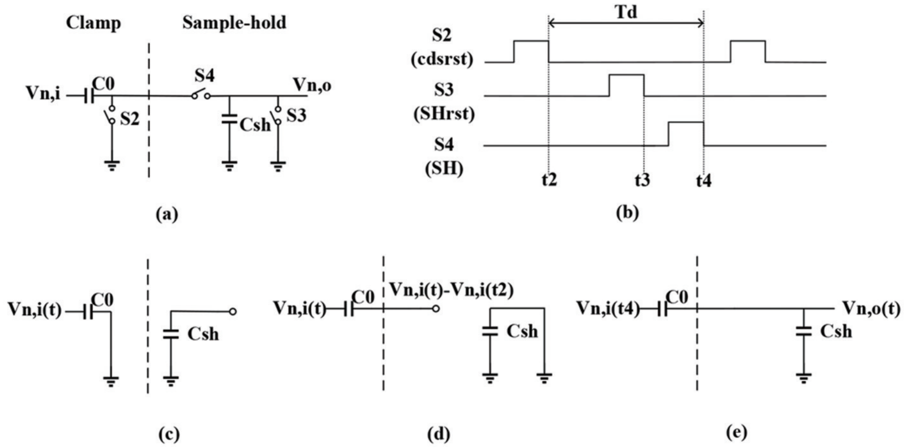

Fig. 2 Correlated double sampling: (a) structure of CDS; (b) timing diagram of CDS, equivalent circuits: (c) reset of C_0 step at t_2; (d) reset of C_{sh} and clamp step at t_3; (e) sample-hold step at t_4

图2 相关双采样：(a)CDS结构；(b)CDS工作时序，等效电路；(c)在t_2时刻C_0复位；(d)在t_3时刻C_{sh}复位以及钳位；(e)在t_4时刻采样保持

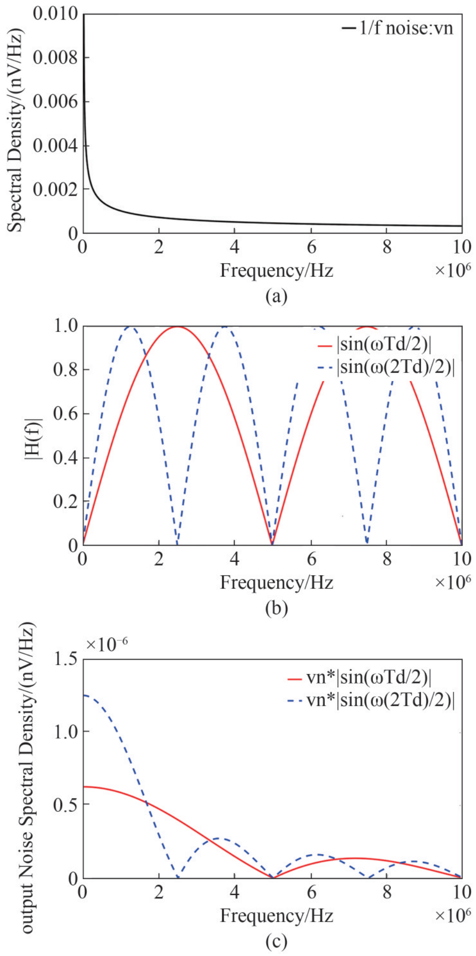

Fig. 3 1/*f* Noise Spectral Density reshaped by CDS with different T_d: (a) the spectral density of 1/*f* noise; (b) comparison of two CDS transfer functions with different T_d; (c) comparison of two output noise spectral density functions with different T_d

图3 1/*f*噪声的功率谱经过不同T_d的CDS重构:(a)1/*f*噪声功率谱;(b)两种不同T_d的CDS传输函数;(c)经过两种不同T_d的CDS重构的输出噪声功率谱

It can be seen from Eqs. (5) and (8) that reducing T_d can decrease the noise power in the low-frequency section.

2 Proposed ROIC input stage

To verify the analysis above, a new ROIC input stage composed of low noise CTIA and AICDS is designed.

2.1 Combined CTIA-AICDS circuit

The combined CTIA-AICDS circuit proposed is shown in Fig. 5. The detector is directly connected to CTIA, which contains a reset switch S_1 and the feedback capacitor C_{int}. Then, the AICDS receives the integral signal. Finally, the modified signal is transmitted through SF to the column stage.

The conventional design uses a differential pair as the operational amplifier, where the MOS occupies nearly twice the area. Its input reference thermal noise voltage is :

$$\overline{V_{n,in}^2} = 8kT\left(\frac{2}{3g_{m1}} + \frac{2g_{m3}}{3g_{m1}^2}\right) . \quad (9)$$

This design uses a cascode type operational amplifier with an input reference thermal noise voltage of:

$$\overline{V_{n,in}^2} = 4kT\left(\frac{2}{3g_{m1}} + \frac{2g_{m3}}{3g_{m1}^2}\right) . \quad (10)$$

It is close to half of the differential pair op-amp. This noise cannot be eliminated by the subsequent CDS structure [21], but will be multiplied through two sampling process, having a large impact on the circuit noise performance. Therefore, the cascode op-amp has benefits on noise reduction and area saving.

Considering to further reduce the noise of CTIA, the following guidelines must be adhered to in the design.

The operating current I_D of the cascode must be low. The small operating current ensures a smaller power consumption, reducing the detector image interference caused by the heat of the pixel circuit. I_D is determined by V_{bias}, which is provided through the current mirror in the bias circuit. The current mirror of the selectable channel generates I_D around 100 nA in this application.

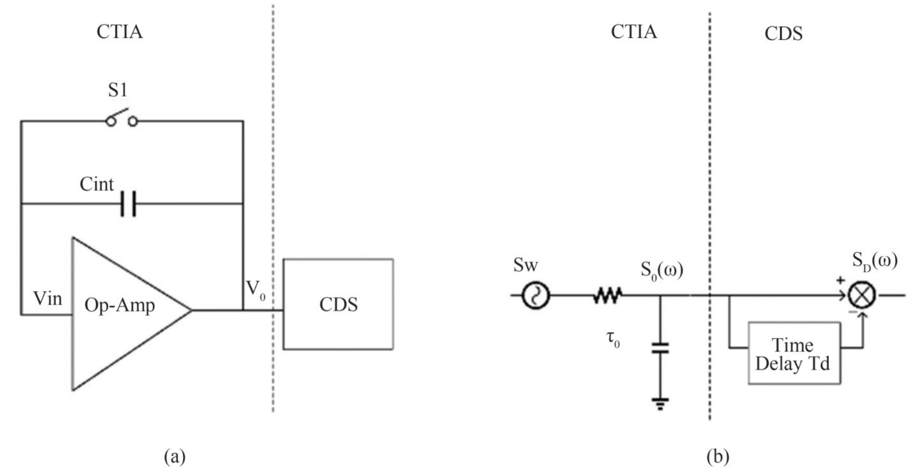

Fig. 4 Structure of combined CTIA-CDS ROIC: (a) the schematic structure; (b) equivalent model structure

图4 组合CTIA-CDS的读出电路结构:(a)电路结构;(b)等效模型

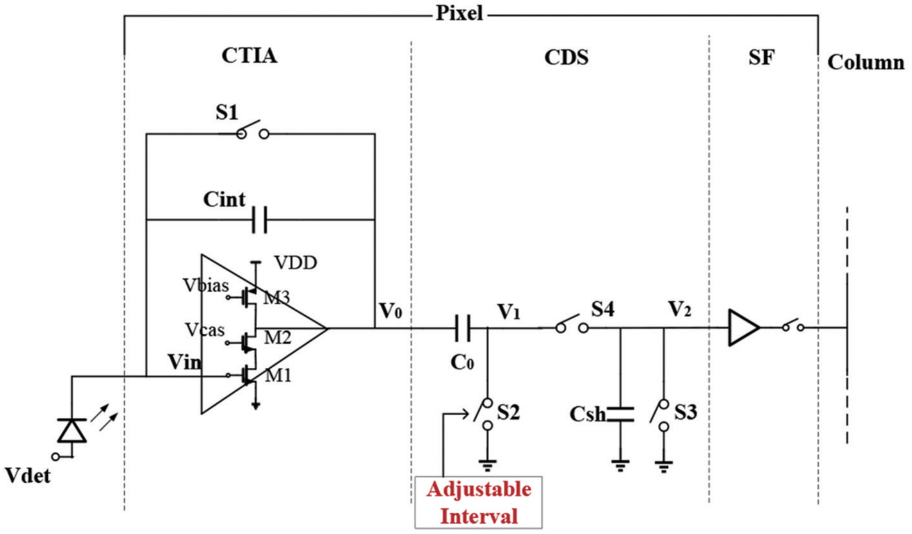

Fig. 5 Combined CTIA-AICDS ROIC
图5 组合CTIA-AICDS读出电路

$\frac{W}{L}$ of input transistor M_1 must be large whereas $\frac{W}{L}$ of load transistor M_3 must be small.

These two conditions make M_1 work in the sub-threshold region, where the leakage current of M_1 is:

$$I_D = I_0 exp\frac{V_{GS}}{\zeta V_T} \quad , \qquad (11)$$

where $\zeta > 1$ is a non-ideal factor and $V_T = kT/q$.

At this point, I_D is exponentially related to V_{GS} and the trans-conductance of MOS device M_1 is:

$$g_{m1} = \frac{dI_D}{dV_{GS}} = \frac{1}{\zeta V_T}I_D \quad . \qquad (12)$$

The gain of the operational amplifier is

$$A_V = -g_{m1}\left\{\left[\left(1 + g_{m2}r_{o2}\right)r_{o1} + r_{o2}\right] \| \, r_{o3}\right\} \quad . \qquad (13)$$

It guarantees a large gain of M_1 in the subthreshold region as we can conclude from Eqs. (12) and (13).

The operating timing of the pixel circuit is shown in Fig. 6. Adjusting the additional CDS reset time T_r can regulate T_d. At the beginning of each frame, S_1 and S_2 turn on to reset C_{int} and C_0. After enough reset time, S_1 is disconnected to start the integration process. Due to the

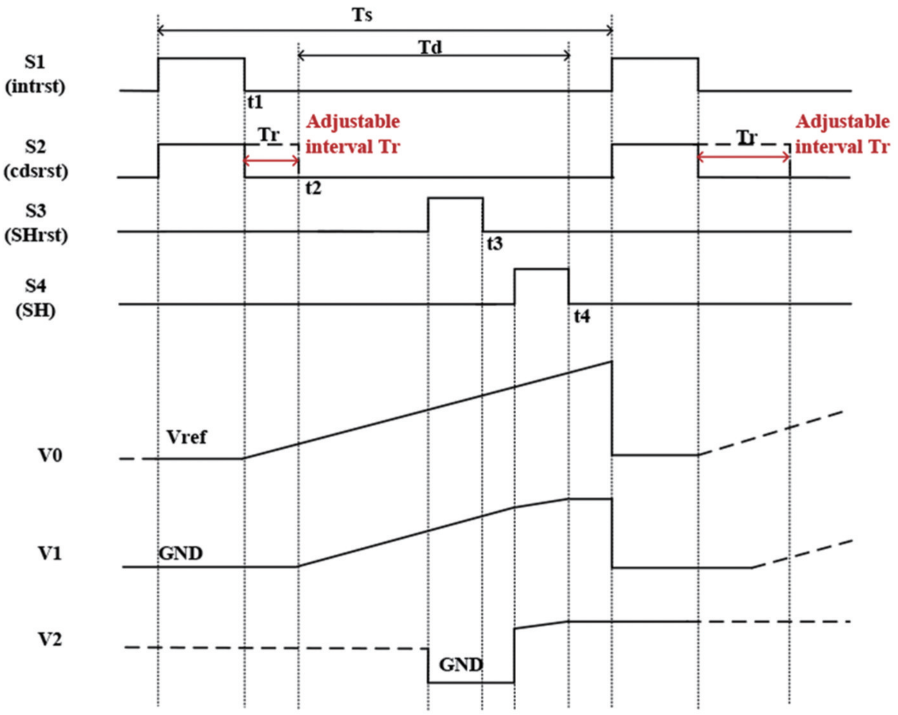

Fig. 6 Timing diagram and node voltage of the proposed ROIC pixel
图6 提出的读出电路像元的时序与节点电压

voltage regulation characteristic of the op-amp, V_{in} remains unchanged and V_0 is integrated as photocurrent is injected into the feedback capacitor. Subsequently, the transmission to CDS of V_0 operates as described in section 2.

2.2 Timing generator of AICDS

The proposed timing generator can adjust the additional CDS reset time T_r relative to integration-reset time t_1 as exhibited in Fig. 6. The CTIA integral reset signal *intrst* generates two pulse signals φ_0 and φ_1 to mark its rising and falling edges. As seen in Fig. 7, the division, counter, comparator, and latch make up the CDS timing control mechanism. It operates as follows.

a. The high-frequency master clock CLK is first divided into a clock, whose cycle period is determined by the required minimum time step.

b. The counter generates 4 bits Gray-code from the divided clock.

c. Comparing Gray-codes with control bits *TR*[3:0], it generates a pulse signal φ_c to determine the falling edge of T_r when digital bits equal.

d. φ_1 and φ_c determine the operational time of the counter.

e. φ_0 and φ_c are injected to the latch to generate *cdsrst*.

A time regulation step of 18 clock cycles is achieved by dividing the frequency with 9 DFFs. With 4 digital bits, a CDS reset time regulation ranging from 0 μs to 27 μs can be achieved for the master frequency CLK of 10 MHz, as shown in Table 2.

Table 2 CDS reset time regulation
表2 CDS复位时间调节

TR[3:0]	Clock cycles
0000	0
0001	18
0010	36
…	…
1111	270

3 Circuit performance and noise simulation

In order to confirm the performance of circuit design, we have simulated the schematic using SPECTRE of Cadence. This circuit is designed in standard 180 nm CMOS process with 3.3 V supply voltage. Integral capacitance $C_{int} = 4\,\text{fF}$, CDS sample capacitor $C_0 = 200\,\text{fF}$ and SH capacitor $C_{SH} = 20\,\text{fF}$.

3.1 Circuit performance simulation

The performance of CTIA amplifier is simulated and shown in Table 3. Sweeping the injection photocurrent from 200 pA to 900 pA, the output waveform of V_0 and V_2 is presented in Fig. 8.

Table 3 The performance of CTIA amplifier
表3 CTIA放大器工作性能

Amplifier parameter	
gain	59.6 dB
Phase margin/°	60
Bandwidth/Hz	8M
Swing/V	2.23(1–3.23)
pixel pitch/μm	15
DC current/nA	68~100

Figure 9 shows the simulation results for the CDS reset time regulation. Setting *TCDSRST*[3:0] = 1001, the simulation waveforms demonstrate that T_r is 9 μs, which is consistent with intended specification.

3.2 Noise simulation

The common simulation method is to sum the noise of each separate cell. Since the CTIA reset noise and CDS of this circuit are correlated, the traditional simulation method cannot accurately reflect the impact of the interval on the noise. This design adopts transient noise simulation, which can accurately reflect the noise magnitude during the hold phase.

We evaluate the equivalent noise charge (ENC) of input node to verify the noise performance of AICDS.

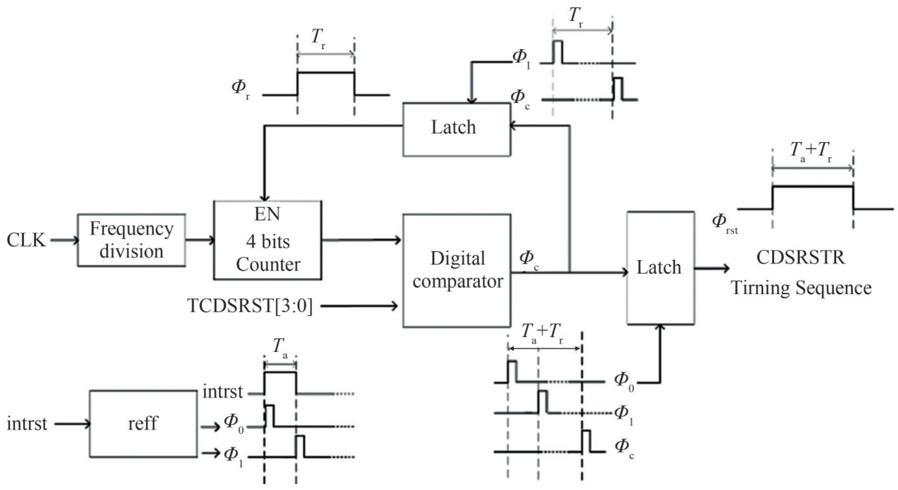

Fig. 7 The proposed timing generator of AICDS
图7 提出的AICDS的时序产生器

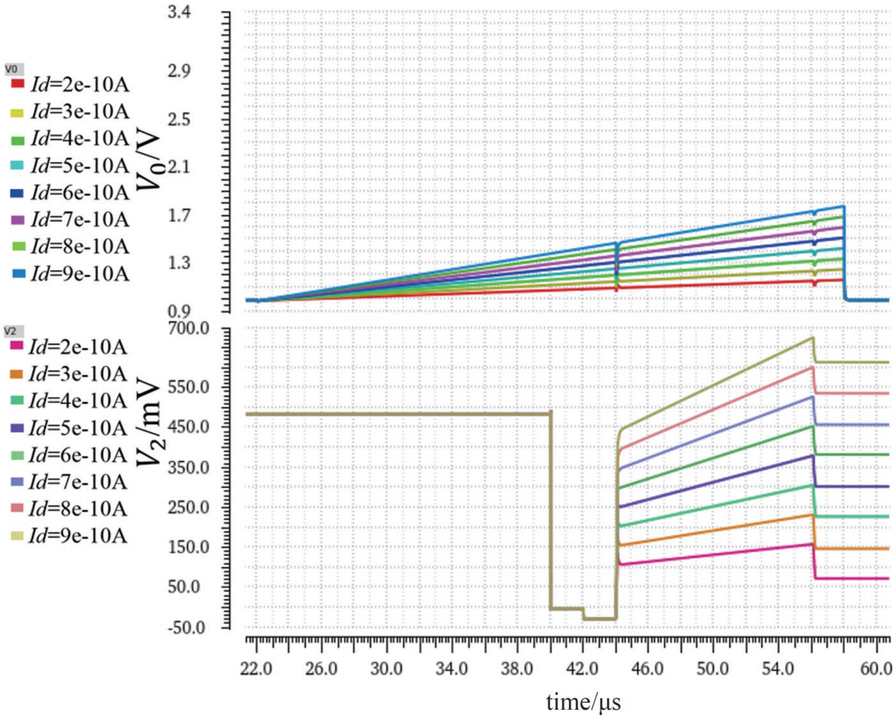

Fig. 8 Integration and dynamic simulation
图8 积分动态仿真

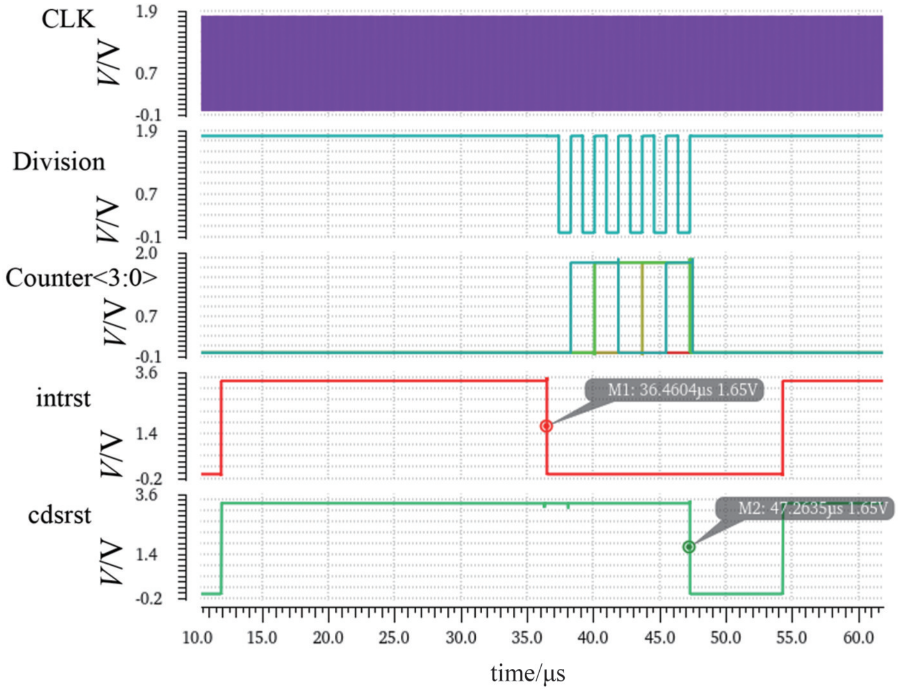

Fig. 9 Time sequence transient simulation
图9 时序瞬态仿真

The ENC μ_n is described as follows:

$$\mu_n = \frac{V_n}{eG} \quad , \quad (14)$$

where V_n is the noise voltage of output node and electron charge $e = 1.6 \times 10^{-19}$ C. The conversion gain G is presented as:

$$G = \frac{V_2}{\mu_e} \quad , \quad (15)$$

where V_2 is the output voltage and μ_e is the electrons injected into the ROIC.

In this design, μ_e is integrated from t_2 to t_4 as shown in Fig. 6.

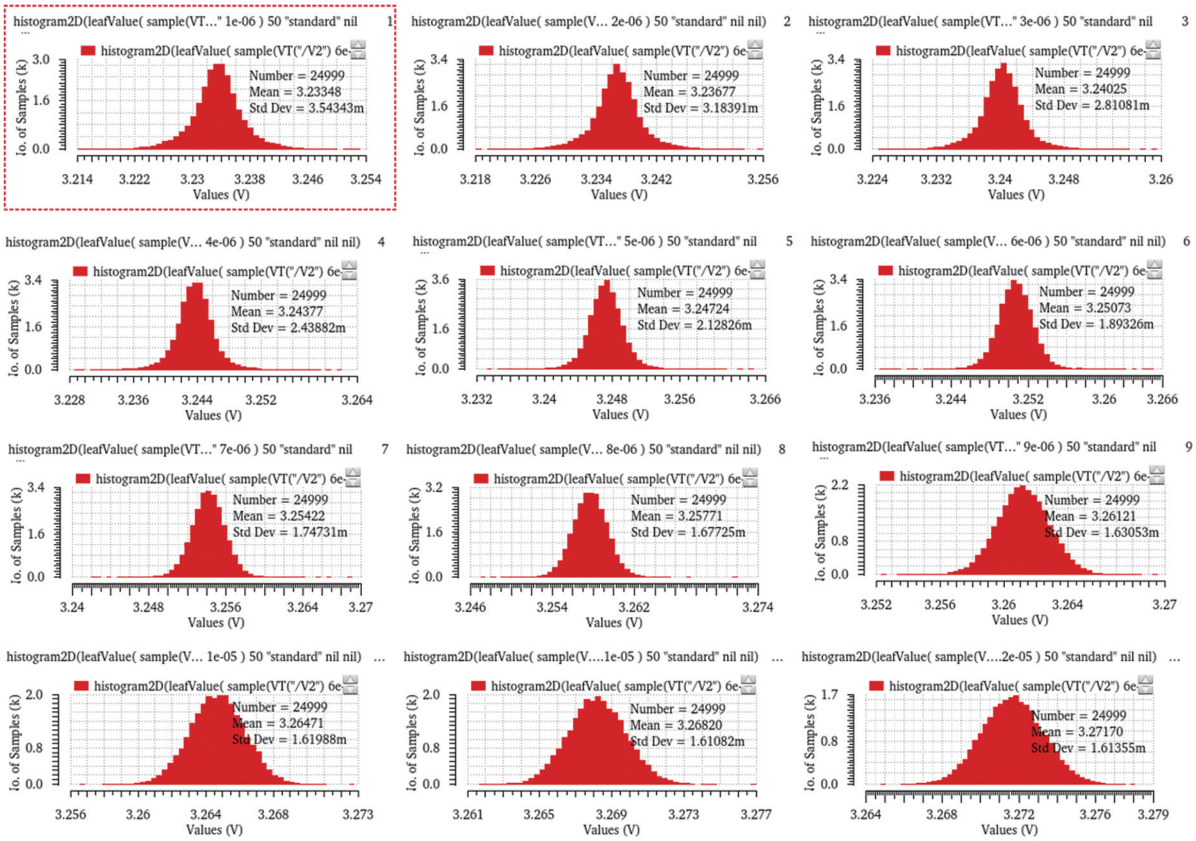

Fig. 10 The histogram of V_2 under different settings of T_r
图10 不同T_r下V_2的直方图

$$\mu_e = I_{det}T_d = I_{det}\left(T_{int} - T_r\right) \quad , \quad (16)$$

where T_{int} = 34 μs.

As for V_2, we can calculate it from Eq. (3).

$$V_2 = \frac{C_0}{C_0 + C_{sh}}\frac{I_{det}T_d}{C_{int}} \quad . \quad (17)$$

Then the conversion gain G is:

$$G = \frac{C_0}{C_0 + C_{sh}}\cdot\frac{1}{C_{int}} \quad . \quad (18)$$

For the case of C_{det} = 40 fF and photocurrent I_{det} = 20 pA, 24999 transient noise simulations are performed and sampled.

For the results, the histogram of output voltage V_2 under different settings of T_r is shown in Fig. 10. The results are finally brought into Eq. (14) to calculate the number of noise electrons.

Noise electrons under different settings of T_r are shown in Fig. 11. The noise electron number of readout circuit ranges from 48.72 to 22.15, with T_r varying from 1 μs to 11 μs. After T_r = 11 μs, the noise is stable at about 22 e^- which is mainly decided by the post-stages.

As T_r increases, the SNR can reach 42.98 dB at T_r = 8 μs. However, after that, the signal quantity declines with decreased T_d whereas the noise stays constant, resulting in attenuation of SNR. The simulation results show that extending T_r, in other words, decreasing T_d, can suppress the noise of combined CTIA-CDS ROIC.

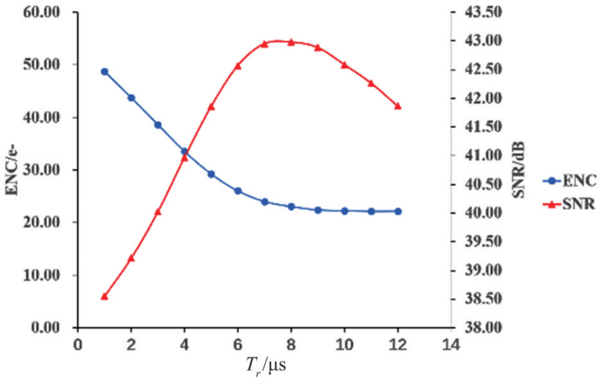

Fig. 11 ENC and SNR vary with T_r
图11 等效噪声电荷和信噪比随T_r的变化

4 Experimental results

The full system is designed and fabricated in TSMC 0.18 μm CMOS technology. The fabricated chip is shown in Fig. 12, annotated with the floorplan. It consists of 640×512 array of 15 μm×15 μm pixel area. To meet the requirement of low noise, the pixel array is located at the center of the chip, while separated analog and digital blocks are placed at the edge.

The platform designed to test the system is shown in Fig. 13[22]. LVDS module can generate the working time sequence and collect the output signal produced by the chip. The LabView-based test platform can control volt-

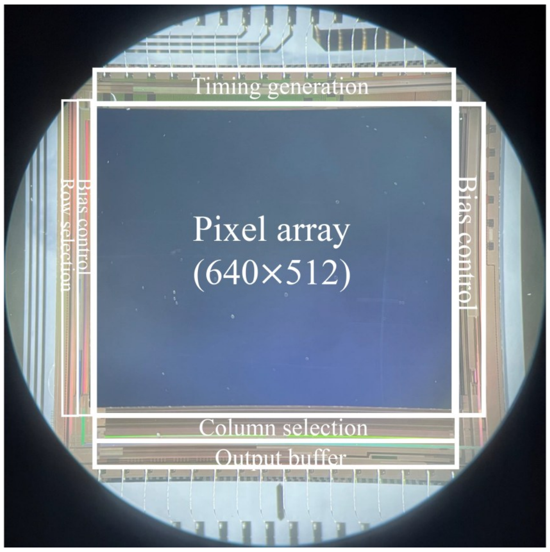

Fig. 12 Layout and floorplan of the fabricated chip
图12 芯片版图和平面布局

age, clock, and waveform. In addition, the acquired readout signal of the pixel array can be displayed as a grayscale map.

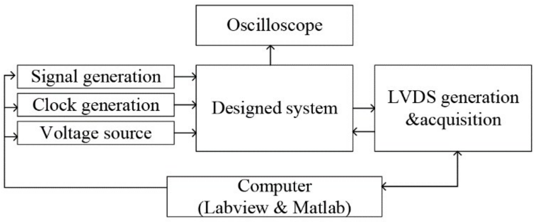

Fig. 13 Schematic diagram of experimental platform
图13 实验测试平台原理图

To compare the noise performance of input stage with and without CDS, we designed a test schematic to turn off the CDS function as shown in Fig. 14 (a). The timing diagram is presented in Fig. 14 (b), where we can see S_2 is invariably off, while S_5 closes to be constantly controlled by a digital bit. As shown in Figs. 15 (a) and 15(b), we get the grayscale map over 640×512 pixel array with CDS off and on. Intuitively, the uniformity with CDS on is far better than that with CDS off, which demonstrates that the noise can be suppressed by CDS. A closer look can be taken by acquiring partial 16×16 array to check the noise distribution, which is shown in Figs. 15 (c) and 15(d). The noise with CDS on is far lower and much flatter than that with CDS off.

The clock frequency is set at 500 kHz, which means the adjustment step is 36 μs. The additional CDS reset time T_r is adjusted and settled in condition of T_{int} = 360 μs and T_{int} = 640 μs. We measure the influence of T_r on the noise through the ratio of $\gamma = T_r/T_{int}$ as presented in Fig. 16, where we can conclude that:

a. The noise electron is up to 18.3 e^- optimally by adjusting T_r, while the noise number is 39 in the case of turning off CDS. It shows an attenuation of 52%;

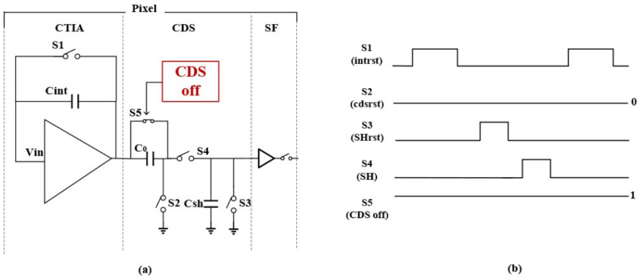

Fig. 14 Structure of CDS test: (a) the schematic structure; (b) timing diagram
图14 CDS测试结构:(a)电路结构;(b)时序

b. With CDS on, the noise has a tendency of decreasing with the increment of T_r, whose slope is -24 μV.

5 Conclusion

In this paper, CDS with adjustable intervals has been proposed as a new technology to improve the noise performance of ROIC. It has been analyzed that decreasing the time interval between the clamp and SH can reduce the pre-stage noise. The feasibility of the technique is proved in a combined CTIA-AICDS controlled by a timing generator in 180 nm CMOS process. 24999 transient noise simulations demonstrate that by adjusting the interval, the ENC of input stage attenuates by 54%, and SNR is enhanced by 5 dB. The experimental test results verify that the proposed structure can suppress the noise by 52% than CDS off and reduce the noise with a slope of -24 μV. It can be broadly used in Hyperspectral applications of low background radiation.

Acknowledgment

The authors would like to thank GENG Peng-Fei and SHAO Jia-Qi for language help and useful discussions.

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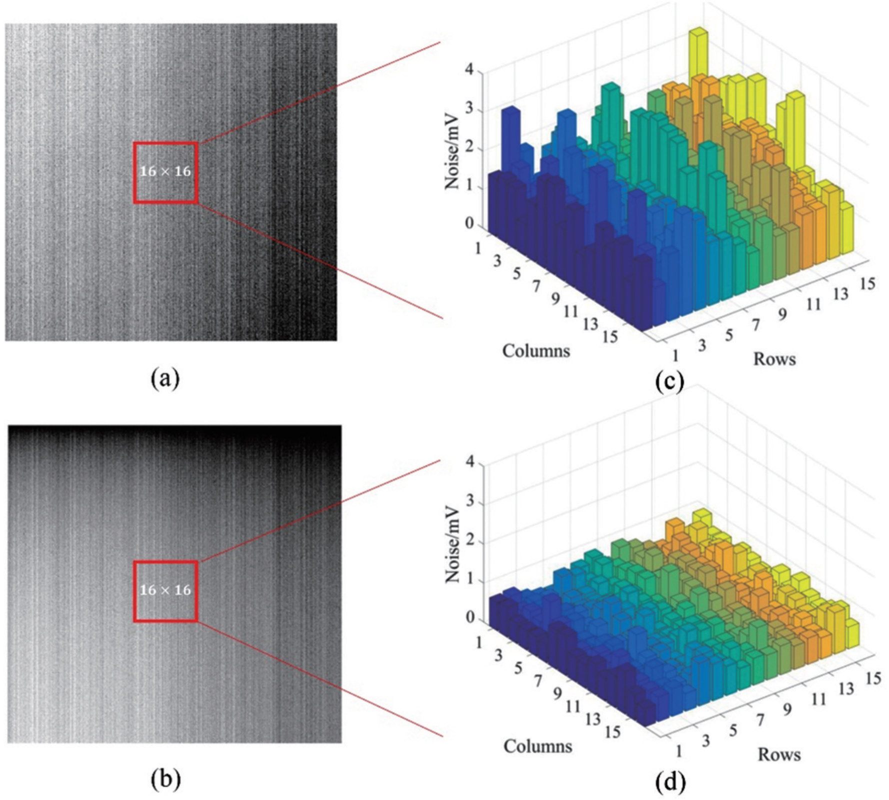

Fig. 15 The output voltage acquisition：(a) the grayscale map over 640×512 array when CDS-off；(b) the grayscale map over 640×512 array when CDS-on, the output noise acquisition；(c) the histogram of 16×16 segment when CDS-off；(d) the histogram of 16×16 segment when CDS-on

图 15 输出电压采集结果：(a)CDS功能关闭时640×512阵列的灰度图；(b)CDS功能开启时640×512阵列的灰度图，输出噪声采集结果；(c)CDS功能关闭时其中16×16阵列的柱状图；(d)CDS功能开启时其中16×16阵列的柱状图

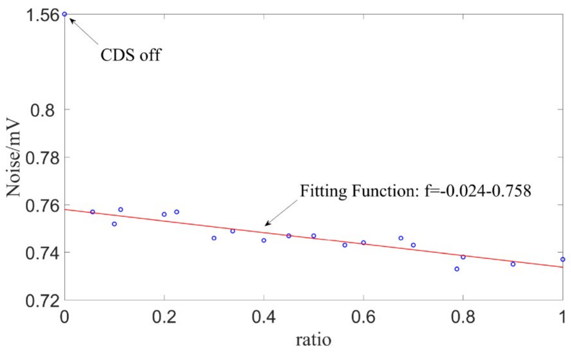

Fig. 16 The output noise voltage in condition of (a) CDS off and (b) varying ratio γ when CDS turns on

图 16 (a)CDS关闭与(b)CDS开启下调节比例γ两种情况下的输出噪声电压

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