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G-band quad-port balanced multiplier with 111.27 mW continuous-wave output power

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Abstract: A 215~230 GHz Schottky varactor-based frequency doubler utilizing novel four-port balanced configuration has been developed with improved conversion efficiency and power-handling capability. The proposed doubler, featuring doubled number of anodes in conventional balanced ones, could inhibit the odd- and fourth-order harmonics. Thus, better conversion efficiency and doubled power handling capability could be achieved. At room temperature, the fabricated doubler exhibits a ~39.5% peak conversion efficiency (@218 GHz) for an input power of 196~340 mW, which is proved to be a perfect solution for the generation of high power terahertz waves even at higher frequencies.

Key words: balanced doubler, terahertz wave generation, nonlinear, Schottky diode
PACS: 85.30.Hi, 85.30.Kk, 84.30.Vn, 07.57.Hm

连续波输出功率111.27 mW的G波段四端口平衡式倍频器

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摘要:利用新颖的四端口平衡式二倍频原型,开发了215~230 GHz频段的肖特基变容管倍频器,并具备更加优秀的变频效率和功率容量。同时,所提出的倍频架构能够实现奇次谐波和四次谐波的本征抑制,并且其中采用的二极管管结数量相对于传统平衡倍频结构提升了两倍。因此,这种四端口倍频电路可以实现更好的转换效率和双倍的功率处理能力。在室温下,当输入功率为196~340 mW时,该倍频器具有约39.5%的峰值转换效率(@218 GHz),即使在较高的频率下,该倍频器也被证明是高功率太赫兹波信号产生的理想解决方案。

关 键 词:平衡式二倍频;太赫兹信号产生;非线性;肖特基二极管
中图分类号:TN771　　**文献标识码**:A

Introduction

As the critical solid-state sources in several terahertz applications including imaging, wireless communication and radio astronomy[1-3], Schottky diode-based multipliers have been well-developed over the past years. The coming generation of heterodyne array instruments toward frequencies up to 1 THz directly put forward the requirement of higher local oscillator (LO) output power levels especially in critical pumping frequencies to enable related array receivers[4]. Generally, terahertz solid-state sources rely on several individual multipliers in cascade to achieve enough frequency multiplication, in which the efficiency and output power of each stage directly affect the overall performances. For example, the generation of powers at frequencies up to 670 GHz put forward the urgent requirements on sufficient powers over 200~230 GHz range. Thus, improving the power-handling capabilities as well as conversion efficiencies have been a research focus of diode-based multipliers.

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At the moment, the classical balanced doublers[5-6] proposed by Erickson are preferred for the inherent suppression on odd-order harmonics, whose power handling-capabilities are restricted by the limited diode numbers. As a result, the power-combined techniques become one of the most preferred methods improving the overall power-handling capabilities, at the expense of non-negligible decreases in conversion efficiency [7-9]. And the overall efficiency of power-combined doublers would also degrade with the increase of multiplying channels, which restricts the highest achievable output power. Thus, developing novel doubling configurations, which can increase the circuit power-handling capabilities with improved conversion efficiencies, becomes an attractive solution for high power terahertz multiplying sources.

In this letter, a novel four-port balanced doubler prototype presented in our recent work [10] has been introduced to break through the achievable output power in G-band (as shown in Fig. 1), which features doubled power-handling capability with improved conversion efficiency than the conventional ones. Accordingly, a hybrid balanced doubler operating up to 230 GHz has been designed and implemented based on improved electro-thermal diode modelling techniques. The proposed circuit could not only inhibit the odd- and fourth-order harmonics, but also can increase the power capacity by a factor of two due to the doubled diode numbers. Namely, the output power could be improved by a factor of two with better conversion efficiency. Moreover, this on-chip concept could drastically reduce its sensitivity to the accuracy of manually assembling, especially at higher terahertz frequencies.

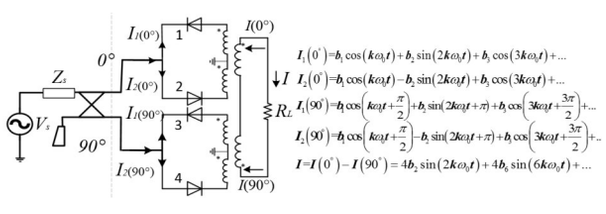

Fig. 1 Diagram of the four-port balanced doubler prototype and related harmonic currents [10]
图1 四端口平衡倍频原型及相关谐波电流图

1 Configuration and design

According to the ideal prototype in Fig. 1, the waveguide-based balanced four-port topology could be established, as shown in Fig. 2. This structure is similar but totally different from the circuit in Ref. [11], which could provide additional suppression on the adjacent 4th-order harmonics. The developed circuit employs two pairs of discrete diodes driven in phase quadrature by a hybrid coupler, which are soldered on a 50 μm-thick quartz substrate. Thus, each diode pair in anti-series would be excited under different polarities, resulting in different harmonic currents $I_1(\theta)$ and $I_2(\theta)$ (where θ could be 0° and 90°). As shown in Fig. 2, the output current of each diode pair should be the differential of $I_1(\theta)$ and $I_2(\theta)$, which inherently suppress the odd-order harmonics. Furthermore, the final current would also be the differential output of ($I(0°)$ and $I(90°)$), which inhibits the 2N-order (where N is even number) harmonics. The generated harmonic currents are illustrated in Fig. 2, while the related expressions are shown in Fig. 1.

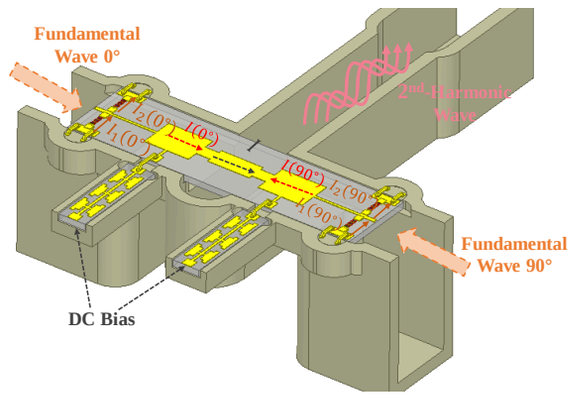

Fig. 2 Diagram of the face-to-face balanced tripler architecture
图2 对差分平衡式三倍频电路图

To implement the 220 GHz balanced doubler, four discrete GaAs Schottky diodes have been utilized. As shown in Fig. 3, the utilized diodes feature 300-nm N-GaAs layer and 2.5-μm N+ GaAs layer with a doping concentration of 2×10^{17} cm^{-3} and 5×10^{18} cm^{-3}, respectively. To increase the overall power capacity, each diode is composed of three anodes (each with a diameter of 7 μm) in series featuring a dimension of 230 μm×48 μm×30μm.

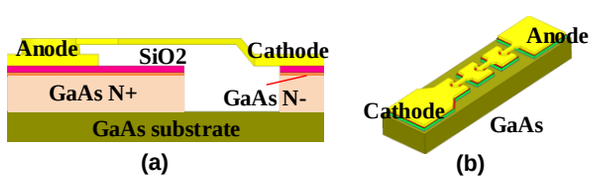

Fig. 3 (a) Corss section view of the diode junction; (b) 3D-view of the diode
图3 (a)二极管结区的剖面图;(b)二极管三维示意图

In addition, self-heating and current saturation effects under high operation power must be taken into consideration for better simulation accuracy. A self-consistent electro-thermal model is developed to optimize high efficiency circuits from both the electrical and thermal perspectives. The electrical model of the diode, as well as the self-heating effects characterization, are similar to that in Ref. [12]. Differently, the temperature-dependent junction parameters, including saturation current (I_s), ideality factor (η) and series resistance (R_s), are extracted based on temperature-controlled *I-V* measurements rather than simply approximating with theoretical expressions [8]. Utilizing the same test setup in Ref. [9], the measured *I-V* and *C-V* curve of a 3-anode diode under different temperature levels are illustrated in Fig. 4(a) and (b).

On the one hand, the constant zero-bias junction ca-

pacitance is extracted to be 32 fF with C-V curves, featuring low dependency on junction temperatures. On the other hand, the temperature-dependent saturation current (I_s), ideality factor (η) and series resistance (R_s) could be calculated and extracted based on the temperature-controlled *I-V* curves, utilizing the extraction method discussed in our previous work[9]. And the extracted and fitted temperature-dependent parameters are illustrated in Fig. 5(a) and (b).

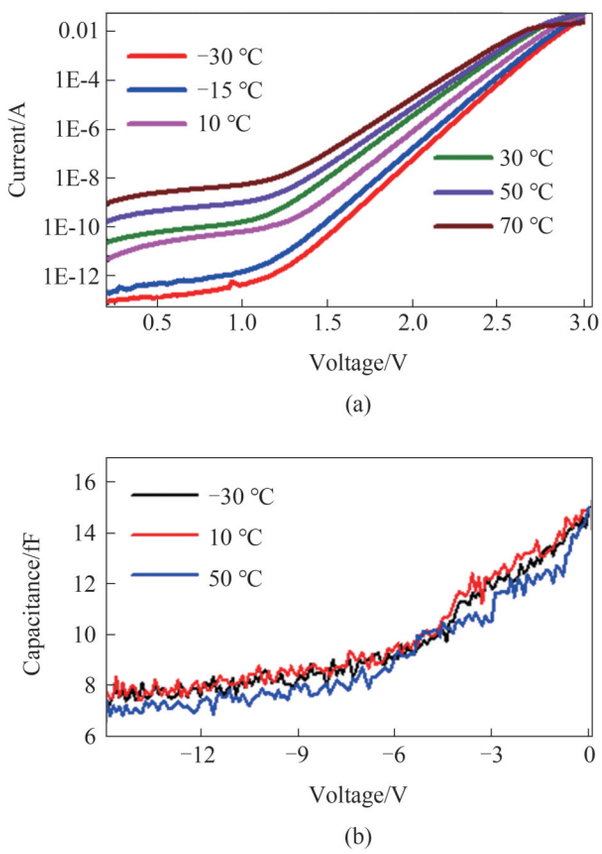

Fig. 4　Measured diode *I-V* curves (a) and *C-V* curves (b) at different temperature levels.
图4　在不同温度梯度条件下测试的二极管*I-V*曲线(a)和*C-V*曲线族

Thermal resistance matrix of the multiplier circuit also need to be extracted to establish the dependency between thermal and electrical domain (shown in Fig. 6(a)). Using the method in Ref. [12], the 3-order thermal resistance matrix (R_{th}) could be calculated and fitted (in Fig. 6(b)). In this way, response of temperatures on dissipated power in different anodes could be predicted, as shown in Fig. 6(c). Furthermore, an accurate self-consistent electro-thermal model could be implemented using the symbolically defined device (SDD) component available in the advanced design system (ADS).

The optimum embedding impedances presented to different harmonics at each junction is determined for maximum conversion efficiency with an input power of 25.5 dBm. With the consideration of self-heating effect, the whole circuit is analyzed and optimized with the cooperation of electro-magnetic and harmonic balance simulations. This process is iterated, modifying the circuit geometry each time, to push the impedances presented to each anode close to their optimum values. Fig. 7(a) illustrated the final geometry of the four-port balanced doubler, which could provide good impedance matching for different harmonics (shown in Fig. 7(b)). The whole circuit comprises an orthogonal coupler, a pair of doubler cells and a three-port E-plane differential probe. The diode chips are assembled on the quartz circuit using the flip-chip technique. And a pair of DC-bias circuits are connected together for better balance. And another circuit has been optimized (Fig. 7(c)), which also provides great impedance matching (Fig. 7(b)), based on the Erickson-style balanced topology with the same diode for better comparison.

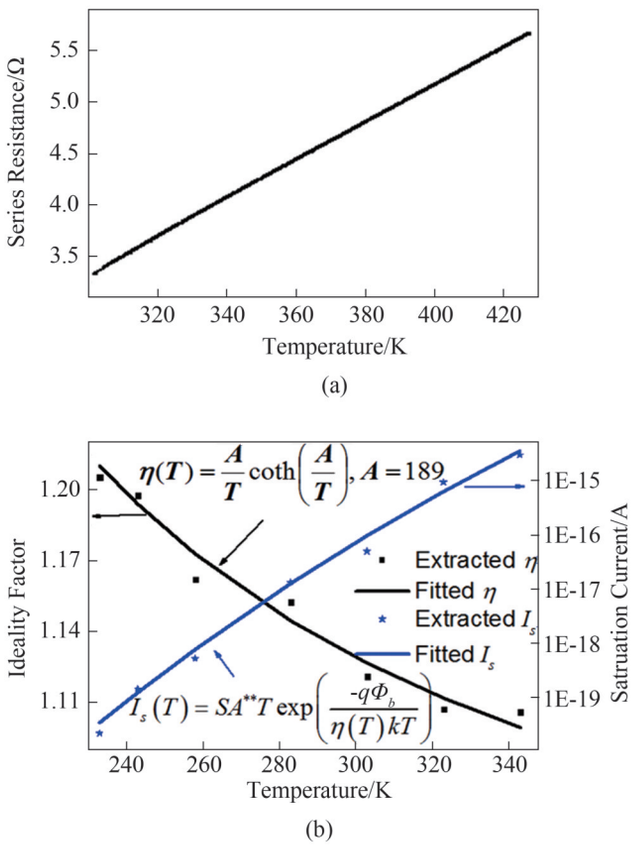

Fig. 5　(a)The extracted&fitted temperature-dependent series resistance; (b)ideality factor and saturation current
图5　(a)提取和拟合的随温度变化的串联电阻;(b)理想因子和饱和电流曲线

2　Fabrication and measurement

The fabricated 220 GHz balanced doubler is shown in Fig. 5. A 105~115 GHz multiplier with an output power tuned to 150~170 mW has been used to pump the traditional circuit in Fig. 7(c). As shown in Fig. 8(a), a peak power of 44 mW at 222.4 GHz is achieved with related efficiency of 30%, while the peak efficiency is 31.2% at 225 GHz. As the doubler in Fig. 7(a) was designed based on the four-port prototype, it is expected to

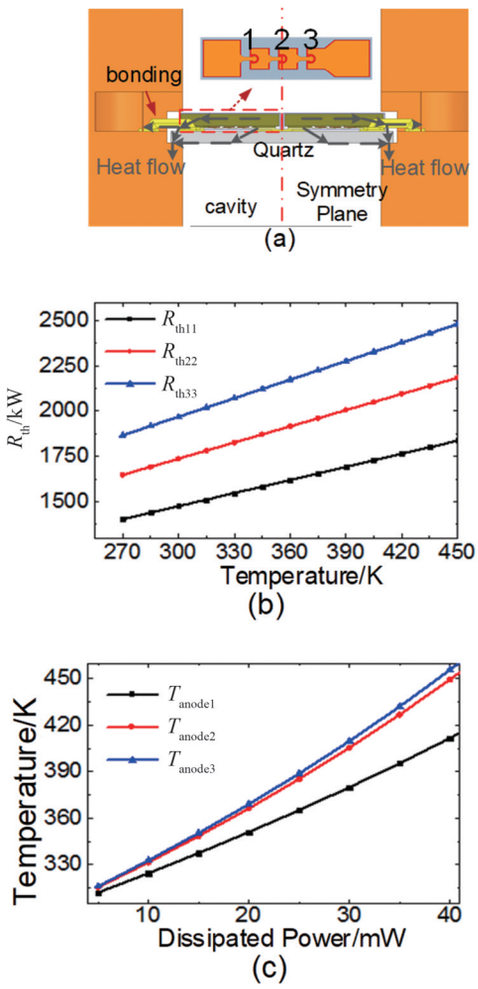

Fig. 6 (a) Cross section views diodes mounted in the cavity; (b) The main diagonal terms in the calculated thermal resistance matrix; (c) Predicted anode temperatures as a function of dissipated power

图6 (a) 倍频电路热仿真截面示意图;(b) 热阻抗矩阵主要对角元随温度的变化曲线;(c) 根据仿真热阻抗矩阵预测的结温随耗散功率变化曲线

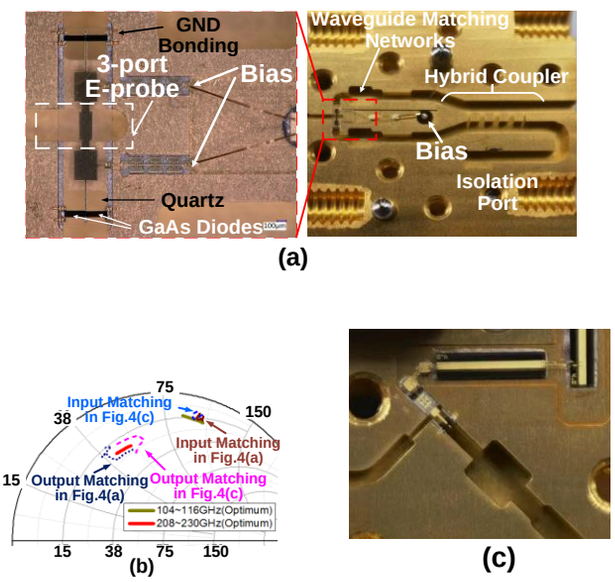

Fig. 7 (a) Details of the fabricated 220 GHz four-port balanced doubler module;(b) Impedance matching in the four-port and conventional circuit;(c) Photograph of the conventional doubler

图7 装配后的220 GHz四端口平衡倍频器模块细节图;(b) 四端口二倍频电路的管结阻抗匹配结果图;(c) 传统倍频器的照片

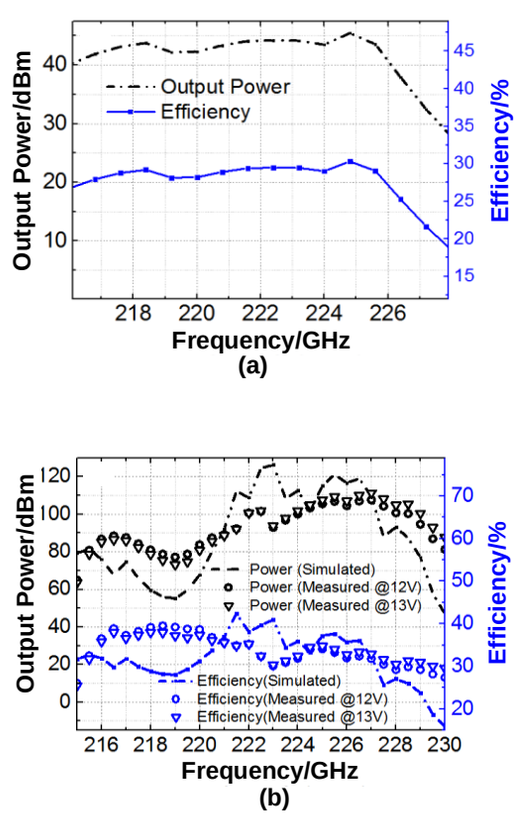

Fig. 8 (a) Performance of the traditional doubler;(b) Output powers and efficiencies of the four-port circuits under different bias.

图8 (a)传统平衡式倍频的测试性能;(b)不同偏置下四端口倍频电路的输出功率和倍频效率

handle higher pumping power. Thus, a 105~115 GHz source with an output power of 196~340 mW has been utilized. Fig. 8(b) shows the measured output power and efficiency versus operation frequency. The peak power is measured to be 111.27 mW at 225.8 GHz with a corresponding efficiency of 33.7%, while the peak efficiency is 39.5% at 218 GHz with a bias of 12 V. This measurement shows little variations compared with the simulation results, proving the validity of the modified electro-thermal model. The lower driven power levels in the lower band cause the decrease in output power and increase in efficiency, as shown in Fig. 8(b).

It is difficult to evaluate the efficiencies of these two doublers under different operation powers. Thus, a comparison of the efficiencies as a function of dissipated power in each diode(DPID) need to be conducted. In Fig. 9(a), the simulated results indicate that the four-port doubler features improved conversion efficiencies and output powers than the Erickson-style one at the same DPID,

with similar junction impedance matching levels achieved in Fig. 7(b). Also, the measured results in Fig. 9(a) shows that the four-port doubler exhibits obviously higher efficiency than the Erickson-style one at the same DPID level, which directly proves the great improvement in conversion efficiency. Meanwhile, results in Fig. 9(a) and (b) could prove that this four-port doubler features more than twice the output power of the Erickson-style circuit, due to its doubled diode number and improved efficiency. Saturation power measurement is prevented by the limited driven powers.

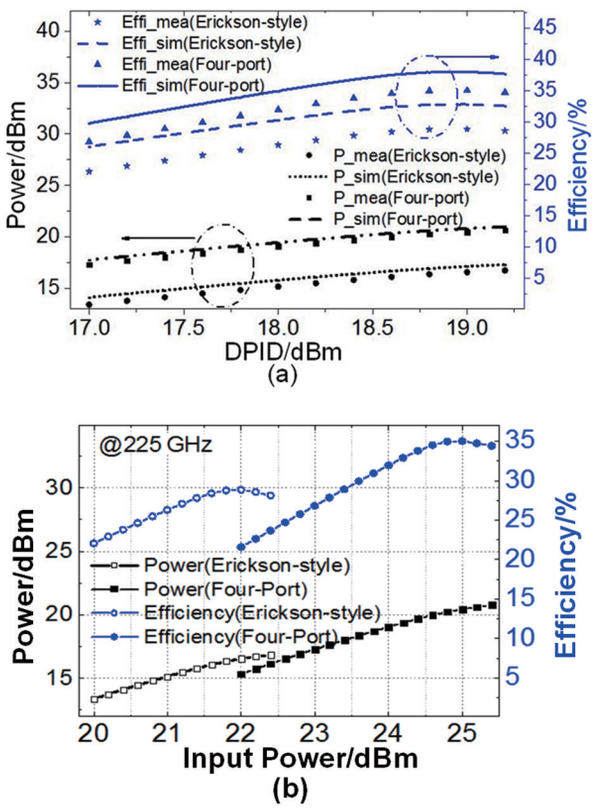

Fig. 9　(a) Comparison of these two modules at the same DPID; (b) Comparison of these two modules as a function of input power
图 9　(a)在相同的 DPID 条件下的两种模块性能对比;(b)在相同输入功率条件下的两种模块对比

Table 1 summarize the reported solid-state frequency doublers in adjacent frequencies. Despite the doubled anode number, the doubler developed in this work could deliver higher efficiency compared with the Erickson-style ones[13-15]. Meanwhile, this four-port frequency topology would provide higher output power when applied with the GaN-based diodes in the future, which represents a valuable method for high power sources.

3　Conclusions

In summary, the proposed novel four-port doubler has been developed, featuring a peak efficiency of 39.5% at 218 GHz in continuous waves. And the proved peak output power is 111.27 mW at 225.8 GHz, which reaches the highest diode-based multiplying power reported in this range to the author's knowledge. This topology also exhibits improved efficiency than the conventional one with doubled power-capability. Thus, this configuration holds great potential in developing high power sources for modern radar systems and other terahertz applications.

Table 1　Comparison of balanced doublers in adjacent frequencies
表 1　相近频段的平衡式二倍频电路对比

Ref	Diode &Num	Topology	Freq (GHz)	Peak power Efficiency	Duty
[13]	GaN 4*2	Erickson-style	177-183	244 mW 11.4%	10%
[14]	GaN 6*2	Erickson-style	190-220	1 006 mW 15%	0.1%
[15]	GaAs 3*2	Erickson-style	170-200	125 mW 25%	CW
This Work	GaAs 3*4	Four-port prototype	215-230	111.27 mW 28~39.5%	CW

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