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A 48 mW DROIC with 15-bit pixel-level ADC for 640×512 mid-wave infrared imagers

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Abstract: A low-power digital readout integrated circuit (DROIC) with 15-bit pixel-level single-slope analog-to-digital converter (ADC) for mid-wave infrared imagers is proposed. A novel pulse comparator featured power-self-adaption is presented for the pixel-level ADC to reduce power consumption. Only when the ramp signal approaches the integration voltage, there is current flowing through the comparator. Furthermore, the pulse output of the comparator also reduces dynamic power consumed by the 15-bit pixel conversion result memories. For achieving the requirement of 15 μm pixel pitch, the memories adopt a 3-transistor dynamic structure and only occupy about 54 μm^2. The current mode transmission is used to read out the analog-to-digital conversion results to column for robustness against voltage crosstalk between adjacent column bus lines. The 640×512 DROIC with this structure is fabricated in 0.18 μm CMOS process. The experimental results demonstrate the DROIC consumes 48 mW at 120 fps. The total integration capacitor is about 740 fF and the charge handling capacity is 8.8 Me^-. The equivalent noise voltage on the integration capacitor is 116 μV and the peak signal-to-noise ratio is 84 dB at the full well.

Key words: IRFPA, DROIC, pixel-level single-slope ADC, power-self-adaptive pulse comparator
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基于15位像素级模数转换器的640×512规格中波红外成像用48 mW数字读出电路

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摘要:提出了一种用于中波红外成像的基于15位像素级单斜率模数转换器的低功耗数字读出电路。像素级模数转换器采用一种新型功耗自适应的脉冲输出型比较器,只有当斜坡电压信号接近积分电压时,比较器才产生功耗。此外,比较器输出脉冲信号,降低了15位量化结果存储器上消耗的动态功耗。该存储器采用三管动态结构,仅占约54 μm^2面积,以满足15 μm像素中心距的面积约束。量化结果以电流模式读出到列级,避免相邻列总线间的电压串扰。基于0.18 μm CMOS工艺,采用该结构,设计并制造了640×512规格的数字读出电路。测试结果表明,在120 Hz的帧频下,功耗仅为48 mW,总积分电容为740 fF,电荷处理能力为8.8 Me^-。在满阱状态,等效到积分电容的噪声电压为116 μV,峰值信噪比为84 dB。

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关 键 词:红外焦平面阵列;数字读出电路;像素级单斜率模数转换器;功耗自适应比较器
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Introduction

For thermal imaging, the cryogenic mid-wave infrared (MWIR) imager has high contrast and resolution [1], so MWIR is widely applied in astronomy, security and surveillance applications. The infrared focal plane array (IRFPA) is the critical component of the infrared imager, consisting of an infrared detector array and a readout integrated circuit (ROIC). To avoid inducing thermal interference in the infrared detector and deteriorating the efficiency and lifetime of the refrigeration machine, low power consumption is critical for cryogenic IRFPAs [2-3].

Because of the short analog signal chain and the data transmission in digital domain, digital ROIC (DROIC) with on-chip analog-to-digital converter (ADC) has been developed and has the advantages of superior signal-to-noise ratio (SNR) and anti-interference capacity [4]. Generally, there are three main kinds of on-chip ADCs: chip-level, column-level and pixel-level, and the latter two kinds are the focus of research [5-7]. In Ref. [5], a column-level dual ramp ADC is presented for high resolution and short conversion time. However, because the conversion time of column-level ADC equals the row period, column-level ADC is limited by the tradeoff between conversion time and power consumption with the increase of the array size and the frame rate like chip-level ADC. Pixel-level ADC has shorter analog signal chain and operates at the frame rate, so it has low-bandwidth and low-noise potential [3]. In Ref. [6], a pixel-level pulse-frequency-modulation (PFM) ADC with extended-counting circuit is reported for large charge-handling capacity and is widely used in long-wave infrared imagers. In Ref. [7], a pixel-level single-slope (SS) ADC is described and is suitable for MWIR imagers. In these implementations, although the bandwidth requirement is low, the pixel-level comparator is always on, leading to high average power.

In this paper, a low-power DROIC with 15-bit pixel-level SS-ADC for MWIR imagers is proposed. A power-self-adaptive pulse comparator is presented to address the challenge of power consumption for the pixel-level ADC. Only when the ramp signal approaches the voltage on the integration capacitor, there is current flowing through the comparator. In addition, compared with the conventional step output, its pulse output makes 15-bit pixel memories store analog-to-digital (A/D) conversion results only once and the dynamic power consumed on the memories is reduced. The memories adopt a 3-transistor (3T) dynamic structure and only occupy 54 μm^2, meeting the area limitation of small pixel pitch. The data retention capability of the dynamic memories is not a concern at liquid nitrogen temperature [8]. Besides, there is large parasitic capacitance on column data buses, so a global gray-coded counter, whose values are applied to the column buses, is adopted for low dynamic power consumption. Because there is only one different bit between two successive gray codes, the jump times are reduced and the error rate is low. After A/D conversion, the data in pixel memories are read out to column in current mode to avoid voltage crosstalk between adjacent bus lines.

The structure of this paper is as follows. Section 1 introduces the proposed readout circuit and its operating principle. The pixel-level power-self-adaptive pulse comparator, pixel-level dynamic memory and column data write/read circuit are detailed. Section 2 presents the experimental results. The conclusion is given in Sect. 3.

1 Circuit implementation

1.1 DROIC architecture

A low-power DROIC for MWIR imagers with the pixel-level SS-ADC is proposed. The DROIC adopts direct injection (DI) structure to meet the restricted area limitation of pixels with ADC [9]. The current injection efficiency η , which is defined as the ratio of the current I_{IN} flowing into ROIC to the detector photocurrent I_D, is calculated by Eq. 1 where g_m is the transconductance of the injection transistor and R_D is the infrared photon detector resistance [1]. In MWIR applications, R_D is generally large, so η is high enough and it is appropriate to adopt the DI structure.

$$\eta = \frac{g_m R_D}{1 + g_m R_D} \quad , \quad (1)$$

where I_{IN} is integrated on the capacitor C_{INT} and is converted to the voltage V_{INT} which is then digitalized. The SS-ADC is an appropriate architecture for pixel-level ADCs due to its compact feature [10]. The ramp generator and the counter are shared by all pixels. Only a comparator and N-bit memories are located in the pixel. The simplified block diagram of the conventional digital pixel with SS-ADC [7, 10] is shown in Fig. 1. After integration, V_{INT} and the ramp bus signal V_{RAMP} are connected to the inputs of the pixel comparator. The data in pixel memories are continuously refreshed following the counter bus signals $BUS < N: 1 >$ before the output of the comparator $WRT < i, j >$ flips. When $WRT < i, j >$ flips, $BUS < N: 1 >$ are latched as A/D conversion results. In such structure, the comparator needs to operate at low-noise and high-speed mode throughout the A/D conversion process to meet the requirements of SNR and linearity [10]. In addition, column driver circuit consumes much power to refresh the data of pixel memories.

Figure 2 illustrates the block diagram of the proposed digital pixel with 15-bit SS-ADC and the proposed low-power DROIC based on this digital pixel. A novel power-self-adaptive pulse comparator is presented and a sampling capacitor C_S is added. C_{MOS} and C_S are MOS and MIM capacitors respectively and are both used as integration capacitors during the integration phase to in-

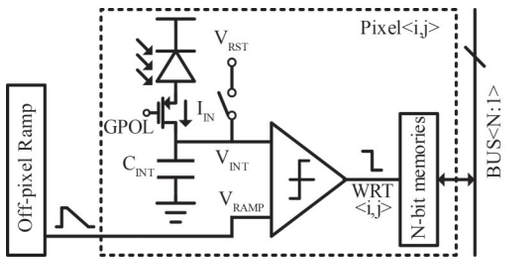

Fig. 1　Conventional digital pixel with SS-ADC
图1　传统基于单斜率模数转换器的数字像素

crease the charge handling capacity in the compact pixel. The total integration capacitor C_{INT} equals $C_{MOS} + C_S$.

The timing diagram of the proposed DROIC is shown in Fig. 3. ϕ'_{INT} is the delay signal of ϕ_{INT}. After the integration phase when the detector current is integrated on C_{MOS} and C_S, the signal ϕ_{AD} is on and the voltage on C_S is quantized by the pixel SS-ADC. Though the switch controlled by ϕ'_{INT} injects charge to C_S, its gate capacitor is far less than C_S so that the linearity of this ADC is scarcely affected. During the A/D phase, the ramp signal V_{RAMP} is connected to the left plate of C_S and its corresponding gray-coded bus signals $BUS<15:1>$ are connected to the 15-bit dynamic memories. $BUS<15:1>$ are driven by the column data write/read (W/R) circuit. Owing to the bottom-plate-sampling technique, when $V_{RAMP} = V_{INT}$, the negative input voltage of the comparator V_N equals the reference voltage V_{REF}. Once $V_{RAMP} < V_{INT}$, the digital codes of $BUS<15:1>$ are written into the pixel memories by the narrow pulse output of the comparator $WRT<i,j>$. During the pixel-to-column readout (RO) phase, the data in the pixel memories are read out to column memory array via $BUS<15:1>$ by the column data W/R circuit row-by-row. In the next frame, the data in the column memory array are output off the DROIC through the data output multiplexer (MUX) circuit.

This proposed DROIC achieves low-power performance in the compact pixel due to several adopted techniques, which are detailed in Sect. 1.2 and 1.3, including the power self-adaptive pulse comparator and the gray-coded bus signals.

1.2　Power-self-adaptive pulse comparator

The proposed low-power pixel-level power-self-adaptive pulse comparator is shown in Fig. 4(a) together with other pixel circuits drawn as dotted lines. Some signals correspond to the counterparts in Fig. 2. The comparator consumes ultra-low average power with low-noise and high-speed performance to meet the SNR and linearity requirements of DROIC.

V_{REF} is set to Eq. 2. V_{THP} is the threshold voltage of PMOS transistors. V_{OV2} and V_{OV5} are the overdrive voltages of M_2 and M_5 when their drain currents are $I_0/2$ and I_0, respectively. I_0 is the saturation current of M_5 when the gate voltage V_{G5} of M_5 equals V_{BP}. ΔV is about 50 mV to ensure M_1 and M_2 in saturation region when $V_N = V_{REF}$. M_8 is biased by V_{SS} to match M_7. M_6 is biased by V_{BP} to limit the short current of the comparator's second stage when $|V_N - V_{REF}|$ is small.

$$V_{REF} = V_{DD} - |V_{THP}| - |V_{OV2}| - |V_{OV5}| - \Delta V \quad . \quad (2)$$

The timing diagram of the comparator is depicted in Fig. 4(b). The comparator works as follows. During the integration phase, $V_{G5} = V_{DD}$, $V_N = V_{REF}$, R_{CMP} and $\overline{\phi_{AD}}$ are '1'. Therefore, the total current of the comparator I_C is zero and $WRT<i,j>$ is '0'. The RS-latch consisting of two NOR gates is reset by the signal R_{CMP}.

During the A/D conversion phase, $V_{G5} = V_{BP}$, $\overline{\phi_{AD}}$ and R_{CMP} are '0'. M_5 is turned on. V_{RAMP} is initially equal to a high voltage so that V_N becomes higher than V_{REF} and falls with the decline of V_{RAMP}. V_N is expressed as:

$$V_N = V_{REF} + (V_{RAMP} - V_{INT}) = V_{DD} - |V_{THP}| - |V_{OV2}| - |V_{OV5}| - \Delta V + (V_{RAMP} - V_{INT}) \quad . \quad (3)$$

(I) When $V_{RAMP} \geqslant V_{INT} + |V_{OV2}| + |V_{OV5}| + \Delta V$, $V_N \geqslant V_{DD} - |V_{THP}|$ so that M_1 is in cut-off region. Due to the current mirror consisting of M_3 and M_4, M_4 is also in cut-off region. As a result, the node V_{MID} equals '1' and $WRT<i,j>$ equals '0'. Within this range, I_C is zero, namely the comparator has no power consumption.

(II) When V_{RAMP} falls below $V_{INT} + |V_{OV2}| + |V_{OV5}| + \Delta V$, but is higher than V_{INT}, I_C increases from zero and $WRT<i,j>$ is still '0'.

(III) When V_{RAMP} is just below V_{INT}, $WRT<i,j>$ becomes '1'. V_{G7} is set to '1', which induces M_7 into the cut-off region. The gray-coded bus signals on $BUS<15:1>$ of this moment are latched in pixel dynamic mem-

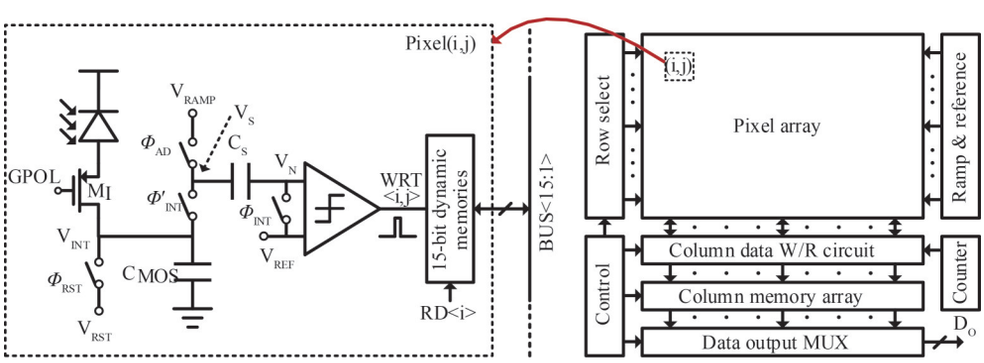

Fig. 2　Block diagram of the proposed DROIC with the novel pixel-level SS-ADC
图2　提出的基于新型像素级单斜率模数转换器的数字读出电路框图

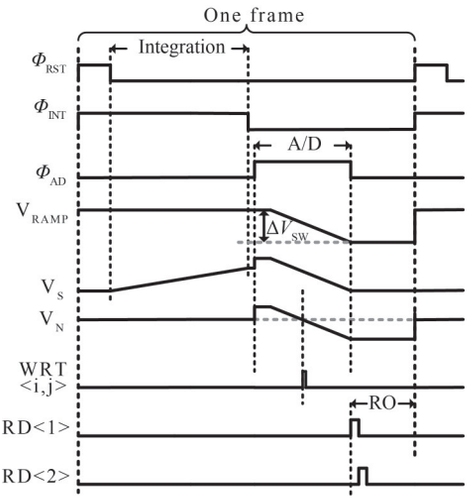

Fig. 3 Timing diagram of the proposed DROIC
图3 提出的数字读出电路的时序图

ories. As in case (I), I_C changes back to zero, and $WRT < i,j >$ becomes '0'. This state remains until the A/D conversion ends.

I_5 and I_6, which are the drain current of the transistors M_5 and M_6, are illustrated in Fig. 4 (b). $I_C \approx I_5 + I_6$. I_5 is the largest proportion of I_C. Figure 5 shows the simulation results of I_C when V_{INT} equals 0.8 V and 1.5 V, respectively. It demonstrates that there is current flowing through the comparator only when V_{RAMP} approaches V_{INT}, namely V_N approaches V_{REF}. The average value of I_5 is less than 20% of I_5's maximum value which equals to the average value of the traditional comparator with the same performance.

In summary, the voltage range ΔV_I of V_N, where $I_5 > 0$, is given by Eq. 4 and is much smaller than the voltage swing ΔV_{SW} of V_{RAMP}. The comparator's average power consumption P_{CMP} can be calculated by Eq. 5. T_F and T_{AD} are the frame time and the A/D conversion time, respectively. Because $T_{AD} \ll T_F$ and $\Delta V_I + \Delta V \ll \Delta V_{SW}$, P_{CMP} is very low and is far less than the counterpart of always-on comparator. Cooperating with the DROIC operation principle that V_N equals V_{REF} when the comparator flips, high SNR and high speed are realized under ultra-low average power consumption.

$$\Delta V_I = \left(V_{DD} - \left|V_{THP}\right|\right) - V_{REF} = \left|V_{OV2}\right| + \left|V_{OV5}\right| + \Delta V \quad (4)$$

$$P_{CMP} \approx \frac{T_{AD}}{T_F}\frac{V_{DD}I_0(\Delta V_I + \Delta V)}{2\Delta V_{SW}} \ll V_{DD}I_0 \quad . \quad (5)$$

1.3 Pixel dynamic memories and column data W/R circuit

During the A/D conversion phase, the bus signals on $BUS < 15:1 >$ are latched in pixel-level memories controlled by the pixel comparator's pulse output. The smaller area the memories occupy, the larger the charge handling capacity is. Noting that the leakage current is extremely low at liquid nitrogen temperature [8], a 3T dynamic memories with a single write/read port is implemented to store the A/D conversion results and its data retention capability is not a concern. Besides, the 15-bit column bus lines are placed in the small-width column, so there is large parasitic capacitance (>1pF) and voltage crosstalk between adjacent bus lines. The bus signals are generated from a global gray-coded counter to reduce the jump times for lower dynamic power consumed on the column buses. A column current comparator is adopted to read out the data from pixel memories to column memory array for robustness against voltage crosstalk between adjacent bus lines.

The circuit diagram of the pixel dynamic memories and the column data W/R circuit, which consists of tri-state gates and current comparators, is shown in Fig. 6. $\overline{\phi_C}$ and ϕ_C are complementary signals.

During the A/D conversion phase, the global gray-coded counter starts from zero and the tri-state gates are enabled by the enable signal EN_{TRI}. The counter results $G < 15:1 >$ are transmitted to $BUS < 15:1 >$. When $WRT < i,j >$ in the pixel of the i^{th} row and the j^{th} column flips, the bus signals on $BUS < 15:1 >$ are written in the memories. In the meantime, the column comparator is in the sleep mode.

During row-by-row pixel-to-column readout phase, ϕ_C is '1'. The current comparators are powered on and are connected to $BUS < 15:1 >$. The readout signal $RD < i >$ controls the A/D conversion results' readout. If the pixel memory stores '0', no current flows into this memory so that the drain current I_2 of M_2 is equal to the drain current I_1 of M_1 and the current comparator's output OUT is '0'. If the memory stores '1', $I_2 = I_1 - I_{MEM}$

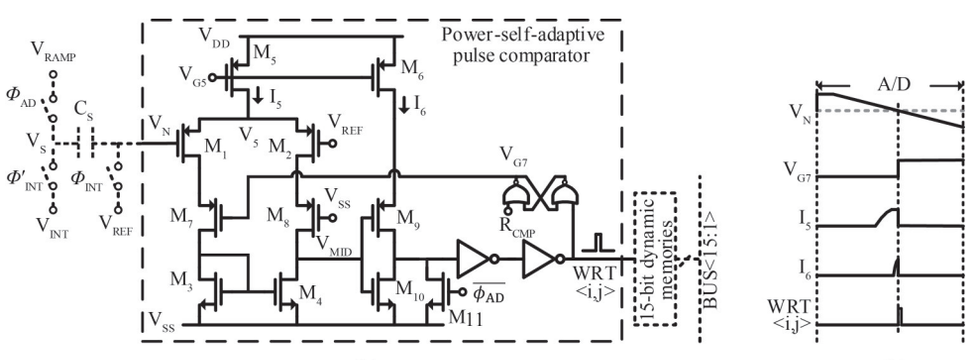

Fig. 4 (a) The circuit diagram, and (b) the timing diagram of proposed power-self-adaptive pulse comparator:(a)(b)
图4 提出的功耗自适应脉冲输出型比较器的(a)电路图,(b)时序图

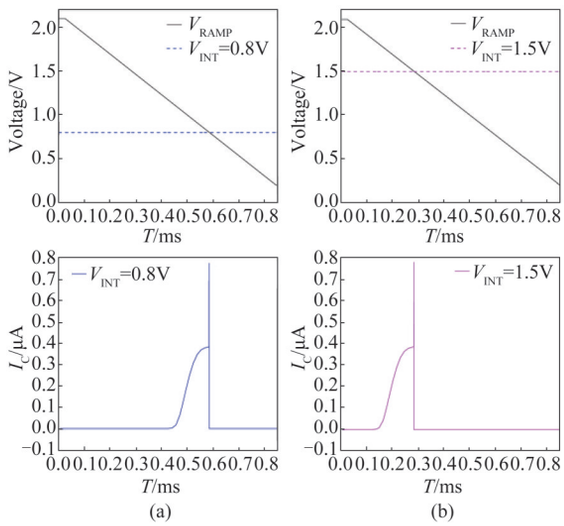

Fig. 5　Simulation results of I_C when V_{INT} equals (a) 0.8V, (b) 1.5 V, respectively
图5　当V_{INT}分别等于(a)0.8V,(b)1.5 V时,I_C的仿真结果

where I_{MEM} is the current of the memory and OUT is '1'. Because the drain current of M_5 consistently equals I_1, the voltage on the bus is clamped to avoid voltage cross-talk between adjacent bus lines.

Because there is only one different bit between two successive gray codes, the power consumption of column data W/R circuit decreases and the error rate is low compared with the binary-coded counterpart. Moreover, owing to adopting the 3T dynamic memories, the area occupied by the pixel-level ADC is small so that the charge handling capacity is large enough.

2　Experimental results and discussions

The proposed low-power DROIC is fabricated in 0.18 μm 1P5M CMOS process for an MWIR detector array. The DROIC microphotograph with a chip size of 11.5 mm×13 mm is shown in Fig. 7(a). The chip mainly comprises 640×512pixel array with 15-bit pixel-level SS-ADC, ramp generator, column data W/R circuit, column memory array and data output MUX circuit. The pixel pitch is 15 μm and the pixel-level memories occupy about 54 μm^2, meeting the pixel area limitation for charge handling capacity. The total integration capacitor C_{INT} is about 740 fF and the charge-handling capacity is about 8.8 Me^-.

This DROIC is electrically tested by applying different DC inputs to simulate gray-scale images through the reset voltage signal V_{RST} of C_{INT}. For low temperature testing, a test printed circuit board (PCB) shown in Fig. 7 (b) is custom-designed, consisting of the part A with the DROIC chip, the part B with decoupling capacitors and the part C with excitation sources. V_{RST} is generated by a high-precision DAC on part C and varies from 0.2 ~2.1 V. During the test, part A is placed in a liquid nitrogen container for cooling. Figure 8 shows the layout of 2×2 pixels.

The total power consumption is 48 mW under 1.8V/3.3V power supply at the frame rate of 120 Hz and the A/D conversion time is about 820 μs. The chip's function is tested. V_{RAMP}, which is output by a buffer, is captured by Agilent oscilloscope as shown in Fig. 9 and conforms to the expected design target. The digital output data are collected and processed by an FPGA. The data values are stable and are relative to V_{RST}. This demonstrates the data stored on the 3T dynamic memories are not lost at liquid nitrogen temperature.

Noise performance is an important concern for DROIC. The equivalent noise voltage $V_{n,ROIC}$ on C_{MOS} and C_S can be expressed by Eq. 6. $V_{n,CMP}$ is the equivalent input noise voltage of the pixel comparator when $WRT < i,j >$ flips and $V_{n,RAMP}$ is the output noise voltage of the off-pixel ramp generator. There are twice reset noise introduced after reset phase and integration phase. The power consumption and the area of the ramp generator are al-

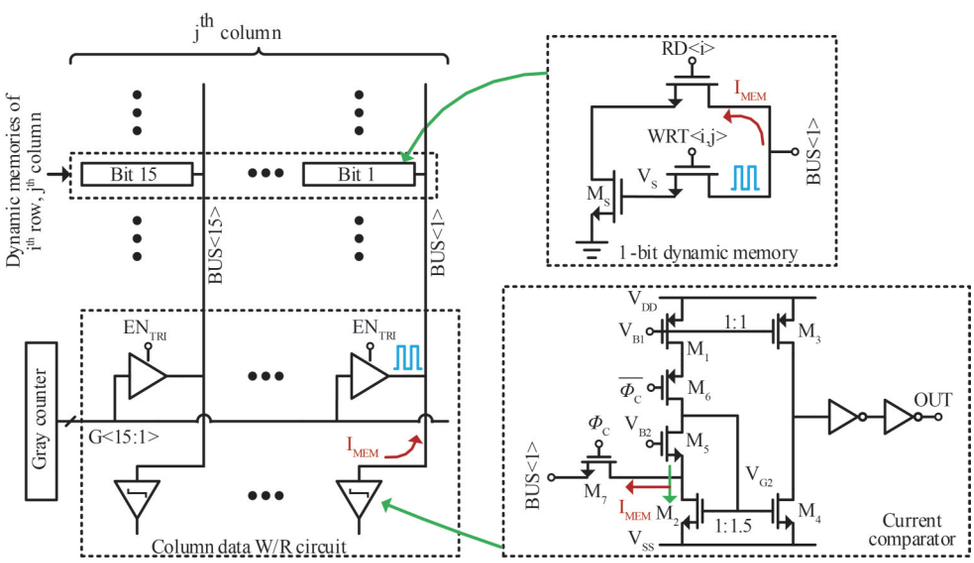

Fig. 6　The circuit diagram of the pixel dynamic memory and the column data W/R circuit
图6　像素动态存储器和列级读写电路的电路图

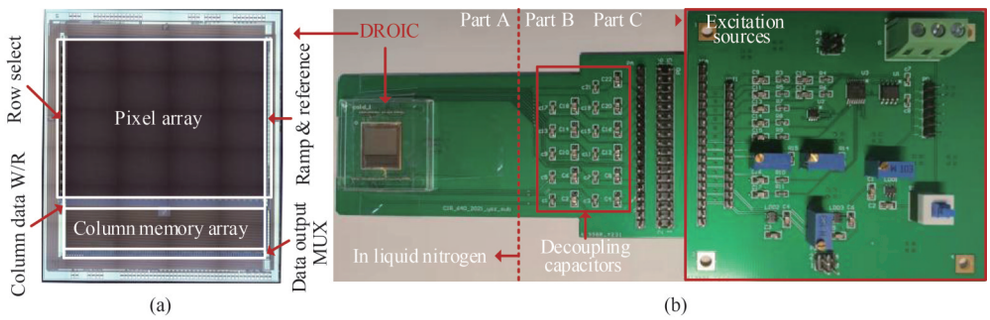

Fig. 7 (a) The microphotograph of the DROIC, (b) custom-designed PCB to test the DROIC
图7 (a)数字读出电路的显微照片,(b)测试数字读出电路的定制化印制电路板

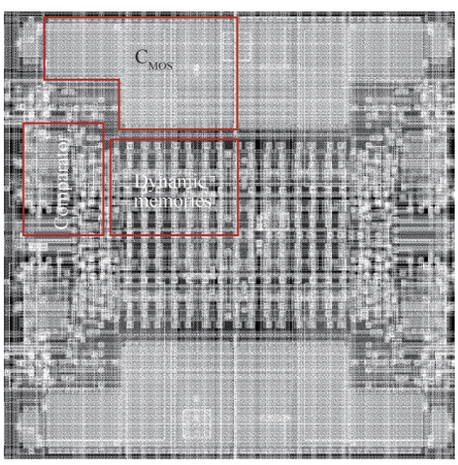

Fig. 8 the layout of 2×2 pixels
图8 2×2像素的版图

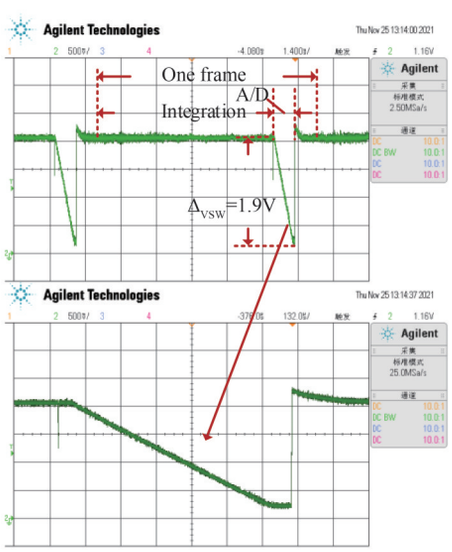

Fig. 9 Measured V_{RAMP} captured by oscilloscope
图9 通过示波器检测到的斜坡信号VRAMP

most unlimited, so $V_{n,\mathrm{RAMP}}$ is designed to be far less than $V_{n,\mathrm{CMP}}$. The comparator is the main noise source. Though the proposed pixel-level power-self-adaptive pulse comparator consumes ultra-low average power, it consumes high enough power for low-noise and high-speed performance when $WRT < i,j >$ flips. Therefore, $V_{n,\mathrm{CMP}}$ is low.

$$V_{n,\mathrm{ROIC}}^2 = \frac{kT}{C_{\mathrm{MOS}}+C_{\mathrm{S}}} + \frac{kTC_{MOS}}{C_{\mathrm{S}}(C_{\mathrm{MOS}}+C_{\mathrm{S}})} + V_{n,\mathrm{CMP}}^2 + V_{n,\mathrm{RAMP}}^2 = \frac{kT}{C_{\mathrm{S}}} + V_{n,\mathrm{CMP}}^2 + V_{n,\mathrm{RAMP}}^2 \quad (6)$$

Figure 10 presents a SNR histogram of the whole pixel array at the full well and the peak SNR (PSNR) is up to 84 dB. The equivalent noise voltage on the integration capacitor is about 116 μV. This demonstrates the proposed DROIC has good noise performance under low power consumption.

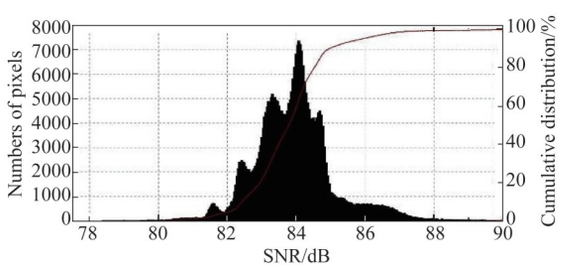

Fig. 10 SNR histogram of the whole pixel array at the full well
图10 满阱下,整个阵列的信噪比直方图

The gray-scale image with V_{RST} = 1.35 V is shown in Fig. 11(a) and its fixed pattern noise (FPN) is shown in Fig. 11(b). The measured FPN, which is defined as the ratio between the standard deviation and the mean, is about 0.28%. Through changing V_{RST}, the digital output versus the integration voltage curve is shown in Fig. 12. The non-linearity results are shown in Fig. 13 and the linearity is about 99.76%.

Table 1 shows the performance comparison between our proposed DROIC and some recent DROICs. The pro-

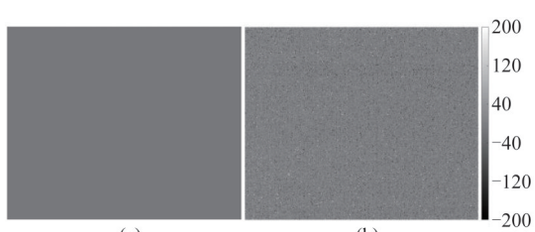

Fig. 11 When V_{RST} = 1.35 V (a) the gray-scale image of the DROIC, (b) the gray-scale image of FPN
图11 V_{RST}=1.35 V时(a)数字读出电路的灰度图,(b)固定模式噪声的灰度图

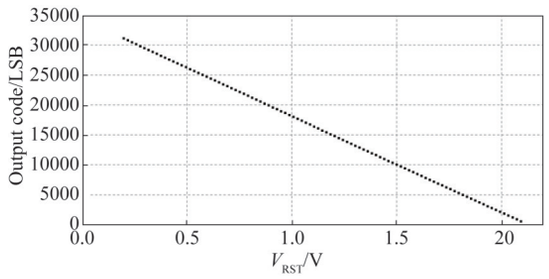

Fig. 12　The digital output versus the reset voltage V_{RST}
图12　数字输出与复位电压V_{RST}的关系

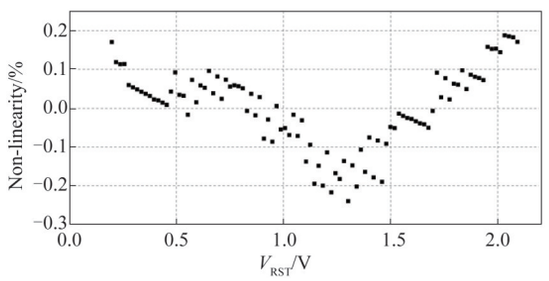

Fig. 13　The non-linearity versus the reset voltage V_{RST}
图13　非线性与复位电压V_{RST}的关系

posed DROIC is more competitive in power performance. Figure of merit (FoM) expressed in Eq. 7 adopts the definition as the power normalized to the number of pixels and the frame rate per step from Ref. [13]. This work, which achieves the lowest FoM among Ref. [5, 11-12], is leading in terms of energy efficiency.

$$\mathrm{FoM} = \frac{\text{Total power}}{\text{Pixel number} \times \text{Frame rate} \times 2^{\text{ADC resolusion}}}. \quad (7)$$

Table 1　Performance comparison of DROICs
表1　读出电路性能比较

Parameter	[5]	[12]	[11]	This work
Technology process /nm	180	–	90	180
Pixel array	640×512	1 024x768	32×32	640×512
Pixel size /μm	10	10	15	15
Frame rate /Hz	180	100	400	120
ADC resolution /bit	13	14	15	15
Power consumption /mW	110	100	1. 4	48
Charge capacity /e^-	2M	2. 6M	2. 4M	8. 8M
Noise voltage */μV/ Peak SNR */dB	160/N. A.	N. A. /83**	N. A. /79	116/84
FoM**/(pJ/pixel·step)	228	77. 6	104	37. 3

* At the full well **Calculated based on the data given in the reference

3　Conclusions

A low-power 640×512 DROIC with 15-bit pixel-level SS-ADC is proposed for cryogenic MWIR imagers and is fabricated in 0. 18 μm CMOS process for verification. The pixel pitch is 15 μm. Cooperating with bottom-plate-sampling technique, a power-self-adaptive pulse comparator is presented for the pixel-level ADC to reduce power consumption. The power consumption of the comparator is nearly zero in most time and turns high enough only when the ramp signal approaches the integration voltage. In addition, its pulse output lowers the dynamic power consumed on the pixel memories because the A/D conversion results are stored only once. The 15-bit memories adopt a 3T dynamic structure and only occupy 54 μm^2, while the data retention capability is not a concern at liquid nitrogen temperature. The A/D conversion results stored in the pixel memories are read out to column in current-mode to avoid voltage crosstalk between adjacent bus lines. The experimental results demonstrate that the DROIC consumes 48mW at 120 fps. The pixel SS-ADC is area-efficient and the proposed DROIC achieves high charge handling capacity of 8. 8 Me^-. The peak signal-to-noise ratio is 84dB at the full well. These results prove that the proposed DROIC is effective in lowering power consumption while keeping high SNR.

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