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FLIP-CHIP INTEGRATED OSCILLATOR WITH REDUCED PHASE NOISE AND ENHANCED OUTPUT POWER BY USING DGS

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Abstract: A novel defected ground structure (DGS) was designed and applied to a flip-chip integrated millimeter wave oscillator. The characteristics of two oscillators with and without DGS were analyzed and compared. Measurement data shows that the phase noise of the oscillator with DGS is reduced by 4 ~ 6dB, and the output power of the oscillator is increased by 0.8dBm in comparison with the oscillator without DGS. It is found that, when DGS is embedded in the resonant tank and the output terminal of an oscillator, the phase noise can be reduced and the output power will be enhanced.

Key words: defected ground structure(DGS); phase noise; output power; flip chip; oscillator

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采用 DGS 降低相位噪声和提高输出功率的倒扣集成振荡器

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摘要:设计了一种新型的缺陷接地结构(DGS)并将之应用到倒扣集成毫米波振荡器中.分析并比较了具有 DGS 结构和没有 DGS 结构的两种振荡器性能.测试数据显示具有 DGS 结构的振荡器与没有 DGS 结构的振荡器相比,相位噪声降低 4 ~ 6dB,输出功率增加 0.8dBm.研究结果表明 DGS 结构嵌入到振荡器的谐振电路和输出端时,振荡器的相位噪声降低且输出功率增大.

关 键 词:缺陷接地结构;相位噪声;输出功率;倒扣芯片;振荡器

Introduction

An oscillator is one of the most important circuit elements in wireless communication, radar, radio frequency identifier systems. The phase noise and output power of an oscillator are important figures of merit [1-3]. Especially, the lower the phase noise is, the better the system will be. The dielectric resonator is useful to obtain oscillator with low phase noise. But dielectric resonator is profitless to integrate with planar circuits and is difficult to be applied in smaller system. A novel structure-DGS has been confirmed to be useful in improving the phase noise and output power of oscillator and integrating with planar circuits[4,5]. DGS shows band rejection property in some frequency range and band pass property in some frequency range. Ahn et al. proposed DGS at first[6]. Since then, a few groups have applied DGS to improve the performance of microwave circuits[7,8]. Up to now, most of research groups have focused on DGS with operation frequency lower than 10GHz. In this paper, a novel DGS structure was designed and applied to hybrid integrated mil-

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limeter wave oscillator. Flip chip technique was used in hybrid integrated oscillator. CPW (co-planar waveguide) transmission line was used in the circuit instead of microstrip. Measurement data shows that the phase noise of the oscillator with DGS is evidently reduced and the output power of the oscillator with DGS is increased in comparison with that of the oscillator without DGS.

1 Design and measurement of the DGS

A novel DGS in CPW transmission line was designed on the semiconductor GaAs substrate as shown in Fig. 1. The slots of the DGS give rise to the equivalent L-C components. At the resonant frequency, the equivalent parallel L-C components form a band rejection property, which is similar to dielectric resonator. The length and width of the slots determine values of inductance and capacitance in the equivalent circuit, which eventually determines the resonant frequency of the structure. When the oscillator operates in millimeter wave frequency, it is difficult for DGS to be fabricated on the printed circuit board (PCB). So, GaAs with thickness of 500μm and dielectric constant of 12.9 was selected as the substrate of the DGS and microelectronics process was adopted in the fabrication of the DGS to ensure process resolution. Fig. 1 (a) is the layout of DGS1 that the resonant frequency is the fundamental one of the oscillator and Fig. 2 (b) is the layout of DGS2 that the resonant frequency is the second order harmonic of the designed oscillator. Characteristic impedance of the CPW transmission lines is 50Ω. Width of the CPW transmission line is 80 μm and the gap between transmission line and ground plane is 60 μm and the length of transmission line is 1000μm. The slot gaps of two symmetric DGS in both ground planes in two layouts are 5μm. Other sizes are marked in Fig. 1. Fig. 2 (a) shows measured and simulated results of DGS1. Simulated resonant frequency is 35.6GHz and measured one is 36.5GHz. The little error between measured results and simulated ones may be caused by over etching process. Fig. 2 (b) shows simulated results of DGS2 and the resonant frequency is 71.2GHz which is equal to the second order harmonic frequency of DGS1. 71.2 GHz is over measurement range of the measurement equipment, so measured results can not be shown in Fig. 2 (b). The EM simulator, IE3D, is used for this simulation.

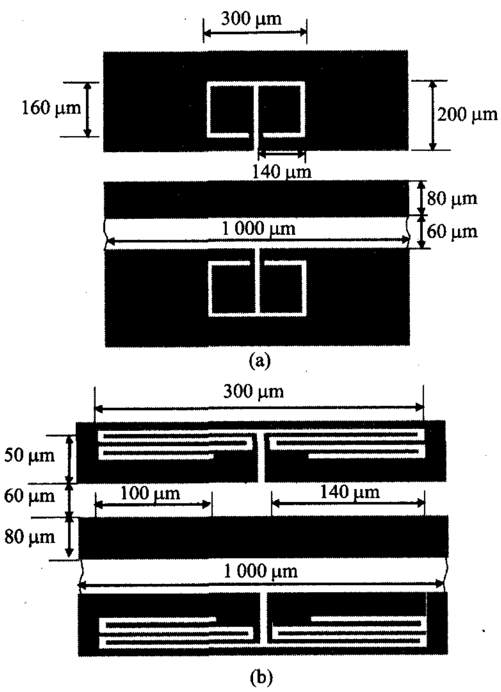

Fig. 1 (a) Layout of DGS1 (b) layout of DGS2
图1 (a)DGS1 版图 (b)DGS2 版图

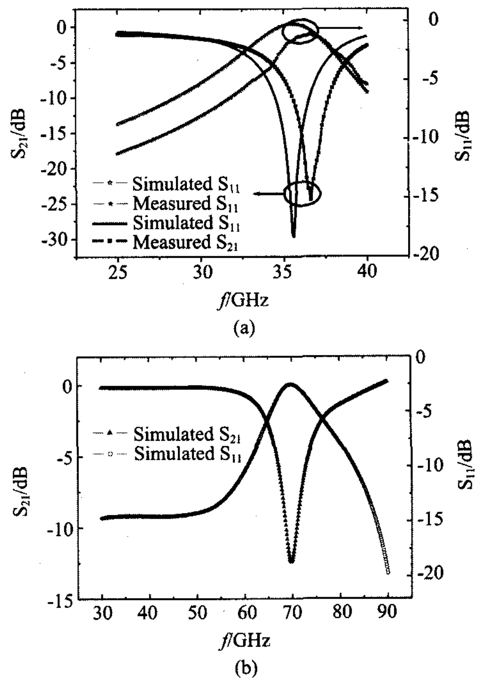

Fig. 2 (a) Measured and simulated S parameters of DGS1 (b) simulated S parameters of DGS2
图2 (a)DGS1 测试和仿真的 S 参数 (b)DGS2 的仿真参数

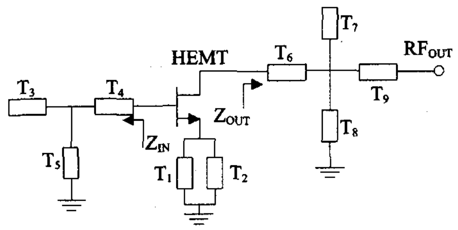

Fig. 3 Schematic of the oscillator without DGS
图 3 没有 DGS 结构的振荡器拓扑图

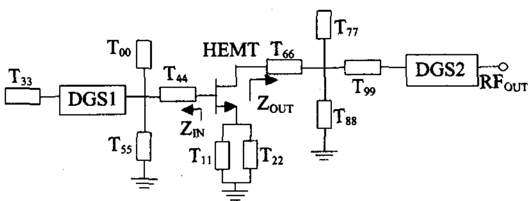

Fig. 4 Schematic of the oscillator with DGS
图 4 具有 DGS 结构的振荡器拓扑图

2 Design and measurement of the oscillator

The oscillator circuit was designed by using Agilent Advanced Design System (ADS). First, the normal oscillator without DGS was designed at center frequency of 36.5GHz. The schematic circuit of the oscillator is shown in Fig. 3. The active device in the oscillator is UMS GaAs HEMT with gate length of 0.25μm and gate width of 6 × 60μm. The DC bias voltages of GaAs HEMT are selected according to the smallest noise figure. The input impedance and output impedance of GaAs HEMT are got at the same time. GaAs HEMT model with common source connection is used in the oscillator design. The same two CPW transmission lines T_1 and T_2 are symmetrically connected between the HEMT's source and the ground, providing a positive feedback to make the HEMT more unstable. CPW transmission lines T_3, T_4 and T_5 comprise the resonant circuit, T_6, T_7, T_8 and T_9 comprise the output match network. Then, the oscillator with DGS was designed. DGS1 is embedded in the resonant circuit of Fig. 3, and DGS2 is embedded in the output network of Fig. 3 to form schematic circuit as shown in Fig. 4. In order to keep impedance Z_{IN} of the resonant terminal and impedance Z_{OUT} of the output network after embedding DGS1 and DGS2, values of CPW transmission lines T_3, T_4, T_5, T_6, T_7, T_8 and T_9 are adjusted into

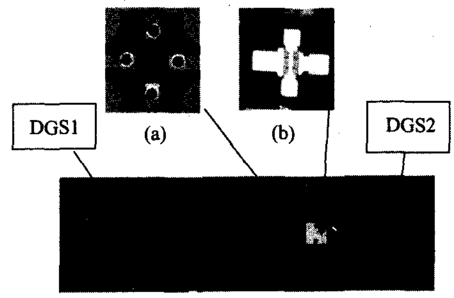

Fig. 5 Photograph of the flip-chip hybrid integrated oscillator with DGS at the resonant and output (a) enlarged bumps (b) top view of GaAs HEMT
图 5 具有 DGS 结构倒扣混合集成振荡器照片 (a) 放大的凸点 (b) GaAs HEMT 的正面照片

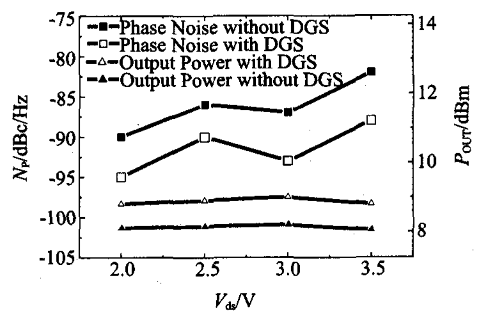

Fig. 6 The phase noise (N_P) and output power (P_{OUT}) of the oscillators, at V_{gs} = −0.5V
图 6 在栅源直流偏压 V_{gs} = −0.5V 时，振荡器的相位噪声和输出功率

T_{33}, T_{44}, T_{55}, T_{66}, T_{77}, T_{88} and T_{99} and the short stub CPW transmission line T_{00} is added to resonant terminal as shown in Fig. 4. Measured S-parameter model of DGS1 and simulated one of DGS2 are used in the simulated oscillator.

The passive CPW transmission lines of the two oscillators with and without DGS were fabricated on GaAs substrate and then were integrated with GaAs HEMT active device together. Flip-chip technique was used in hybrid integrated oscillator in order to reduce parasitic effect of gold wire bonding as shown in Fig. 5. The size of the oscillator with DGS is 1.7 × 5.37mm^2. Fig. 5 (a) is enlarged picture of bumps and Fig. 5 (b) is the top view of GaAs HEMT chip. After hybrid integration, two oscillators were mounted on PCB respectively. Bias pads of the chips were bonded on PCB to connect with DC power supply and RF output port to connect with RF probes in measurement. The measured phase noise and output power of the two oscillators de-

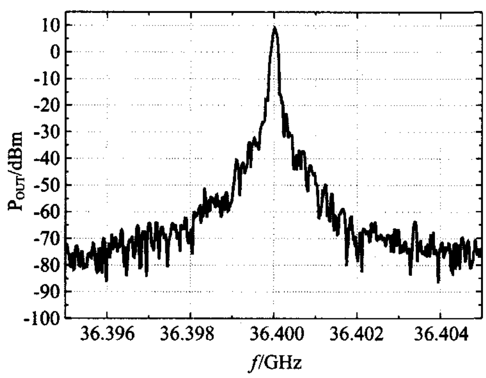

Fig. 7 The output spectrum of the oscillator with DGS (V_{ds} = 3V, V_{gs} = −0.5V)
图7 在直流漏源偏压 V_{ds} =3V,栅源偏压 V_{gs} = −0.5V 时，具有 DGS 振荡器的输出频谱

pending on the bias voltages V_{ds} are depicted in Fig. 6. The phase noise of the oscillator with DGS varies from −88dBc/Hz to −95dBc/Hz at 1 MHz offset and is lower than that of the oscillator without DGS by 4 ~ 6dB, the output power of the oscillator with DGS increases about 0.8dBm than that of the oscillator without DGS at V_{ds} from 2.0V to 3.5V and V_{gs} = −0.5V. Fig. 7 shows the output spectrum of the oscillator with DGS resonator at V_{ds} =3V and V_{gs} = −0.5V. It exhibits reduced phase noise performance of −95dBc/Hz at 1MHz offset and increased output power performance of 9dBm.

3 Conclusion

A novel DGS was designed and successfully applied to improve the performance of the millimeter wave oscillator in this paper. The flip-chip technique was applied to implement hybrid oscillators that include active device chip and off chip resonators. Compared to the oscillator without DGS, the oscillator with embedded DGS exhibits a 4 ~ 6 dB reduction in phase noise and an increase of 0.8 dBm in the output power.

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