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Cavity-backed on-chip patch antenna in 0.13 μm SiGe BiCMOS technology

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Abstract: This letter presents a 340 GHz cavity-backed on-chip patch antenna design and fabrication using standard 0.13 μm SiGe BiCMOS technology. The patch placed at AM layer is fed by a stripline at LY layer through via holes from LY to AM layer. The via holes are built between the top metal layer (AM layer) and the ground plane (M1 layer) to form a cavity which improves the impedance matching bandwidth and the radiation performances of the antenna. The proposed antenna shows a simulated impedance bandwidth of 9.2 GHz from 335.6 to 344.8 GHz for S_{11} less than −10 dB. The simulated gain of the antenna at 340 GHz is 3.2 dBi. The total area of the antenna is 0.5×0.56 mm^2.

Key words: 0.13 μm SiGe BiCMOS technology, cavity backed, patch antenna, on-chip antenna
PACS: 84.40.Ba, 84.40.Az, 84.35.+i, 02.10.Yn

基于 0.13 μm SiGe BiCMOS 工艺的在片背腔贴片天线

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摘要: 提出了一款基于 0.13 μm SiGe BiCMOS 工艺设计、加工的 340 GHz 在片背腔贴片天线. 辐射贴片位于 AM 金属层,带状线馈线置于 LY 金属层并通过连接 AM 金属层和 LY 金属层的金属化通孔对辐射贴片馈电. 通过设计连接 AM 金属层和 M1 金属层的金属化通孔形成谐振腔体展宽了天线阻抗带宽、提升了天线辐射性能. 天线的仿真阻抗带宽($S_{11} \leqslant -10$ dB)为 9.2 GHz(335.6 ~ 344.8 GHz). 天线在 340 GHz 处的仿真增益为 3.2 dBi. 天线的整体尺寸为 0.5×0.56 mm^2.

关 键 词: *0.13 μm SiGe BiCMOS* 工艺; 背腔; 贴片天线; 在片天线

中图分类号: TN827 + .3 **文献标识码:** *A*

Introduction

In recent years, with the high development of CMOS and BiCMOS integrated circuit (IC) technologies, silicon-based ICs at mm-wave and THz frequencies have opened up opportunities for many applications such as sensing, short range imaging and medical applications [1]. As the key component in a communication system, an antenna has independent properties that affect the system as a whole [2]. Fully integrated on chip antennas (OCAs) can eliminate the need for off-chip connection and packaging processes, which would introduce extra loss and make the overall size bulky [3]. Moreover, fully integrated OCAs reduce the overall form-factor of the system, and facilitate assembly as high precision mm-wave interconnects are eliminated [4]. Many CMOS/BiCMOS OCAs have been fabricated and studied based on slot, dipole, folded dipole, Yagi, patch and inverted-F [5-10]. However, most OCAs perform poor radiation efficiency due to the low resistivity and high permittivity of the lossy silicon substrate. Several techniques have been

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reported to improve the radiation performance of OCAs, including micromachining, dielectric resonators antennas (DRAs), artificial magnetic conductor (AMC) concept. However, these design methods increase the design complexity and are usually costly. Substrate integrated waveguide (SIW) technique has been widely used in printed circuit board antenna designs. SIW cavity-backed antenna is a good candidate for silicon-based integrated systems [8]. In Ref. [8], a 340 GHz single antenna and a 2 × 2 antenna array are designed using SIW cavity-backed slot-loaded magnetic loop structure in 0.13 μm SiGe BiCMOS technology. The maximum gains of the antenna element and array are 3.3dBi and 7.7 dBi, respectively. In Ref. [11], an SIW slot antenna is designed in 0.13 μm SiGe BiCMOS technology and achieves a gain of −0.5 dBi at 410 GHz.

In this paper, a 340-GHz cavity-backed on-chip patch antenna is presented. The proposed antenna is fabricated using standard 0.13-μm SiGe BiCMOS technology without any postprocesses. The patch is fed by a strip line placed at LY layer and some rows of vias from LY to AM layer. A backed cavity is designed to improve the impedance bandwidth and the radiation performances of the antenna. The cavity is formed by the top metal layer (AM) connected to the bottom metal layer (M1) through vias in between. The proposed antenna shows a simulated impedance bandwidth of 9.2 GHz from 335.6 to 344.8 GHz for S_{11} less than −10 dB. The simulated gain of the antenna at 340 GHz is 3.2 dBi.

1　Antenna Design

Fig. 1 illustrates the chip environment used in this design. There are seven metal layers over the silicon substrate. The inter-metal dielectric is SiO_2 with a relative permittivity of 4.1 and a loss tangent of 0.002 3 at 340 GHz [12]. The total thickness from the top metal layer (AM) to the bottom metal layer (M1) is around 17.12 μm. The silicon substrate has the thickness of 250 μm. Above AM, there is a passivation layer with a thickness of 4.3 μm. The geometry of the proposed OCA is presented in Fig. 2. The patch is placed on the topmost metal layer (AM). An annular ring slot is etched on AM layer. The M1 layer is used as ground plane. A coplanar waveguide (CPW) structure is designed for antenna measurement. The feeding strip line placed at LY layer is connected to the CPW input by a transition as shown in Fig. 2 (c). At the end of the strip line, eleven rows of vias from LY to AM are designed to feed the patch, which improves the impedance matching of the antenna. The SIW cavity is formed by the top metal layer (AM) connected to the bottom metal layer (M1) through vias in between.

Fig. 3 illustrates three different antennas: (1): patch antenna; (2): patch antenna with annular slot; (3): patch antenna with annular slot and backed cavity (proposed antenna). The simulated results of reflection coefficient for these three antennas are shown in Fig. 4. It can be observed that another higher resonant frequency at 343.7 GHz is generated by introducing the SIW backed cavity structure. The additional higher frequency resonance, in combination with the original lower one at

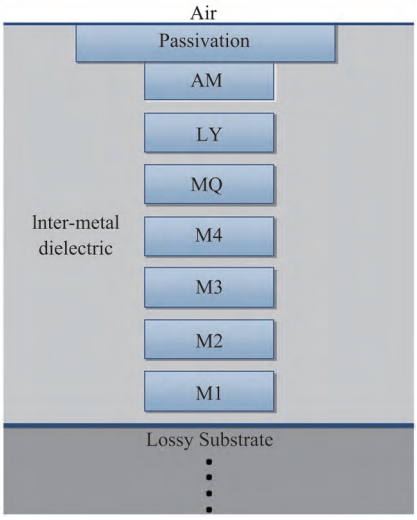

Fig. 1　Lateral view of chip environment
图 1　工艺中的金属和介质结构示意图

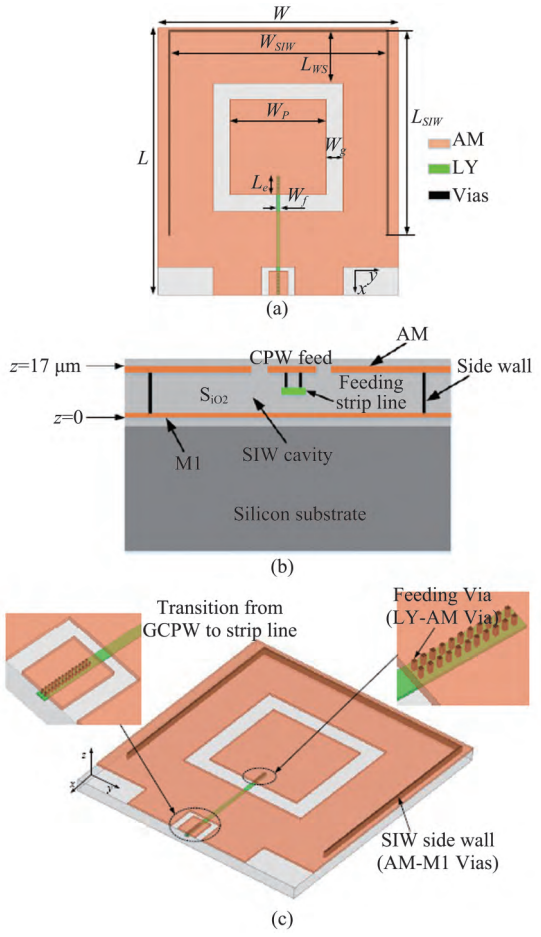

Fig. 2　The geometry of the proposed antenna (not to scale), (a) Top view of the antenna, (b) Side view of the antenna, (c) 3-D view of the antenna
图 2　天线结构图(a)俯视图(b)侧视图(c)立体结构图

337.6 GHz of the patch mode, broadens the bandwidth

of the antenna. E-field distributions of the proposed antenna at 337.6 GHz, 343.7 GHz are illustrated in Fig. 5. Fig. 5(a), (c) show the E-field distributions at 337.6 GHz on planes $z=17$ μm and $z=10$ μm, respectively. It is observed that the field distributions at the lower resonant frequency is actually the TM_{10} mode of the patch antenna. Fig. 5(b), (d) show the E-field distributions at 343.7 GHz on planes $z=17$ μm and $z=10$ μm, respectively. The field distributions at the higher resonant frequency is the TE_{110} mode of the cavity.

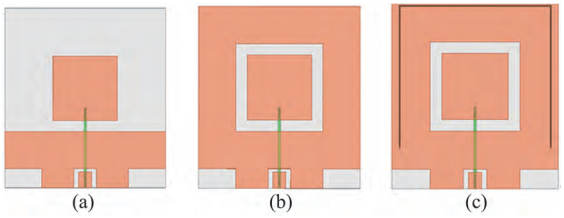

Fig. 3 Three different antennas, (a) Antenna 1: patch antenna, (b) Antenna 2: patch antenna with annular slot, (c) Proposed antenna

图3 三款不同天线(a)天线1:贴片天线,(b)天线2:加载环缝隙的贴片天线,(c)本文中最终设计的背腔贴片天线

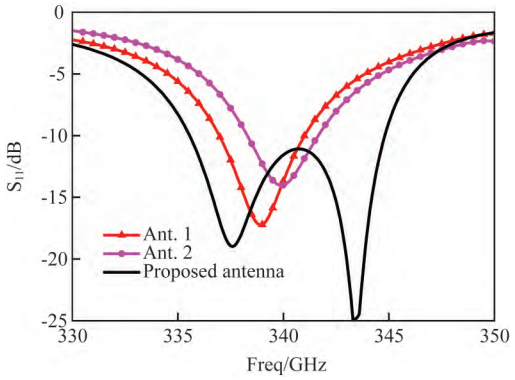

Fig. 4 Simulated reflection coefficients of three different antennas

图4 三款天线的 S_{11} 仿真结果

The width of the cavity W_{SIW} and the gap between annular ring slot and SIW side wall along x-direction L_{WS} are two key parameters for tuning the antenna. Fig. 6 (a) and (b) present the behaviors of the two resonances as W_{SIW} and L_{WS} change, respectively. As shown in Fig. 6 (a), the higher resonant frequency shifts down to lower frequency while W_{SIW} increases (other parameters keeping unchanged), which degrades the impedance matching at the lower resonant frequency. Similar conclusion can be got from Fig. 6 (b) as L_{WS} increases. The above simulated results and analyses prove that we can optimize the dimensions of the backed cavity structure to tune the higher frequency resonance. It`s noted that the width of the annular slot W_g is also a key parameter to tune the two resonances and the impedance bandwidth in antenna design.

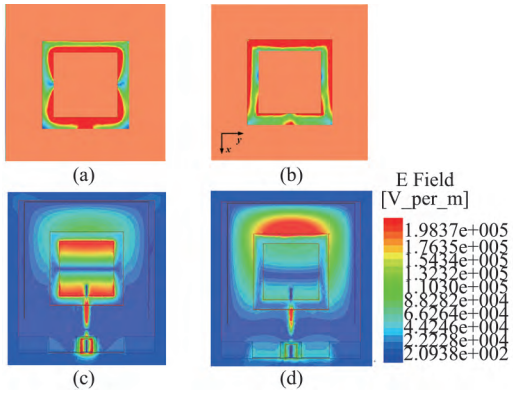

Fig. 5 Simulated E-filed distributions of the proposed antenna, (a) 337.6 GHz ($z=17$μm), (b) 343.7 GHz ($z=17$μm), (c) 337.6 GHz ($z=10$μm), (d) 343.7 GHz ($z=10$μm)

图5 天线电场分布仿真结果(a)337.6 GHz ($z=17$μm),(b)343.7 GHz ($z=17$μm),(c)337.6 GHz ($z=10$μm),(d)343.7 GHz ($z=10$μm)

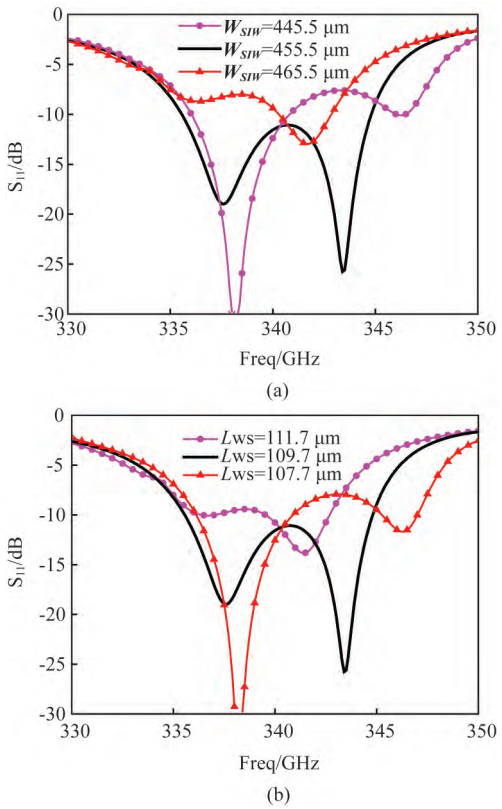

Fig. 6 (a) Reflection coefficients of antennas with different W_{SIW}, (b) Reflection coefficients of antennas with different L_{WS}

图6 (a)不同 W_{SIW} 对应天线 S_{11} 仿真结果,(b)不同 L_{WS} 对应天线 S_{11} 仿真结果

As shown in Fig. 2(c), eleven rows of feeding vias are placed at the end of the feeding stripline to feed the patch. Fig. 7 illustrates the reflection coefficients with

and without feeding vias. It is observed that these feeding vias improve the impedance matching of the antenna. It is noted that the positions of two resonances are hardly influenced by the existence of the feeding vias. Fig. 8 shows antennas with N ($N=1, 2, 6$) rows of feeding vias. The illustration for $N=11$ can be seen in Fig. 2(c). Antennas with different N are simulated and the simulated reflection coefficient results are shown in Fig. 9. The impedance matching of the antenna improves as the number of rows increases. The optimized dimensions of the proposed antenna are listed in Table 1.

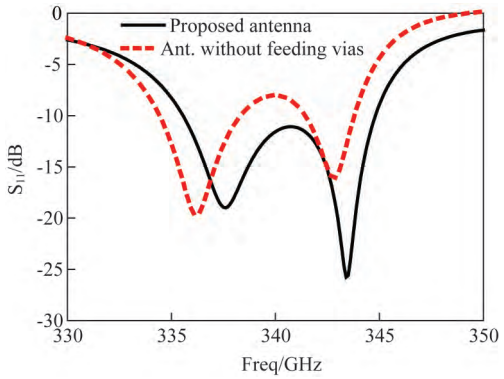

Fig. 7　Reflection coefficients of antennas with and without feeding vias

图 7　有、无馈电金属过孔时对应天线的 S_{11} 仿真结果

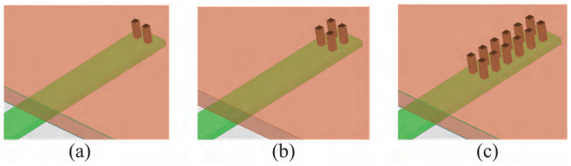

Fig. 8　Antennas with N rows of feeding vias. (a) $N=1$, (b) $N=2$, (c) $N=6$

图 8　不同金属过孔排数 N 对应示意图(a) $N=1$, (b) $N=2$, (c) $N=6$

Table 1　Optimized dimensions of the proposed antenna (unit: μm)

表 1　经优化的各天线参数值 (单位: μm)

Parameters	W	L	W_{SIW}	L_{SIW}	L_{ws}	W_p	W_g	L_e	W_f
Value	500	560	455.5	429.5	109.7	200	35	40	8

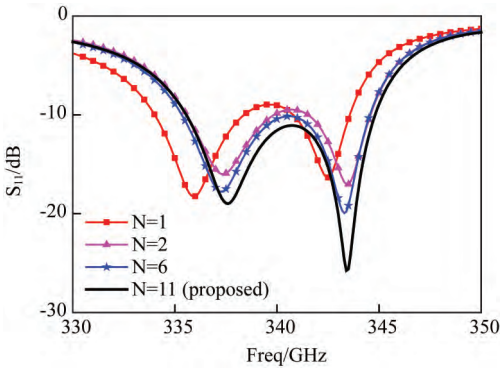

Fig. 9　Reflection coefficients of antennas with different rows of feeding vias

图 9　不同金属过孔排数 N 对应天线 S_{11} 仿真结果

2　Results and discussions

Fig. 10 presents the micrograph of the proposed antenna. The antenna was measured with the setup shown in Fig. 11. The fabricated antenna is measured based on the Cascade Microtech Elite-300 probe station and Keysight PNA-X (N5247A) with the VDI extender providing the signal source from 220 ~ 330 GHz. Due to the limitations of the highest measurement range of the vector network analyzer (VNA), which reach to 330 GHz, only the frequencies of S_{11} lower than 330 GHz were obtained. The measured and simulated reflection coefficients of the proposed antenna are presented in Fig. 12. It is observed that the simulated -10 dB impedance bandwidth are 9.2 GHz from 335.6 to 344.8 GHz. The measured -10 dB impedance bandwidth starts from 327.8 GHz while the simulated one starts from 335.6 GHz. Considering such a high operating frequency, a 2.3% deviation of about 7.8 GHz between the simulated starting frequency and the measured starting frequency is acceptable. It can be estimated that the measured result agrees well with the simulated one based on the available data. The discrepancy between the simulated results and measured results mainly results from measurement setup and the deviation of the silicon substrate characteristics setting in the simulation from its actual values. Fig. 13 shows the simulated gain patterns in *xoz*-plane and *yoz*-plane at 340 GHz. The simulated gain at 340 GHz is 3.2 dBi. As shown in Fig. 14, the maximum simulated radiation effi-

Table 2　Performance comparison with reported works

表 2　本文设计天线与其他文献中天线性能对比

Ref.	Type	Process	BW	Freq. (GHz)	Gain (dBi)	Radiation efficiency	Area (mm^2)
[2]	AMC-based open-loop	0.18 μm CMOS	28.3% (AR BW)	65	-4.4 (Measured)	n. a.	1.8×1.8
[3]	Cavity-backed slot loop	0.13 μm SiGe BiCMOS	4%	340	3.7	48% (Simulated)	0.7×0.7
[5]	Slot	0.09 μm CMOS	13.8%	60	-2.1(Simulated)	19.6% (Simulated)	1.3×1.1
[6]	Dipole	0.13 μm SiGe HBT with BiCMOS9 backend	>25%	160	< -7 (Simulated)	n. a.	0.5×0.5
[8]	Yagi	0.18 μm CMOS	16.7%	60	-10.6 (Measured)	10% (Simulated)	1.1×0.95
[9]	Patch	0.045 μm CMOS	n. a.	410	5 (Simulated Directivity)	50% (Simulated)	0.2×0.2 (Patch size)
[10]	Inverted-F	Post-back-end-of-line	20.4%	61	-19 (Measured)	3.5% (Simulared)	n. a.
[11]	SIW slot	0.13 μm SiGe BiCMOS	n. a.	400	-0.5 (Simulated)	49.8%	n. a.
This work	Cavity-backed Patch	0.13 μm SiGe BiCMOS	2.7%	340	3.2 (Simulated)	56.7% (Simulated)	0.5×0.56

ciency is 56.7% at 340 GHz.

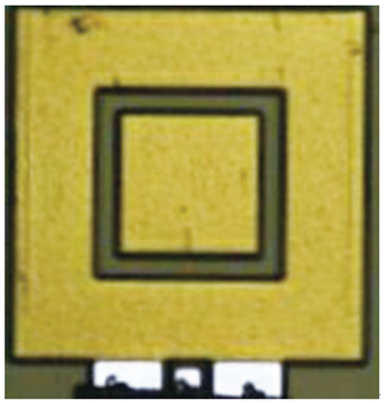

Fig. 10 Micrograph of the proposed antenna
图 10 天线实物照片

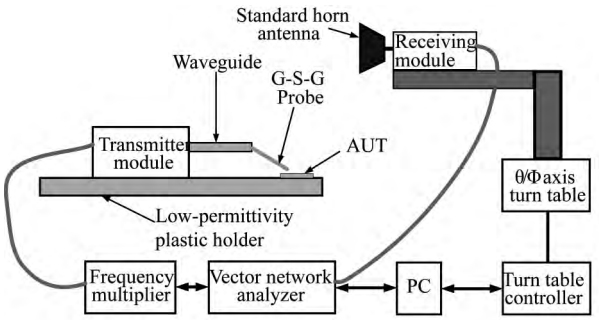

Fig. 11 Schematic diagram of the measurement setup
图 11 天线测试设置示意图

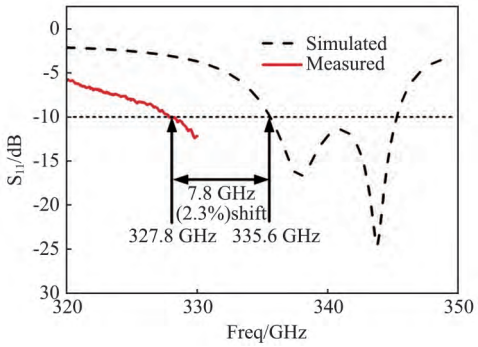

Fig. 12 Measured and simulated reflection coefficients of the proposed antenna
图 12 天线测试与仿真 S_{11} 结果

Table 2 lists the performance comparison of the proposed antenna with the reported works. It can be seen that the proposed antenna enhanced the gain and radiation efficiency using SIW backed cavity without any post process. The proposed antenna also achieves higher gain and radiation efficiency

3 Conclusions

This paper presents a study of the performance of an on-chip cavity-backed patch antenna designed and fabricated with 0.13 μm SiGe BiCMOS process. The square

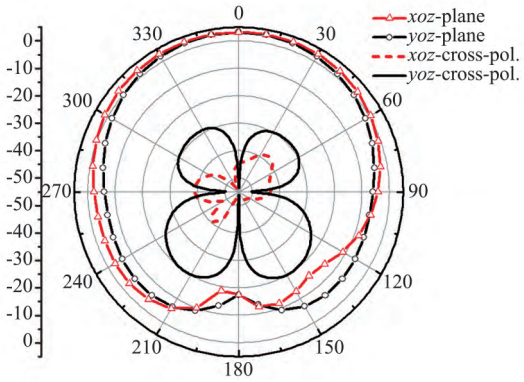

Fig. 13 Simulated gain patterns at 340 GHz of the proposed antenna
图 13 天线在 340 GHz 处的仿真方向图

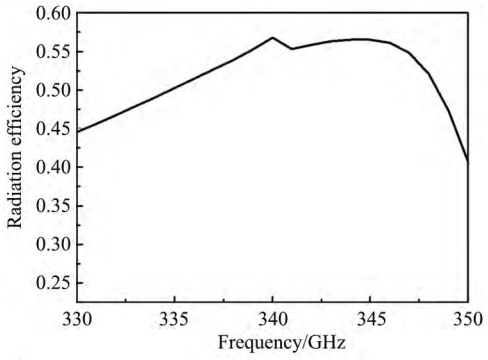

Fig. 14 Simulated radiation efficiency of the proposed antenna
图 14 天线仿真辐射效率

patch is placed at AM layer fed by a strip line placed at LY layer and some rows of vias from LY to AM layer. An SIW backed cavity is designed to improve the impedance bandwidth and the radiation performances of the antenna. The proposed antenna shows a simulated impedance bandwidth of 9.2 GHz from 335.6 to 344.8 GHz for S_{11} less than −10 dB. The simulated gain of the antenna at 340 GHz is 3.2 dBi. The total area of the antenna is 0.5 × 0.56 mm^2.

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艺开发的时间和费用,为红外探测器的版图设计提供参考. 在刻蚀速度公式和离子阴影效应的共同作用下,碲镉汞的刻蚀轮廓呈 V 形. 在获得了其它材料的刻蚀速度之后,还可以对其它材料的离子束刻蚀轮廓进行模拟. 对掩膜的刻蚀轮廓演变进行了模拟,并给出了一个优化设计掩膜厚度的例子.

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(上接第 314 页)

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