第36卷第2期 2017年4月
红外与毫米波学报
J. Infrared Millim. Waves
Vol. 36, No. 2 April, 2017

文章编号: 1001 -9014(2017)02 -0167 -06
DOI:10.11972/j.issn.1001 -9014.2017.02.008

0.5 μm InP DHBT technology for 100 GHz + mixed signal integrated circuits

CHENG Wei*, ZHANG You-Tao, WANG Yuan, NIU Bin, LU Hai-Yan, CHANG Long, XIE Jun-Ling

(Science and Technology on Monolithic Integrated Circuits and Modules Laboratory, Nanjing Electronic Devices Institute, Nanjing, 210016, China)

Abstract: A high performance 3-inch 0.5 μm InP double heterojunction bipolar transistor (DHBT) technology with three interconnect layers has been developed. The epitaxial layer structure and geometry parameters of the device were carefully studied to get the needed performance. The 0.5 μm × 5μm InP DHBTs demonstrated f_t = 350 GHz, f_{max} = 532 GHz and BV_{CEO} = 4.8 V, which were modeled using Agilent-HBT large signal model. Static and dynamic frequency dividers designed and fabricated with this technology have demonstrated maximum clock frequencies of 114 GHz and 170 GHz, respectively. The ultra high speed 0.5 μm InP DHBT technology offers a combination of ultra high speed and high breakdown voltage, which makes it an ideal candidate for next generation 100 GHz + mixed signal integrated circuits.

Key words: InP, heterojunction bipolar transistor, frequency divider
PACS: 85.30.De, 71.55.Eq

面向100 GHz+数模混合电路的0.5 μm InP DHBT工艺

程 伟*, 张有涛, 王 元, 牛 斌, 陆海燕, 常 龙, 谢俊领

(南京电子器件研究所 微波毫米波单片集成和模块电路重点实验室,江苏 南京 210016)

摘要:报道了一种高性能的3英寸磷化铟双异质结双极型晶体管工艺.发射极尺寸为0.5 μm×5 μm的磷化铟双异质结双极型晶体管,电流增益截止频率以及最高振荡频率分别达到350 GHz以及532 GHz,击穿电压4.8 V.基于该工艺研制了114 GHz静态分频器以及170 GHz动态分频器两款工艺验证电路,这两款电路的工作频率均处于国内领先水平.

关 键 词:磷化铟;异质结双极型晶体管;分频器

中图分类号:TN322+.8 **文献标识码**:A

Introduction

The combination of ultra high speed and high breakdown voltage makes InP double heterojunction bipolar transistors (DHBTs) particularly suitable for high speed mixed signal ICs and sub-MMW MMICs (s-MMICs). To date, several outstanding circuits have been demonstrated in InP DHBT technology, including static frequency dividers with an operating frequency above 200 GHz[1] and 210 GHz power amplifiers with an output power above 200 mW[2]. For mixed signal ICs, the static frequency divider and dynamic frequency divider are usually used as benchmark circuits for a given device technology. Prior to this work, the highest reported clock rates for the static frequency divider and dynamic frequency divider in an InP DHBT technology were both 100 GHz in China[3-5].

In this paper, we report on the development of a 0.5μm InP DHBT technology, optimized for the fabrication of 100 GHz + clock mixed signal ICs. The 0.5 μm InP DHBTs were modeled using Agilent-HBT (AHBT) large signal models. A static frequency divider and a dynamic frequency divider were fabricated with maximum clock frequencies of 114 GHz and 170 GHz, respectively.

Received date: 2016-04-05, **revised date**: 2016-12-13 **收稿日期**:2016-04-05, **修回日期**:2016-12-13
Foundation items: Supported by the Natural Science Foundation of Jiangsu Province of China (BK20131072)
Biography: CHENG Wei, male, Shandong, China. Ph. D. Research fields focus on InP HBTs and ICs.
* **Corresponding author**: E-mail: dspbuilder@163.com

1 Design and fabrication

The InP DHBT structure was grown using molecular beam epitaxy (MBE) on a 3-inch semi-insulating InP substrate. The InP DHBT epitaxy structure is given in Table 1, which consists of a thin highly carbon-doped InGaAs base to reduce the base contact resistivity. A base contact resistivity of 3.9 Ω-μm^2 was extracted from Transmission Line Model (TLM) measurement on fabricated InP DHBT wafers. A composite collector including an InGaAs setback layer and an InP pulse doping layer was used to eliminate the conduction band spike at the base-collector interface. The more detailed design and optimization methods of the composite collector can be found in Ref. [6].

Table 1 InP DHBT epitaxial layer structure

表1 InP DHBT 外延层结构

Layer	Material	Thickness/nm	Dopant
Emitter Contact	InGaAs	200	Si
Emitter	InP	200	Si
Base	InGaAs	35	C
Set-back	InGaAs	30	Si
δ- doping	InP	20	Si
Collector	InP	150	Si
Collector Contact	InGaAs	50	Si
Sub-collector	InP	200	Si
Etch-stop	InGaAs	10	ud
InP substrate			S. I.

According to the scaling laws of bipolar transistors, increasing the InP DHBT bandwidth requires both vertical scaling of the epitaxy layer and lateral scaling of the transistor junction dimensions. For this reason, besides the vertical layer structure optimization, the horizontal geometry scaling was also carefully studied in order to reduce the resistive and capacitive parasitics, which were very important to improve the high frequency performances of the HBTs, such as the maximum current gain cutoff frequency (f_t) and maximum power gain cutoff frequency (f_{max}). Figure 1 illustrates key geometry parameters of an InP DHBT, including emitter contact width (W_{EC}), emitter contact length (L_{EC}), base contact width (W_{BC}), base contact length (L_{BC}), emitter mesa undercut (W_{BE}) and collector contact width (W_{CC}). Figure 2 shows the expected f_{max} versus some key geometry parameters. The geometry parameters of the device were carefully designed and optimized under the guidance of these relationships.

The InP DHBTs were fabricated using a wet-etch triple mesa process. I-line photolithography was used for all photolithographic process steps. Metal posts on base and collector metals were used to make their heights at the same level as that of emitter contact. Thin film NiCr resistor and SiN MIM capacitor fabricated on the InP substrate were used as passive components. BCB was used for device passivation and planarization. The low permittivity dielectric of BCB was also used as the low-loss interlayer dielectric between the three level metals. In addition, the second metal or the third metal could also be used as the ground plane to form the inverted microstrip environment. The cross section of the 0.5 μm InP DHBT device is shown in Fig. 3.

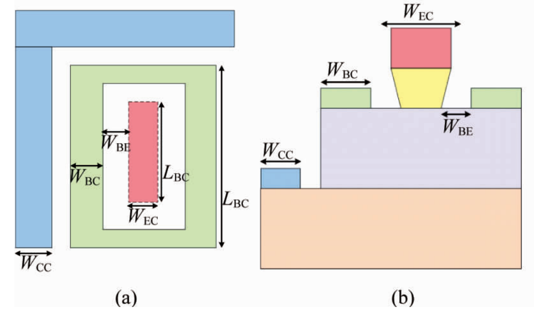

Fig. 1 Key geometry parameters of an InP DHBT: (a) top view, (b) cross section

图1 InP DHBT 器件特征尺寸:(a)俯视图,(b)剖面图

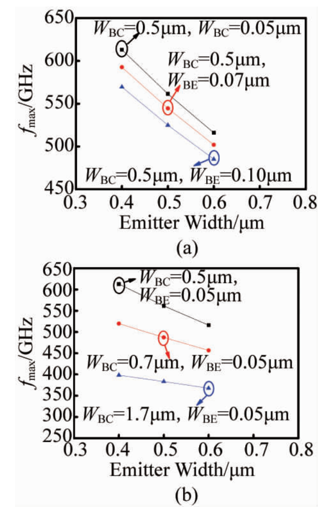

Fig. 2 Simulated f_{max} versus some key geometry parameters: (a) W_{EC} and W_{BE}, (b) W_{EC} and W_{BC}

图2 f_{max}随器件特征尺寸变化曲线:(a) W_{EC}和 W_{BE},(b) W_{EC}和 W_{BC}

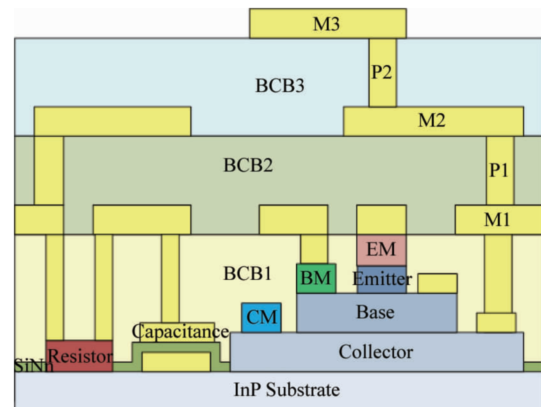

Fig. 3 Cross-section of the 0.5 μm InP DHBT device

图3 0.5 μm InP DHBT 工艺剖面图

The Agilent-HBT model was used for modeling large signal of the InP DHBTs. This model takes into account various unique properties of InP DHBTs, such as collector transit time modulation with applied bias, base-collector current blocking at high collector currents. Some key parameters values of the InP DHBT model are summarized in Table 2. R_E is the emitter resistance of the InP DHBT. R_{CI} and R_{CX} are the intrinsic and extrinsic collector resistances, respectively. R_{BI} and R_{BX} are the intrinsic and extrinsic base resistances, respectively. C_{je} is the base-emitter capacitance and C_{jc} is the base-collector capacitance. Good agreements between measured and modeled S-parameters were achieved, as shown in Fig. 4. The large signal model was then employed in the design of static and dynamic dividers.

Table 2 Key parameters of the InP DHBT model
表 2 InP DHBT 模型关键参数

Parameter	Value	Units
R_E	4.27	Ohm
R_{CI}	2.03	Ohm
R_{CX}	0.49	Ohm
R_{BI}	25.24	Ohm
R_{BX}	2.40	Ohm
C_{je}	15.49	fF
C_{jc}	36.76	fF

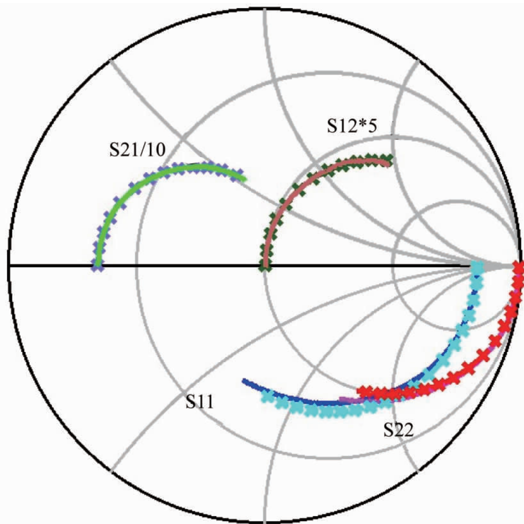

Fig. 4 Modeled (lines) versus measured (cross symbols) S-parameters
图 4 大信号模型仿真与实测结果对比 S 参数

A static frequency divider and a dynamic frequency divider were designed as demonstration ICs for the 0.5 μm InP DHBT technology, which were both highly optimized to obtain peak performances. The dividers were implemented with emitter-coupled-logic (ECL) topology, which could reduce the gate delay compared with the current-model-logic (CML) topology. The emitter followers were inserted between the master and slave latches in order to implement impedance transformation and provide appropriate bias for the transistor to obtain the best speed performance. Moreover, in order to maximize the speed and bandwidth of the dividers, peaking inductors were added in series with the load resistances to decrease the transition time. The input and output of the dividers were all designed to be single-ended interfaces for convenient measurement, and the interface circuitry of the divider core was carefully designed to avoid affecting performance of the divider core. The layout of the divider is a very important phase during the whole design. A compact layout could reduce the parasitic capacitance and inductance effectively, which would slow down the divider obviously. A dense wiring scheme and a thin film microstrip line environment were used to reduce the interconnect delays and maintain the signal integrity. Moreover, some key transmission lines were simulated in the ADS momentum to take into account both the transmission line effect and signal integrity. Figure 5 illustrates the simplified schematics of the static and dynamic frequency dividers. The maximum simulated toggle rates for the static and dynamic dividers are 140 GHz and 212 GHz, respectively.

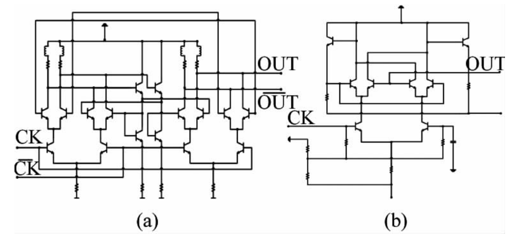

Fig. 5 Simplified schematic of the divider core: (a) static divider, (b) dynamic divider
图 5 分频器核心原理图:(a)静态分频器,(b)动态分频器

2 Measurement and discussion

After fabrication, measurements for the InP DHBTs were performed at room temperature. The microscope picture of the InP DHBT is shown in Fig. 6, the area of the single emitter finger is 0.5 μm × 5 μm and the base contact width is 0.5 μm at each side of the emitter. The DC characteristics of the fabricated InP DHBTs were measured using B1500 semiconductor parameter analyzer. Common-emitter current-voltage characteristics of an InP DHBT with an emitter area of 0.5 μm × 5 μm are shown in Fig. 7. The current gain (β) is 33 and the common-emitter breakdown voltage (BV_{CEO}) is 4.8 V. The offset and the knee voltages are 0.1 V and 0.5 V, respectively. The small knee voltage and sharp current rising indicate that the current blocking effect has been successfully suppressed by the composite collector[7].

On-wafer small-signal RF performance was measured with N5247A vector network analyzer from 0.2 to 67 GHz after performing a standard short-open-load-through (SOLT) calibration. On-wafer short and open pad structures identical to those used by the InP DHBTs were measured to deembed the pad parasitics. Figure 8 shows the measured current gain (H_{21}), maximum stable/available gain (MSG/MAG) and Mason's unilateral

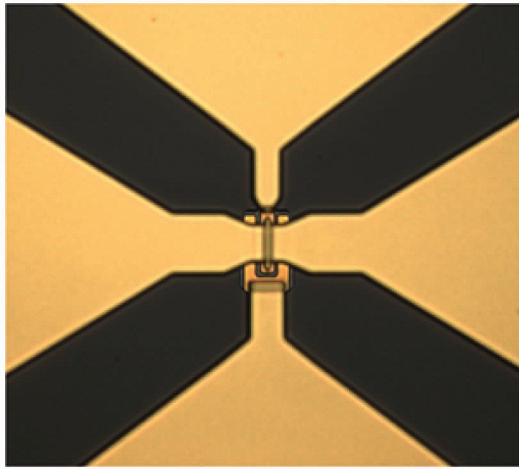

Fig. 6 Microscope picture of a 0.5 μm×5 μm DHBT
图6 0.5 μm×5 μm DHBT 器件显微镜照片

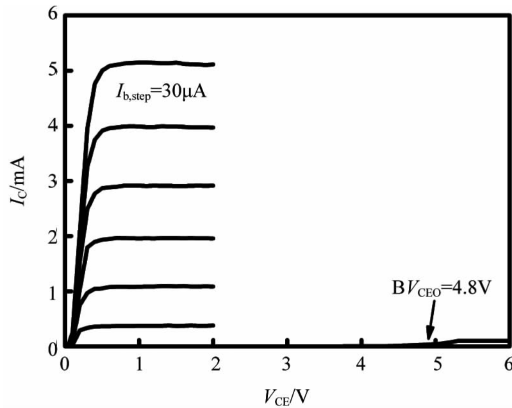

Fig. 7 Common-emitter current-voltage characteristics of a 0.5 μm×5 μm DHBT
图7 发射极面积0.5 μm×5 μm DHBT 器件 *I-V* 特性曲线

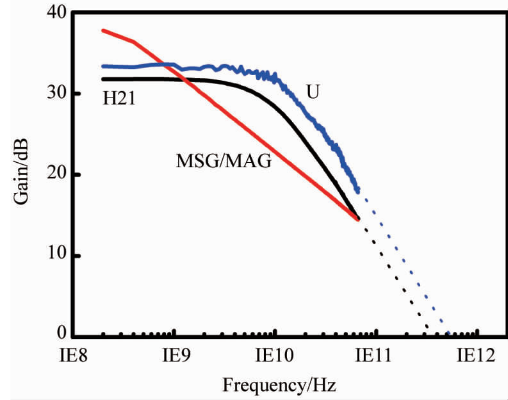

Fig. 8 H_{21}, MSG/MAG and U for a 0.5 μm×5 μm DHBT versus frequency at V_{CE} = 1.5 V and I_C = 11 mA
图8 发射极面积0.5 μm×5 μm DHBT 器件 H_{21}, MSG/MAG 以及 U 随频率变化曲线

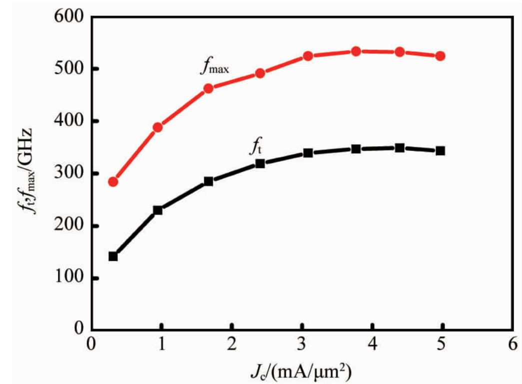

Fig. 9 Extrapolated f_t and f_{max} of a 0.5 μm×5 μm DHBT versus J_c at V_{CE} = 1.5 V
图9 发射极面积0.5 μm×5 μm DHBT 器件 f_t 以及 f_{max} 随电流密度变化曲线

Gain (U) as functions of frequency of a 0.5 μm×5 μm InP DHBT. The small jitter of the measured U was caused by the resonant hole modulation[8]. f_t and f_{max} were extracted from the measured H_{21} and U by using a -20 dB/decade slope, respectively, at a bias condition of V_{CE} = 1.5 V and I_C = 11 mA. The extrapolated f_t and f_{max} of a 0.5 μm×5 μm InP DHBT are 350 GHz and 532 GHz, respectively. Figure 9 shows variation of f_t and f_{max} versus collector current density (J_c) at V_{CE} = 1.5 V and the Kirk effect is observed at a J_c of 4.8 mA/μm^2 when f_t falls to 95% of its peak value. Table 3 compares recently reported InP DHBTs in China.

Table 3 Comparison of InP DHBTs
表3 InP DHBT 性能比较

Refs.	Technology	f_t/GHz	f_{max}/GHz
[7]	1.6 μm InP DHBT	242	106
[9]	0.5 μm InP DHBT	-	416
[10]	1.0 μm InP DHBT	170	256
This wok	0.5 μm InP DHBT	350	532

After fabrication, the static and dynamic frequency dividers were measured at room temperature on a wafer probe station. A conventional 50 GHz CW source was used for low frequency measurement. Testing beyond 50 GHz in the V, W and D-bands was performed with combination of low frequency source and frequency multiplier modules. The output spectrum of the divider was measured by a 50 GHz spectrum analyzer. V-band or W-band harmonic mixer modules were used on the divider output when testing above 100 GHz or 150 GHz. The maximum clock rates achievable for the static frequency and dynamic frequency dividers were 114 GHz and 170 GHz, respectively. The maximum simulated toggle rates of the dividers were a little higher than those measured from the fabricated circuits, which was probably because that only some keys but not all of the transmission lines were taken into account during the circuit design process to reduce the time and complexity of the EM simulation. Moreover, the large signal model of the InP DHBT was implemented based on the measurement data from 200 MHz to 67 GHz, so there were some errors in the simulation results

especially in the frequency range beyond 67 GHz. Figures 10-11 illustrate the measured output spectra for the static and dynamic frequency dividers, respectively. Table 4 compares the performances of recently reported static and dynamic frequency dividers in China.

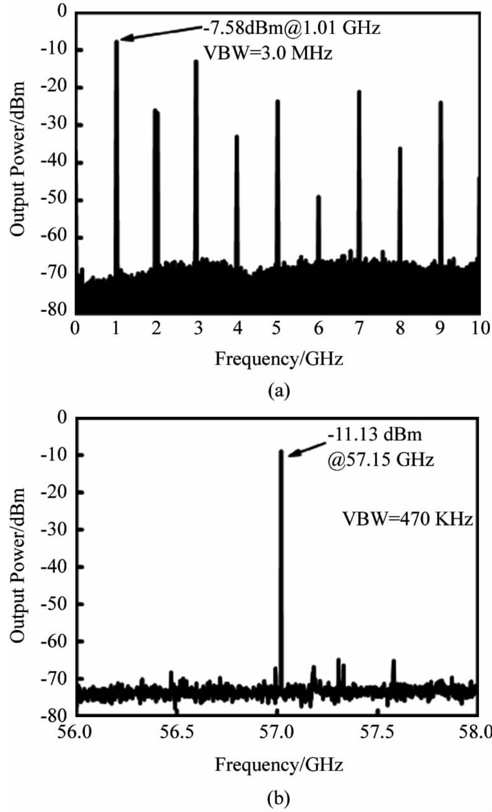

Fig. 10　Output spectra for the static frequency divider: (a) 2 GHz input, (b) 114 GHz input
图 10　静态分频器输出频谱:(a)输入频率 2 GHz,(b)输入频率 114 GHz

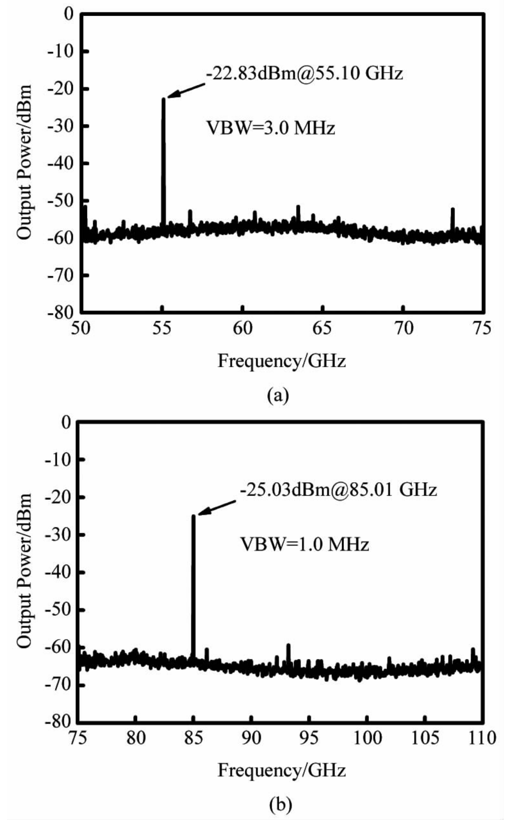

Fig. 11　Output spectra for the dynamic frequency divider: (a) 110 GHz input, (b) 170 GHz input
图 11　动态分频器输出频谱:(a)输入频率 110 GHz,(b)输入频率 170 GHz

Table 4　Comparison of InP DHBT static and dynamic frequency dividers
表 4　InP DHBT 静态和动态分频器性能比较

Refs.	Type	Technology	(f_t/f_{max}) /GHz	Max. operating freq./GHz	DC power /mW
[3]	Static	0.7 μm InP DHBT	280/280	83	350
[4]	Dynamic	1.0 μm InP DHBT	214/193	83	1 060
[5]	Static	1.4 μm InP DHBT	170/253	40	650
This wok	Static	0.5 μm InP DHBT	350/532	114	600
This work	Dynamic	0.5 μm InP DHBT	350/532	170	550

Although f_t and f_{max} could be used to describe the maximum operating frequency of the InP DHBT, they are of limited value in predicting the speed of the high speed mixed-signal ICs. In fact, static and dynamic frequency dividers are usually used as benchmark circuits for a given device technology. The propagation delay of the divider is dependent on the charging times of the parasitic capacitances and resistances encountered in the signal path, which could be calculated using the method of open circuit time constants (MOTC). The most significant delay part is $C_{cb}\triangle V_{logic}/Ic$, where C_{cb} is the capacitance of the base-collector junction, $\triangle V_{logic}$ is the logic swing of the circuit, and Ic is the collector current. Therefore, a small C_{cb} and a high current density are preferred to increase the digital circuit speed.

For the current density, as the current density increases, the mobile carriers modify the electric field profile. When the electron concentration in the base-collector depletion region exceeds the doping density of the collector, the electric field of the collector at the base side will reach zero, the Kirk effect thus occurs and the corresponding collector current density is Kirk current density (J_{Kirk}). The Kirk effect causes an additional electron barrier at the base-collector interface, which degrades the DC and RF performances of the InP DHBT. So the operating current density of the InP DHBT in the circuit should be close to but less than J_{Kirk}. The Kirk current density can be derived as follows:

$$J_{Kirk} = [2\varepsilon_s \nu_{eff}(V_{bi} + V_{cb} - \Delta E_C(T_s + T_g)/qT_g)]/T_C^2 + qN_C\nu_{eff} \quad (1)$$

ε_s is the dielectric constant of the semiconductor. N_C and T_C are the doping concentration and thickness of the collector. ν_{eff} is the effective velocity of the electrons in the collector, T_s is the thickness of the setback layer, V_{bi} is the built-in voltage of the base-collector junction and V_{cb} is the applied voltage. According to Eq. (1), the Kirk current is inversely proportional to the square of collector thickness, so a thinner collector is helpful to improve the current density. The thickness of the collector has been reduced from 250 nm in Ref. [3] to 200 nm in this study, which means that the current density will increase about 1.56 times that in Ref. [3] according to Eq. (1) and this is helpful to improve the speed of the mixed-signal circuit.

Base-collector capacitance (C_{cb}) is another critical factor limiting the speed of the mixed-signal circuit. C_{cb} could be derived as follows:

$$C_{cb} = \varepsilon_s A_{cb}/T_C = \varepsilon_s (2W_{BC} + W_{EC}) L_{BC}/T_C \quad , \quad (2)$$

A_{cb} is the base collector area. According to Eq. (2), C_{cb} is proportional to the base collector area, so a smaller base collector junction is helpful to reduce the base collector capacitance. The width of the emitter contact has been reduced from 0.7 μm in Ref. [3] to 0.5 μm in this study and the width of the base contact from 1.0 μm to 0.5 μm. By using smaller emitter and base contacts, the base collector area has been reduced about 45% resulting in a lower base-collector capacitance.

Conclusion

In summary, a 0.5 μm InP DHBT technology has been developed. A 0.5 μm × 5 μm emitter area device demonstrated f_t = 350 GHz, f_{max} = 532 GHz and BV_{CEO} = 4.8 V. A 114 GHz static frequency divider and a 170 GHz dynamic frequency divider were designed, fabricated and demonstrated with this technology. The 0.5 μm InP DHBT technology offers a combination of ultra high speed and high breakdown voltage, which makes it suitable for high performance digital and mixed signal applications.

References

[1] Griffith Z, Urteaga M, Pierson R, *et al*. A 204.8GHz Static Divide-by-8 Frequency Divider in 250nm InP HBT[C]. in *IEEE Compound Semiconductor Integrated Circuit Symposium* (Monterey, CA 3-6 Oct 2010), p. 1.

[2] Griffith Z, Urteaga M, Rowell P, *et al*. A 23.2 dBm at 210 GHz to 21.0 dBm at 235 GHz 16-way PA-cell combined InP HBT SSPA MMIC[C]. in *IEEE Compound Semiconductor Integrated Circuit Symposium*, *La Jolla*, *CA*. 19-22 Oct 2014, p. 1.

[3] Zhang Y, Li X, Zhang M, *et al*. A 83 GHz InP DHBT Static Frequency Divider [J]. *Journal of Semiconductors*, 2014, **35** (4), 045004.

[4] Zhong Y, Su Y, Jin Z, *et al*. An InGaAs/InP W-band dynamic frequency divider[J]. *Journal of Infrared and Millimeter Waves*, 2012, **31** (5): 393.

[5] Su Y, Jin Z, Cheng W. *et al*. An InGaAs/InP 40 GHz CML Static Frequency Divider [J]. *Journal of Semiconductors*, 2011, **32** (3): 035008.

[6] Cheng W, Jin Z, Yu J, *et al*. Design of InGaAsP composite collector for InP DHBT[J]. *Chinese Journal of Semiconductors*, 2007, **28**(6): 943.

[7] Cheng W, Jin Z, Su Y, *et al*. Composite-collector InGaAs/InP double heterostructure bipolar transistors with current-gain cut-off frequency of 242 GHz [J]. *Chinese Physics Letter*, 2009, **26**(3): 038502.

[8] Willen B, Rohner M, Schwarz V, *et al*. Experimental evaluation of the InP-InGaAs-HBT power-gain resonance[J]. *IEEE Electron Device Letters*, 2002, **23**: 579.

[9] Cheng W, Wang Y, Zhao Y, *et al*. A THz InGaAs/InP double heterojunction bipolar transistor with f_{max} of 416GHz[J]. *Research and Progress of Solid State Electronics*, 2013, **33**: F0003.

[10] Cheng W, Zhao Y, Gao H, *et al*. High breakdown voltage InGaAs/InP double heterojunction bipolar transistors with f_{max} = 256 GHz and BV_{CEO} = 8.3 V[J]. *Journal of Semiconductors*, 2012, **33**(1): 56.