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A 190 ~ 225 GHz high efficiency Schottky diode doubler with circuit substrate flip-chip mounted

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Abstract: A 190 ~ 225 GHz high multiplying efficiency frequency doubler was developed with discrete GaAs planar Schottky diode. The 50 μm thick quartz circuit substrate is flip-chip mounted for diode thermal dissipation, as well as RF signals and DC grounding effectively. Diode embedding impedances were calculated by full-wave analysis with lumped port to represent the nonlinear junction for circuit matching. The doubler is self-biasing and fix-tuned. The highest efficiency of 9.6% and corresponding output power of 8.25 mW were obtained at 202 GHz with pumping power of 85.5 mW. The typical tested efficiency is 7.5% in 190 ~ 225 GHz. The multiplying efficiency features flat and broadband operation. The doubler reaches the state-of-the-art performance reported worldwide.

Key words: GaAs Schottky diode, frequency doubler, terahertz, efficiency
PACS: 84.30.Qi

基于倒扣技术的 190 ~ 225 GHz 肖特基二极管高效率二倍频器

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摘要:基于分立式 GaAs 肖特基势垒二极管,研制出了 190 ~ 225 GHz 高效率二倍频器.50 μm 厚石英电路利用倒扣技术,实现二极管的良好散热、可靠的射频信号及直流地.通过数值分析方法,二极管非线性结采用集总端口模拟,提取二极管的嵌入阻抗,以设计阻抗匹配电路.在 202 GHz,测得最高倍频效率为 9.6%,当输入驱动功率为 85.5 mW 时,其输出功率为 8.25 mW;在 190 ~ 225 GHz,测得倍频效率典型值为 7.5%;该二倍频器工作频带宽、效率响应曲线平坦,性能达到了国外文献报道的水平.

关 键 词:GaAs 肖特基二极管;二倍频器;太赫兹;效率

中图分类号:TN773.2 **文献标识码**:A

Introduction

Terahertz band spans the gap between the infrared and millimeter waves. This portion of electromagnetic spectrum has attracted great commercial and scientific interest. It can be used for a variety of applications, such as molecular spectroscopy, atmospheric remote sensing, sensing and monitoring of chemical and biological molecules. Until now, frequency multiplication is still a commonly applied solution to produce power at terahertz wave where the fabrication of fundamental oscillators and amplifiers are difficult[1-3]. Typically, a number of multiplier modules are cascaded to reach terahertz frequencies and the frequencies have been beyond 2.75 THz[4]. The multiplier modules are commonly based on Schottky diodes[7-14]. Transistor based MMIC multipliers are rapidly improved and have been demonstrated at millimeter wave frequencies[5-6].

In this letter, we present a high multiplying efficien-

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cy hybrid integrated balanced frequency doubler. The multiply circuit is flip-chip mounted for thermal dissipation, and RF signals grounding. This is because conventional applied beam leads have the problem of reliability and added parasitic parameters to RF signals grounding. The doubler features characteristics of self-biasing and fix-tuned. The highest efficiency of 9.6% and corresponding output power of 8.25 mW were measured at 202 GHz with pumping power of 85.5 mW. The typical tested efficiency is 7.5% in 190 ~ 225 GHz. The efficiency response is flat and broadband. This performance is comparable to the state-of-the-art results reported around 220 GHz.

1 Circuit Design

The most widely used frequency doubler topology at millimeter wave and terahertz frequency is Erickson style doubler[7]. Its core element is a balanced pair of diodes, which produces the even-order harmonic output signals, suppresses the odd-order harmonics, and isolates the input and output signals without using of distributed filters. The three dimensional physical structure was analyzed using high frequency structure simulator (HFSS). First, the diode is setup in HFSS and its S-parameters is exported for harmonic balance analysis (HBA) in advanced design system (ADS) to find optimum diode embedding impedances. Second, breaking up the doubler circuit into several parts, where each part is simulated and optimized individually. All passive networks including low pass filter, E-plane waveguide to microstrip transition, input and output matching networks, and diodes passive part are analyzed by EM simulators. The different parts are then combined and optimized together for required multiplying efficiency. Third, the exported S-parameters of the optimized complete circuit are used for harmonic balance analysis in ADS and the process is repeated before the ultimate requirement is reached[8].

1.1 Diode embedding impedances

The complete doubler circuit is described as Fig. 1, a flip-chip planar Schottky varactor chip with four diodes integrated in anti-series configuration is adopted, which can enhance the power handling capability due to the increasing number of the applied diode. The chip has a center pad that is soldered to the stripline on the quartz circuit, and two other pads are soldered directly to the quartz pad which is finally connected to waveguide block. The reverse bias is applied to the diodes from the center line. Input signals are out-of-phase to the diodes at different arm, the generated even harmonic signals are in-phase at output port, and the generated odd harmonic signals are out-of-phase and can not propagate to the output port. Therefore, the multiply circuit can realize balanced even-order harmonic frequency multiplication.

To accurately predict the optimum embedding impedances, the influence of the diode chip parasitic components should be considered. A full 3D EM simulation of the diode chip is analyzed with internal coaxial or lumped port to model the Schottky junction. The S-parameter file of the diode chip is exported for embedding impedances discussion in ADS. The diode Schottky junction is modeled with SPICE parameters (C_{jo} = 0.01 pF,

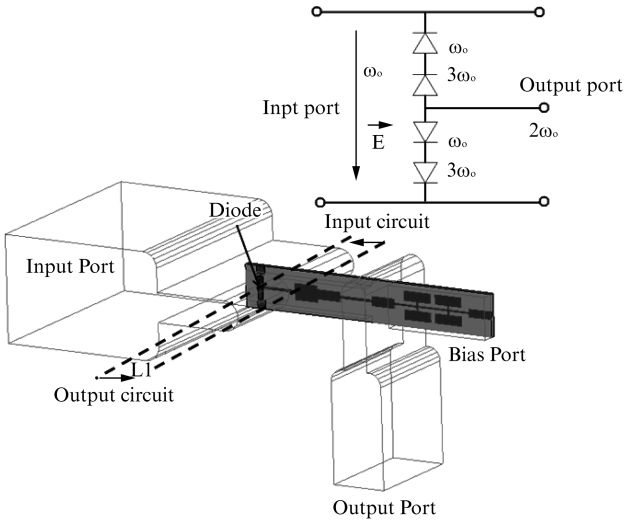


Fig. 1　Doubler complete model in HFSS
图 1　二倍频器 HFSS 电路模型

Is = 1.5 × 10^{-13} A, Rs = 5 Ω, n = 1.15). By running HBA in ADS, the diode optimum input pump frequency and output second harmonic frequency impedances are found. At 110 GHz, with pumping power of 80 mW, calculated diode optimum impedance to input frequency Z_{in} (f_p) and the second harmonic frequency Z_{out} (f_{2p}) is 21 − j × 46 and 14 − j × 34, respectively, the impedances is then used to synthesize the doubler circuit.

1.2 Thermal analysis

To increase diode power handling ability, several paths are applied simultaneously. The diode doping is optimized and the number of anodes per-chip is increased. The substrate layer is thinned to several microns and transferred to a high thermal conductivity AlN or diamond substrate. The diodes are fabricated by GaN to increase breakdown voltages and subsequently to increase the power handling capabilities of frequency multipliers. However, there is a practical limitation to the number of anodes, as the number of anodes is increased, compromising must be made between optimum input coupling to the anodes, optimum matching of each anode at the idler frequencies and optimum matching at the output frequency. Diodes fabricated with GaN have the problem of lower electron mobility than GaAs, therefore multiplying efficiency is lower than GaAs multipliers. In this paper, diodes thermal dissipation is discussed to improve the multiplying efficiency.

Two different approaches to mount the circuit substrate are presented in Fig. 2. In our designed doubler, the circuit is flip-chip mounted in block to improve thermal conduction dissipation. Compared with conventional mounting approach, the diode of flip-chip mounted circuit has the shortest conduction distance, and this approach can effectively improve RF signals grounding without adding parasitic. In the conventional way, the beam leads are clamped by the split block to realize RF signals grounding, which has the problem of assembling and reliability. The thermal conduction dissipation is the dominant heat transport mechanism. Therefore, the diode is soldered into quartz substrate with indium solder which has low thermal resistance.

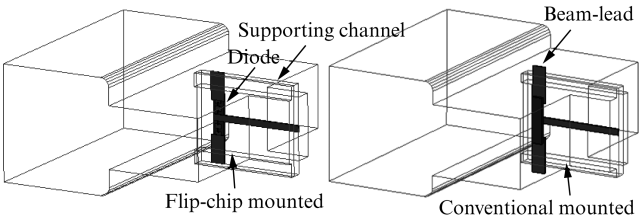
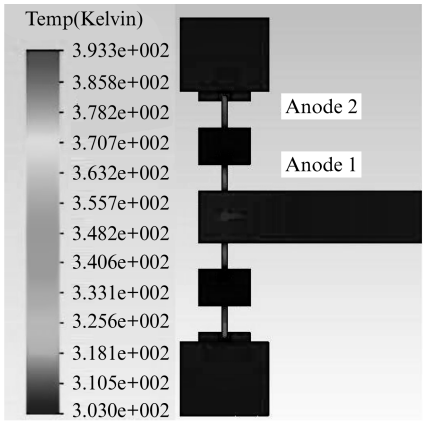
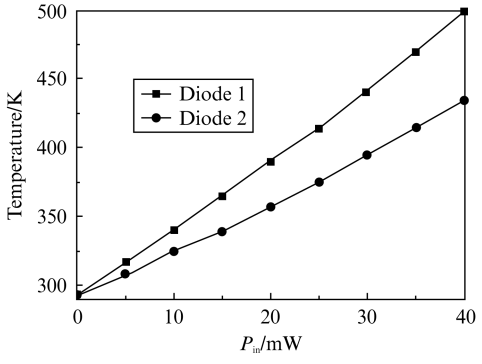


Fig. 2 Two different doubler circuit mounting approach
图2 二倍频电路不同安装方式

The input power is supposed equally applied to the four anodes for easy thermal analysis, and a 3-D thermal model in steady-state is analyzed with FEM. The applied grounding gold beam-leads size is 0.06 mm × 0.03 mm × 0.01 mm (width, length, height), which is the same width as the flip-chip mounting circuit pad. Figure. 3 ~ 4 shows the steady-state temperature distribution within the multiplier circuit and the anode junction. At input power of 20 mW to peranode, the highest diode junction temperature of conventional mounted way is about 393 K, with increasing of input power the temperature will elevate. While the circuit is flip-chip mounted, it can be found the highest temperature is about 371 K with the same power, the junction temperature is decreased about 22 K. They together show that the junction temperature response is almost linear as a function of power and the temperature differs between the anodes. The hottest spot is observed in anode 1 which is located farthest to the waveguide block. This is due to the distributed thermal

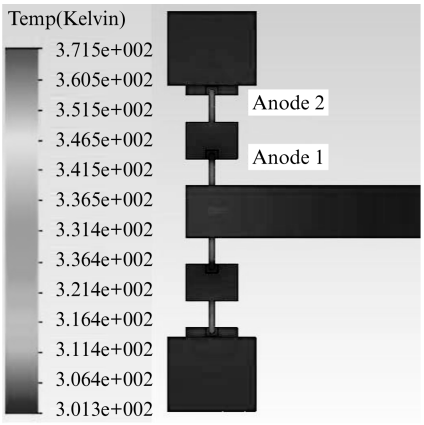


(a) Temperature distribution with 20 mW peranode

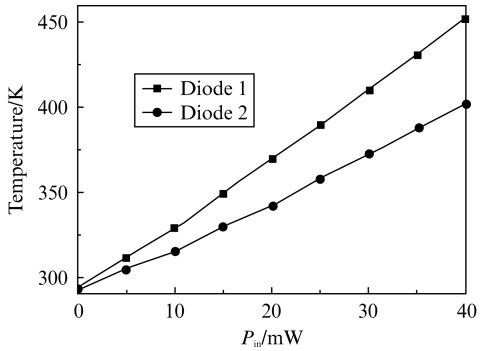


(b) Junction temperatures versus input power

Fig. 3 Circuit conventional mounted
图3 倍频电路传统安装方式



(a) Temperature distribution with 20 mW peranode



(b) Junction temperatures VS input power

Fig. 4 Circuit flip-chip mounted
图4 倍频电路倒扣安装方式

mass and the thermal coupling between adjacent anodes. It can be found that the flip-chip mounted doubler has lower temperature than that of conventional way, and the latter may have superior efficiency.

1.3 Circuit optimization

As described in Fig. 1, the diodes are in series across the input waveguide. The input signals will feed the anti-series diode array in a balanced mode (TE_{10}), and the input back short (L_1) is tuned for maximum transmission of pumping signals to diode, with following reduced-width of suspended stripline waveguide channel to sufficiently cut off the input TE_{10} mode. The output section consists of the waveguide-microstrip transition, and the suspended microstrip quartz circuit which is classified into two parts. The first part next to the varactor chip (L_1) is characterized by quasi-coaxial part, while the second part which forms the output embedding circuit is suspended strip line. The excited second harmonic is radiated in the unbalanced wave mode TEM, passes through the quasi-coaxial region, and then coupled into the output waveguide port with a succession of matching transmission line. Therefore, effective isolation between the input and the output radiations can be achieved due to the mode orthogonal[7]. Based on calculated impedance, the input and output circuit can be designed, respectively. The seven port S-parameters of the complete doubler circuit are extracted and combined with nonlinear diode to model the multiply efficiency.

2 Experimental results

The doubler circuit substrate is ultra thin quartz substrates with thickness of 0.05 mm, and the dielectric constant is 3.78. Two circuits are designed for flip-chip and conventional mounted respectively. The diodes and beam leads are soldered with indium solder into circuit substrate, and then the circuits are mounted to the split block with silver epoxy. The doubler block is manufactured by brass and electroplated with gold. The photos of two different doublers with flip-chip and conventional mounted modules are shown in Fig. 5.

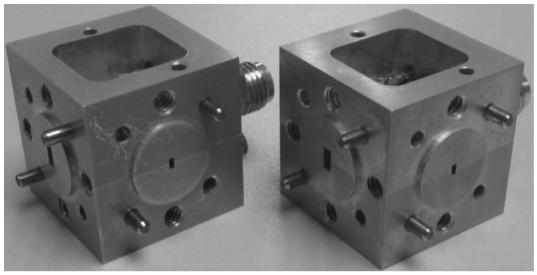


Fig. 5　Photo of the two different doublers
图 5　两种倍频器实物图

The doubler measurement setup is presented in Fig. 6. The input pumping power of doublers are provided by ELVA-1 BWO-W signal generator, and its output power has been precisely calibrated by millimeter and submillimeter power meter PM-4. For the flip-chip mounted doubler, the measured output power versus pumping frequency is given in Fig. 7, with input power of 80 ~ 100 mW in 95 ~ 112.5 GHz, the output power is higher than 5.0 mW and 7.0 mW in 190 ~ 200 GHz and 200 ~ 225 GHz, respectively. The highest measured efficiency of 9.6% and corresponding output power of 8.25 mW are measured at 202 GHz with pumping power of 85.5 mW. Figure 8 shows that the efficiency response is flat, and the typical tested efficiency is 7.5%. The agreement between simulations and measurements is excellent with maximum deviation of about 2%. This deviation maybe induced by mounting imbalance of diode chip and circuit, and diode model accuracy in simulations.

The circuit flip-chip mounted and conventional mounted doubler efficiency is presented in Fig. 9. Obviously, it can be found that the measured efficiency of the former doubler is superior, and the highest and typical

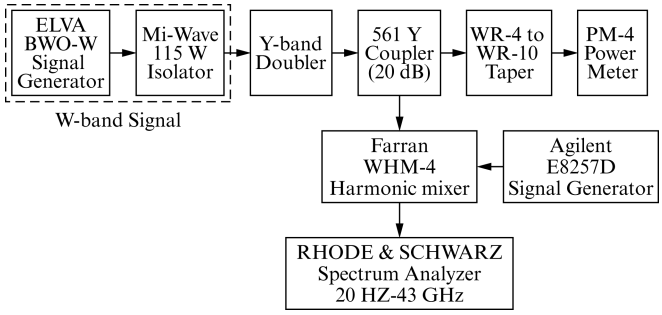


Fig. 6　Measurement setup of the doubler
图 6　二倍频器测试框图

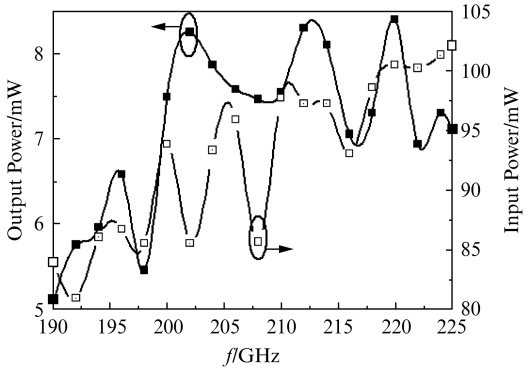


Fig. 7　Measured output power versus pumping power
图 7　倍频输出功率和驱动功率关系

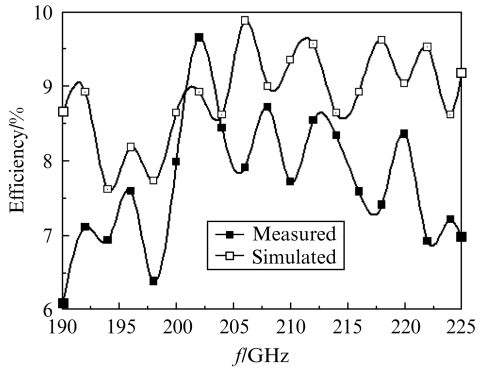


Fig. 8　Multiply efficiency
图 8　倍频效率

efficiency is higher about 3.5% and 3.0% than that of the latter, respectively. The flip-chip mounted doubler also shows superior flat response. It can be included that, with flip-chip mounted approach, the doubler can realize superior efficiency by improved thermal conduction and low added parasitic.

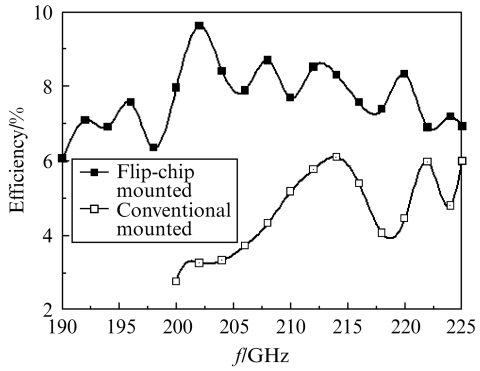


Fig. 9　Multiply efficiency with two different mounted approach
图 9　两种倍频器倍频效率

Table 1 illustrates some other reported multipliers. Compared with integrated diode doublers[9-13], the typical and highest performance of our multiplier with discrete diodes is superior, while the integrated diode technology is commonly applied for high efficiency and high frequency performance applications[9-10]. To the multipliers in paper[11-12], our multiplier has the advantage of broad

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bandwidth and high efficiency. While comparing with VDI commercial products[13], our typical efficiency is low about 2.5%, but our doubler design is more cost-effective with discrete diodes. The developed doubler achieves the state-of-the-art performance reported in abroad.

Table 1 Doubler performance comparison
表 1 二倍频器性能比较

References	Model	Diode style	Multiply factor	Frequency(GHz)	Multiply Efficiency(%)
This paper	—	Discrete	2	190 ~ 225	Typ 7.5, Max 9.6@202 GHz
[9]	—	Integrated	2	177 ~ 202	Typ 7.0, Max 9.0@188 GHz
[10]	—	Integrated	2	140 ~ 220	Typ 3.8, Max 6.4@204 GHz
[11]	—	Discrete	3	240	Max 2.5@252 GHz
[12]	—	Discrete	3	282	7@282 GHz
[13]	WR4.3 ×2	Integrated	2	170 ~ 250	Typ 10.0, Max 12.5@216 GHz

3 Conclusions

A high multiplying efficiency hybrid integrated balanced frequency doubler was developed. The circuit is flip-chip mounted to provide an improved thermal path for heat flow from the diodes to the metal waveguide block, and present an effective RF signals grounding without adding parasitic. The reliability and performance of the doubler is improved. The doubler operates at self-biasing and fix-tuned. The highest efficiency of 9.6% and corresponding output power of 8.25 mW are measured at 202 GHz with input power of 85.5 mW. The tested efficiency is between 6% and 9.6% in 190 ~ 225 GHz. The doubler efficiency response is flat and broad bandwidth. It is attractive for terahertz test instruments and transceiver systems.

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