第33卷第6期
2014年12月

红外与毫米波学报
J. Infrared Millim. Waves

Vol. 33, No. 6
December, 2014

文章编号:1001 - 9014(2014)06 - 0584 - 07

DOI:10.3724/SP. J. 1010. 2014. 00584

Millimeter-wave low power UWB CMOS common-gate low-noise amplifier

YANG Ge-Liang, WANG Zhi-Gong*, LI Zhi-Qun, LI Qin, LIU Fa-En, LI Zhu

(Institute of RF- & OE-ICs, Southeast University, Nanjing 210096, China)

Abstract: This paper presents an Ultra-wideband (UWB) low-noise amplifier (LNA) based on a single-ended common-gate (CG) in cascade with cascode configuration. The proposed LNA was implemented by a standard 90-nm RF CMOS technology. The measured flat gain is more than 10 dB from 28.5 to 39 GHz. The −3 dB bandwidth is 15 GHz from 27 to 42 GHz which covers almost the entire Ka band. The minimum noise figure (NF) is 4.2 dB, and the average NF is 5.1 dB within the 27 ~ 42 GHz range. The S_{11} is better than −11 dB over the overall testing band. The input 3rd-order intermodulation point (IIP3) is +2 dBm at 40 GHz. The DC power dissipation of the whole circuit is as low as 5.3 mW. The chip occupies an area of 0.58 mm × 0.48 mm including all pads.

Key words: millimeter-wave, wide-band, CMOS, common-gate (CG), low-noise amplifier(LNA), integrated circuit (IC)

PACS: 07.57.Kp, 84.40.-x

CMOS 毫米波低功耗超宽带共栅低噪声放大器

杨格亮, 王志功*, 李智群, 李 芹, 刘法恩, 李 竹

(东南大学 射频与光电集成电路研究所,江苏 南京 210096)

摘要:陈述了一个基于单端共栅与共源共栅级联结构的超宽带低噪声放大器(LNA).该LNA用标准90-nm RF CMOS工艺实现并具有如下特征:在28.5 ~ 39 GHz频段内测得的平坦增益大于10 dB;−3 dB带宽从27 ~ 42 GHz达到了15 GHz,这几乎覆盖了整个Ka带;最小噪声系数(NF)为4.2 dB,平均NF在27 ~ 42 GHz频段内为5.1 dB;S_{11}在整个测试频段内小于−11 dB.40 GHz处输入三阶交调点(IIP3)的测试值为+2 dBm.整个电路的直流功耗为5.3 mW.包括焊盘在内的芯片面积为0.58 mm × 0.48 mm.

关 键 词:毫米波;宽带;互补金属氧化物半导体(CMOS);共栅;低噪声放大器(LNA);集成电路(IC)

中图分类号:TN4 **文献标识码**:A

Introduction

The development of wireless communication demands future CMOS ICs that transmit and receive data at high speeds with low error rates, low cost and low power. The millimeter-wave technology is acknowledged to be promising to compensate the spectrum blockage in low frequency range and satisfy the increasing requirements for higher data-rate transmission. The practical demonstrations on the CMOS monolithic millimeter-wave ICs [1-3] heighten our confidence that we have found a more effective and economical solution than the conventional III-V compound semiconductor technology.

Among the building blocks in millimeter-wave front-end, the LNA plays a dominant role to deliver sufficient power gain for the incoming signal while suppressing the potential noise for the desirable signal-to-noise ratio at output. The implementation of an LNA decides whether a CMOS process is suitable for the millimeter-wave applications. Various topologies, such as common-source, CG and cascode, have been demonstrated available for an LNA design. To the authors' best knowledge, most of the studies are carried out based on the first two choices because the common-source topology has both voltage and current gain which is an advantage for an amplifier design, the cascode topology mitigates the Miller-effect caused by the drain-gate parasitic capacitance C_{gd} of the

Received date: 2013 - 08 - 04, **revised date**: 2014 - 10 - 04 **收稿日期**:2013 - 08 - 04, **修回日期**:2014 - 10 - 04

Foundation items: Supported by the 973 project (2010CB327404), the 863 project (2011AA10305), and National Natural Science Foundation of China (61106024, 60901012)

Biography: YANG Ge-Liang (1984-), male, Anhui, China, Ph. D. Research interests include RF and microwave IC designs for wireless communications. E-mail: yglamen@gmail.com

* **Corresponding author**: Email: zgwang@seu.edu.cn

common-source stage which leads to a high isolation performance. A 3-stage 60-GHz narrow band common-source LNA [4] was proposed with 15-dB maximum gain and 4.4 dB minimum NF. Another V-band 3-stage cascode LNA [5] was designed with more than 20-dB power gain. However, it consumes a high power of 79-mW from a 2.4-V supply, and besides, the NF is as high as 8 dB.

The CG topology, well known for its superior bandwidth, linearity, stability and robustness to PVT variations, has attracted more interests from the research community. For instance, it has been used in a LNA with differential configuration [6-7]. In addition, the CG topology was also used combined with g_m-boosted [8] and current-reuse [9-10] techniques for NF and power optimization. Whereas, all of these studies [6-10] realized the LNA at the frequencies lower than 20 GHz. Thus, further exploration is significant to maintain the flexibilities of CG LNA. Within this context, a 2-stage, CG in cascade with cascode, wideband LNA is proposed to provide insight into the millimeter-wave range IC design. The significant characteristics in terms of gain, input impedance, NF and linearity of the CG topology are analyzed mathematically followed by the circuit implementation and experimental discussions. At the end, a brief conclusion is conducted.

1 Annalysis of the fundamental CG topology

1.1 Gain and input impedance

The ABCD matrix, well known for its cascading characteristic, can be employed to provide the uniform method for the gain, input impedance and noise analysis. As far as the CG topology is concerned, a 2-port small-signal equivalent model shown in Fig. 1 is used for the ABCD matrix derivation. For the mathematical simplification, R_g is dismissed from the model since it is small enough ($<10\ \Omega$ for a transistor with $W=2\ \mu m \times 15$) compared with R_{ds}, $1/\omega C_{gs}$ and $1/\omega C_{gd}$. Accordingly, the 2-port network is characterized by

$$\begin{bmatrix} U_1 \\ I_1 \end{bmatrix} = \begin{bmatrix} A & B \\ C & D \end{bmatrix} \begin{bmatrix} U_2 \\ I_2 \end{bmatrix} \quad , \quad (1)$$

in which

$$A = \frac{U_1}{U_2}\Big|_{I_2=0} = \frac{1 + sR_{ds}C_{gd}}{1 + g_m R_{ds}} \quad , \quad (2)$$

$$B = \frac{U_1}{I_2}\Big|_{U_2=0} = \frac{R_{ds}}{1 + g_m R_{ds}} \quad , \quad (3)$$

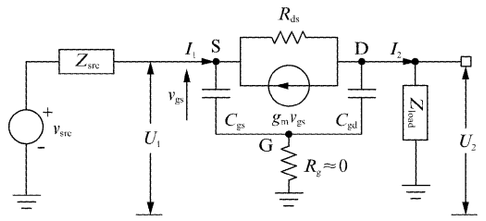

Fig. 1　Small-signal equivalent model for NMOS transistor with CG configuration. S, D and G represent the transistor's source, drain and gate node, respectively

图 1　共栅配置下 NMOS 晶体管的小信号等效模型. S,D 和 G 分别代表晶体管的源、漏和栅极节点

$$C = \frac{I_1}{U_2}\Big|_{I_2=0} = sC_{gs}\left(A + \frac{C_{gd}}{C_{gs}}\right) \quad , \quad (4)$$

$$D = \frac{I_1}{I_2}\Big|_{U_2=0} = 1 + BsC_{gs} \quad . \quad (5)$$

Equation (5) shows that $|D| \geqslant 1$, thus it can be concluded that the current gain of the common gate topology is $\leqslant 1$. This means there is no current gain but only voltage gain possible in the common gate topology.

The next feature to determine is the input impedance. To also take into account the effect of Z_{load}, the ABCD-parameters of the total system is represented by

$$\begin{bmatrix} A' & B' \\ C' & D' \end{bmatrix} = \begin{bmatrix} A & B \\ C & D \end{bmatrix} \begin{bmatrix} 1 & 0 \\ 1/Z_{load} & 1 \end{bmatrix} \quad . \quad (6)$$

Therefore, the input impedance can be calculated as

$$Z_{in} = \frac{A'}{C'} = \frac{A + B/Z_{load}}{C + D/Z_{load}} \quad . \quad (7)$$

Substituting Eqs. (4) and (5) in (7), we obtain

$$Z_{in} = 1/\left(sC_{gs} + \frac{sC_{gd} + 1/Z_{load}}{A + B/Z_{load}}\right) \quad . \quad (8)$$

Usually, R_{ds} has a large value. In this case, A, B in Eqs. (2) and (3) can be rewritten as

$$A = sC_{gd}/g_m,\ B = 1/g_m \quad . \quad (9)$$

When the equation above is substituted in Eq. (8), we obtain

$$Z_{in} = 1/(g_m + sC_{gs}) \quad . \quad (10)$$

Equation (10) implies that the input impedance of the CG topology has little dependence on Z_{load}. This is an elemental feature of the CG topology. It provides the designer the sufficient freedom to set the bias point of the transistor for desired input impedance.

It can be found from Eq. (10) that the real and imaginary part of Z_{in} are

$$R_{in} = \frac{g_m}{g_m^2 + (\omega C_{gs})^2},\ X_{in} = -\frac{\omega C_{gs}}{g_m^2 + (\omega C_{gs})^2} \quad . \quad (11)$$

Assume R_{src} and X_{src} are real and imaginary part of the source impedance, respectively. Under input matching circumstances $R_{in} = R_{src}$, $X_{in} = -X_{src}$. This means an inductance equals to

$$L_{src,match} = \frac{C_{gs}}{g_m^2 + (\omega C_{gs})^2} \quad . \quad (12)$$

As far as a NMOS transistor with $W=2\ \mu m \times 15$ is concerned, the corresponding $g_m = 16.58$ mS and $C_{gs} = 23.67$ fF. Therefore, the calculated $L_{src,match}$ equals 78 pH at a frequency of 35 GHz.

1.2 Noise analysis

The NF of a multi-stage LNA was proved to be mainly decided by the transistor of the first stage. The noise sources in a CMOS device are referred to as the channel thermal noise and the gate induced noise due to non-quasi-static effect [11]. Mathematically, the channel thermal noise can be described as [12]

$$\overline{i_d^2} = 4\kappa T \gamma g_{d0} \Delta f \quad , \quad (13)$$

where $g_{d0} = \mu_n C_{ox} W(V_{GS} - V_T)/L$ is the drain conductance for zero drain voltage.

The gate induced noise is given as [13]

$$\overline{i_g^2} = 4\kappa T \sigma g_g \Delta f \quad , \quad (14)$$

where σ is a constant, $g_g = [\omega(C_{gs} + C_{gd})]^2/5g_{d0}$ is a

high-frequency rectified result referring to Ref. [14].

In this work, a CG topology is chosen as the input stage. Therefore, the noise equivalent circuit of the CG transistor should be modeled. Figure 2 shows the noise composition of the CG topology in which the gate induced noise is represented by a voltage source in series with a resistor. Taking advantage of the ABCD matrix previously derived, the output channel noise can be converted to the input as shown in Fig. 3. Defining two variables

$$V_n = -Bi_d,\ i_n = -(D-1)i_d \quad . \quad (15)$$

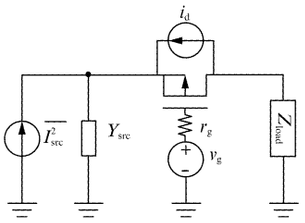

Fig. 2 Noise sources present in the transistor
图2 晶体管中的噪声来源

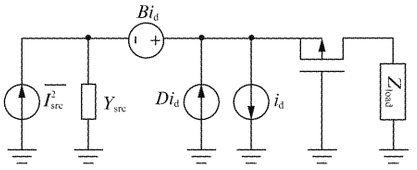

Fig. 3 Converting the channel noise to the input
图3 沟道噪声转换到输入端

Then it can be easily determined that

$$\overline{V_n^2} = |B|^2\,\overline{i_d^2},\ i_n = \frac{D-1}{B}V_n \quad . \quad (16)$$

Thus, i_n is completely correlated to V_n. Substituting Eq. (13-16), a noise resistance can be derived as

$$R_n = \frac{\overline{V_n^2}}{4\kappa T\Delta f} = |B|^2\gamma g_{d0} \quad . \quad (17)$$

The following step is to convert the gate induced noise to the input. Since the noise voltage source can be shifted to the in-and output, the output noise source can be brought back to the input by multiplying it with A and C as shown in Fig. 4. Accordingly, the NF is calculated to be

$$NF = 1 + \frac{\overline{|i_n + i_g r_g C + Y_{src}[V_n - (1-A)i_g r_g]|^2}}{\overline{i_{src}^2}} \quad ,(18)$$

in which, $i_g r_g = v_g$. It is known that i_g is partially correlated with V_n. Expending i_g into two explicit parts:

$$i_g = i_{gc} + i_{gu} \quad , \quad (19)$$

where i_{gc} and i_{gu} are V_n-correlated and -uncorrelated part,

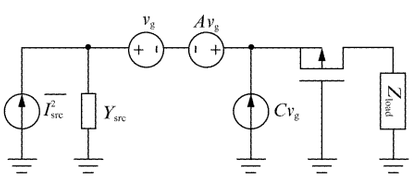

Fig. 4 Converting the gate induced noise to the input
图4 诱导栅噪声转换到输入端

respectively. Therefore, the following formula holds.

$$\overline{i_g^2} = \overline{i_{gc}^2} + \overline{i_{gu}^2} = 4\kappa T\Delta f\sigma g_g|c|^2 + 4\kappa T\Delta f\sigma g_g(1-|c|^2) \quad . \quad (20)$$

The resulting NF is found to be

$$NF = 1 + \frac{G_u}{G_{src}}|r_g|^2\left|C-(1-A)Y_{src}\right|^2 + \frac{R_n}{G_{src}}\left|\frac{D-1}{B} + \frac{i_{gc}}{V_n}r_g[C-(1-A)Y_{src}] + Y_{src}\right|^2 \quad ,(21)$$

where

$$G_u = \frac{\overline{i_{gu}^2}}{4\kappa T\Delta f} = \frac{\omega^2(C_{gs}+C_{gd})^2\sigma}{5g_{d0}}(1-|c|^2) \quad ,(22)$$

$$G_{src} = \frac{\overline{i_{src}^2}}{4\kappa T\Delta f} = \frac{\omega^2 C_{gd}(C_{gs}+C_{gd})}{g_{d0}}|c|\sqrt{\frac{\sigma}{5\gamma}} \quad ,(23)$$

$$Y_{src} = G_{src} + jB_{src} \quad . \quad (24)$$

In addition

$$\frac{i_{gc}}{V_n} = \frac{i_{gc}}{i_d}\cdot\frac{i_d}{V_n} = -\frac{c}{B}\frac{\omega(C_{gs}+C_{gd})}{g_{d0}}\sqrt{\frac{\sigma}{5\gamma}} \quad ,(25)$$

in which, the correlation factor $c \approx j\,0.395$. Substituting Eqs. (2) ~ (5) and (25) into (21) with $R_{ds} \to \infty$ in consideration, we obtain

$$NF \approx 1 + \frac{G_u}{G_{src}}r_g^2[G_{src}^2 + (B_{src}-\omega C_{gd})^2] + \frac{R_n}{G_{src}}\{[G_{src} - M(B_{src}-\omega C_{gd})]^2 + (B_{src}+\omega C_{gs}+MG_{src})^2\} \quad ,(26)$$

where

$$M = |c|g_m r_g\frac{\omega(C_{gs}+C_{gd})}{g_{d0}}\sqrt{\frac{\sigma}{5\gamma}} \quad . \quad (27)$$

It is worth mentioning that Eq. (26) is a simplified result under the assumptions $(\omega C_{gd}/g_m)^2 \ll 1$ and $M\omega C_{gd}/g_m \ll 1$, which is usually the case.

To find the optimal value of B_{src}, the derivative of the NF is taken and made equal to zero $\partial NF/\partial B_{src} = 0$.

$$B_{src} = B_{opt} = (G_u r_g^2\omega C_{gd} - R_n\omega C_{gs})/(G_u r_g^2 + R_n) \quad . (28)$$

The resulting optimal source inductance can be derived as

$$L_{src,opt,NF} = \frac{G_u r_g^2 + R_n}{\omega^2(R_n C_{gs} - G_u r_g^2 C_{gd})} \neq L_{src,match} \quad . (29)$$

As can be seen there is a tradeoff between the optimal inductance concerning noise performance and input match. To find the optimal value for G_{src}, also the derivative is taken and made equal to zero $\partial NF/\partial G_{src} = 0$.

$$G_{src} = G_{opt} = \frac{\omega(C_{gs}+C_{gd})}{G_u r_g^2 + R_n}\sqrt{G_u r_g^2 R_n} \quad . (30)$$

Taking into account the optimal G_{src} and B_{src}, the resulting NF_{min} is determined by

$$NF_{min} = 1 + \frac{2}{\sqrt{5}}\frac{\omega}{\omega_T}\sqrt{\gamma\sigma(1-|c|^2)}\,\omega(C_{gs}+C_{gd})r_g\left(1+\sqrt{\frac{|c|^2}{1-|c|^2}}\right) \quad . \quad (31)$$

1.3 Linearity analysis

The nonlinearity of a MOS transistor arises from its voltage-to-current (V-I) conversion. The drain current in a MOSFET can be modeled in terms of its gate-source voltage as follows:

$$i_d = g_{m1}v_{gs} + g_{m2}v_{gs}^2 + g_{m3}v_{gs}^3 \quad , \quad (32)$$

where g_{m1} is the main transconductance, g_{m2} represents its second-order nonlinearity obtained by the second-order derivative of MOSFET DC transfer characteristics and g_{m3} is the third-order nonlinearity obtained by the third-order derivative of MOSFET DC transfer characteristics. To find the IIP3 of the CG topology, a linear equivalent circuit shown in Fig. 5 is modeled to help with the derivation.

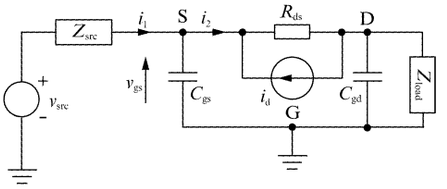

Fig. 5　Linear equivalent model for the CG topology
图 5　共栅结构的线性等效模型

The current and voltage relationships shown in Fig. 5 can be described by the following set of equations:

$$\begin{cases} i_1 = -v_{gs}sC_{gs} + i_2 \\ -v_{gs} = (i_2 + i_d)R_{ds} + i_2(sC_{gd} \| Z_{load}) \end{cases} . \quad (33)$$

The set of equations above can be solved to obtain i_1, which is given by

$$-i_1 = v_{gs}sC_{gs} + Ki_d + v_{gs}K/R_{ds} , \quad (34)$$

where

$$K = R_{ds}/(R_{ds} + sC_{gd} \| Z_{load}) . \quad (35)$$

Substituting Eq. (32) and (34) in $v_{src} = i_1 Z_{src} - v_{gs}$ we obtain

$$-v_{src} = [1 + Z_{src}(Kg_{m1} + sC_{gs} + K/R_{ds})]v_{gs} + Kg_{m2}Z_{src}v_{gs}^2 + Kg_{m3}Z_{src}v_{gs}^3 . \quad (36)$$

Notably, given $y = a_1x + a_2x^2 + a_3x^3 + \cdots$, it can be found that $x = b_1y + b_2y^2 + b_3y^3 + \cdots$, where

$$b_1 = 1/a_1 , \; b_2 = -a_2/a_1^3 , \; b_3 = (2a_2^2 - a_1a_3)/a_1^3 . \quad (37)$$

Therefore, v_{gs} can be expressed by v_{src} according to Eq. (36). Substituting the result in Eq. (32), i_d can be expressed as

$$i_d = -g_{m1}b_1v_{src} + (g_{m1}b_2 + g_{m2}b_1^2)v_{src}^2 - (g_{m2}b_3 + 2b_1b_2g_{m2} + g_{m3}b_1^3)v_{src}^3 + \cdots , \quad (38)$$

where $b_1 = A$, $b_2 = -Kg_{m2}Z_{src}A^3$, $b_3 = 2(Kg_{m2}Z_{src})^2A^3 - Kg_{m3}Z_{src}A^2$, $A = 1/[1 + Z_{src}(Kg_{m1} + sC_{gs} + K/R_{ds})]$.

The resulting IIP3 can be written as

$$\text{IIP3} = \frac{2}{3\text{Re}(Z_{src})}\left|\frac{g_{m2}b_3 + 2b_1b_2g_{m2} + g_{m3}b_1^3}{g_{m1}b_1}\right| = \frac{2}{3\text{Re}(Z_{src})}\frac{1}{|A||A/g_{m1} - KZ_{src}||g_{m3} - 2Kg_{m2}^2Z_{src}A|} . \quad (39)$$

Equation (39) shows another feature of the CG topology that its IIP3 has little dependence on Z_{load} and C_{gd} when $R_{ds} \to \infty$. In this case, $|K| = 1$, a high IIP3 can be obtained if the transistor is properly configured.

2　Circuit implementation

Previously, the CG LNAs were designed for low frequency applications [6-10] as well as the UWB CG LNA [15] whose circuit construction (CG in cascade with cascode) is similar to this study. Therefore, a further investigation was carried on by this work to provide insight into the UWB CG LNA implemented in the millimeter-wave band. To extend the LNA's bandwidth, the inductive-peaking technique shown in Fig. 6 was introduced. The NMOS transistor, which is loaded by a series-shunt-series network in the LNA, is substituted by a current source.

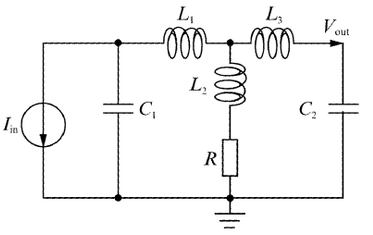

Fig. 6　Series-shunt-series peaking network
图 6　串联-并联-串联峰化网络

To explain the effect of the series-shunt-series peaking network, its normalized transimpedance is derived as

$$Z_N(s) = \frac{1 + \dfrac{s}{\omega_0 m_2}}{\dfrac{s^4}{\omega_0^4}k_C(1-k_C)\left(\dfrac{1}{m_1m_2} + \dfrac{1}{m_2m_3} + \dfrac{1}{m_3m_1}\right) + \dfrac{s^3}{\omega_0^3}k_C(1-k_C)\left(\dfrac{1}{m_1} + \dfrac{1}{m_3}\right) + \dfrac{s^2}{\omega_0^2}\left(\dfrac{1}{m_2} + \dfrac{1}{m_3} + \dfrac{k_C}{m_1}\right) + \dfrac{s}{\omega_0} + 1} , \quad (40)$$

where $\omega_0 = 1/RC$, $m_1 = R^2C/L_1$, $m_2 = R^2C/L_2$, $m_3 = R^2C/L_3$, $K_C = C_1/(C_1 + C_2)$.

Figure 7 illustrates the frequency response of the amplifier with and without ($L_1 = L_2 = L_3 = 0$) series-shunt-series peaking. As expected, the −3 dB bandwidth is extended a lot (more than 3 times) when the inductive-peaking technique is utilized.

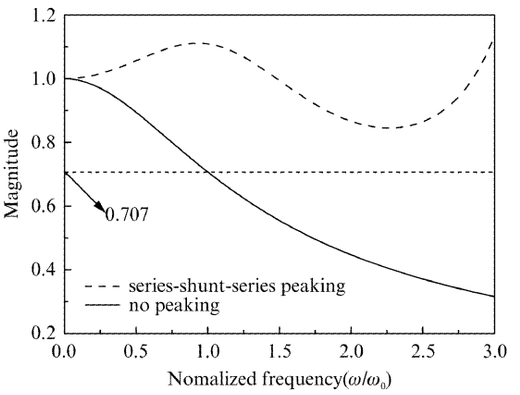

Fig. 7　Frequency response of Z_N with and without peaking
图 7　采用和未采用峰化技术下 Z_N 的频率响应

Figure 8 schematizes the proposed LNA in which both of the two stages incorporate the series-shunt-series peaking network. An off-chip bias Tee is connected at the input port to provide a closed DC loop for the first stage. A micro-strip line (MS-Line) is employed for the implementation of the $L_{src,matcth}$ because it has such a small value. Additionally, an inductor is placed between the gate of the CG transistor and VG_1 to assist the noise matching and the gain flatness enhancement [16]. It is shown in Fig. 9 that the larger inductance will improve the noise match but deteriorate the input impedance match. This definitely verifies the prediction aforementioned that the tradeoffs should be made between the noise and input impedance match. Finally, a 180 pH inductance was chosen for the design. Another inductor placed between the cascode transistors is aimed to enhance the gain and output match.

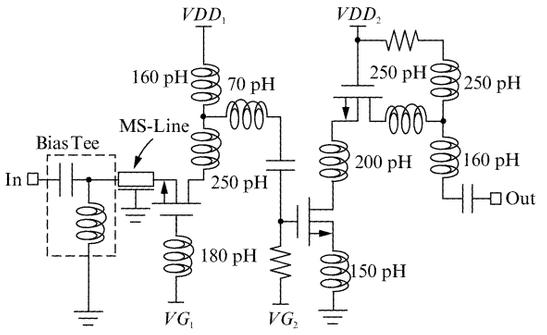

Fig. 8 Schematic of the proposed CG LNA
图8 共栅 LNA 的原理图

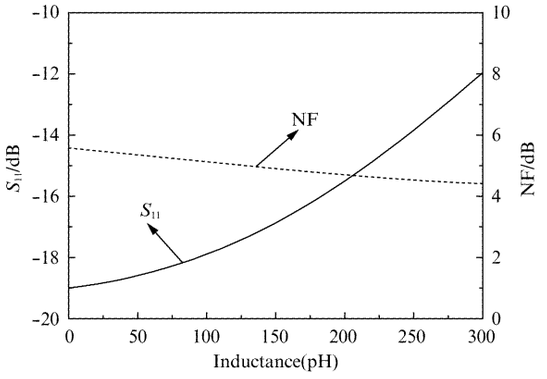

Fig. 9 S_{11} and NF vary with respect to the gate inductance
图9 S_{11}和 NF 随栅电感感值的变化

3 Experimental results and discussions

The proposed CG LNA was fabricated in a standard 90-nm RF CMOS process. The chip photograph is shown in Fig. 10. The overall chip area is 0.58 mm × 0.48 mm. The LNA draws 3 mA current from a 0.36-V supply at the first stage and 4.2 mA from a 1-V supply at the second stage. On-wafer measurements are performed by an Agilent's N5245A 4-port 50-GHz network analyzer. The S-parameters measured from 25 to 45 GHz by on-wafer probe testing are shown in Fig. 11 together with the simulation results. Within 28.5 ~ 39 GHz, the measured S_{21} achieves a maximum value of 10.8 dB at 31 GHz and a minimum value of 9.5 dB at 35.5 GHz. The gain unflatness is less than 1.5 dB in such a wide frequency range (28.5 ~ 39 GHz). Moreover, the 10.5 dB level referred −3 dB bandwidth ranges from 27 to 42 GHz which covers almost the entire Ka band. The measured S_{11} is less than −11 dB across the whole testing band. The measured S_{22} is less than −8.2 within a frequency range of 25 ~ 37.2 GHz. The simulation in general agrees well with the measured results. The stability factor K calculated from the measured S-parameters is greater than 1 and Δ is less than 1, respectively, as shown in Fig. 12, suggesting unconditional stability of the circuit. Figure 13 shows both the simulated and measured NF with a minimum 4.2 dB at 32.8 GHz and a maximum of 6 dB at 37 GH. The average NF (NF_{avg}) is 5.1 dB within the 27 ~ 41.8 GHz range. The measured results are not fit well with the simulated ones at frequencies higher than 40 GHz, as the operating frequency of the off-chip bias-T at the input port is limited by 40 GHz. Fig. 14 shows the measured IIP3 at 40 GHz with a two-tone separation of 50 MHz. An IIP3 of +2 dB is obtained by extrapolation. The measured output 1-dB gain compression point (OP1dB) is shown in Fig. 15.

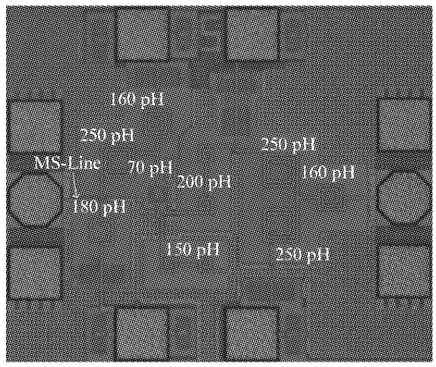

Fig. 10 Chip photograph of the proposed LNA
图10 LNA 的芯片照片

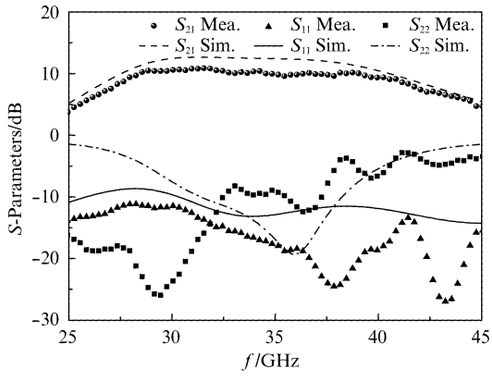

Fig. 11 Measured S-parameters
图11 S-参数测试结果

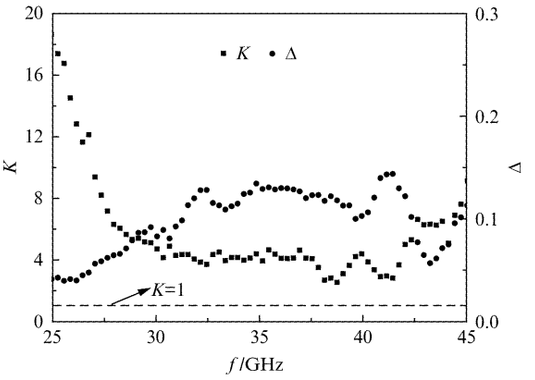

Fig. 12　Measured stability factors
图 12　稳定因子测试结果

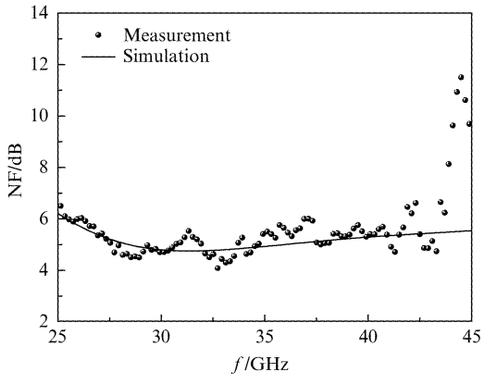

Fig. 13　Measured and simulated NF
图 13　NF 测试与仿真结果

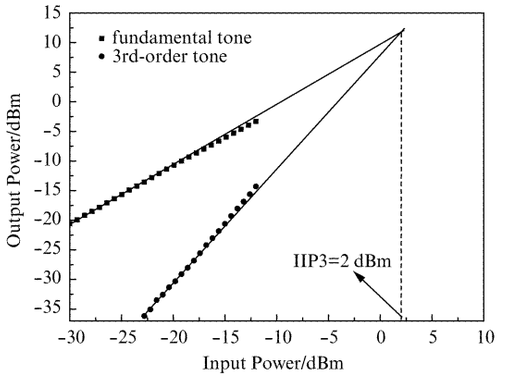

Fig. 14　Measured IIP3 at 40 GHz
图 14　40 GHz 频率处 IIP3 的测试结果

The performances of the proposed LNA are summarized in Table 1. The recently published papers [17-21] are also listed for comparison. The figure of merit (F. O. M) defined as Eq. (41) in Ref. [17] is introduced for comparison as well.

$$\text{F. O. M.} = \frac{\text{Gain(dB)} \cdot \text{BW(GHz)}}{[\text{NF}_{\text{avg}}(\text{dB}) - 1] \cdot \text{P}_{\text{DC}}(\text{mW})} \quad (41)$$

It can be observed from Table 1 that the proposed CG LNA have impressive performances in power dissipation, −3 dB bandwidth, IIP3 and F. O. M, which are better than other published millimeter-wave LNAs reported to date.

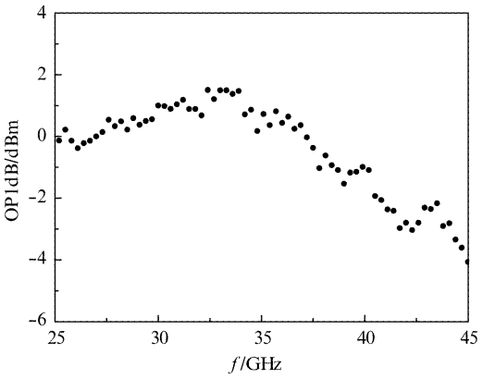

Fig. 15　Measured OP1dB
图 15　OP1dB 的测试结果

Table 1　Measured performances summary and comparison
表 1　测试性能总结与对比

Ref.	Process	Topology	Flat gain/dB	BW*/ GHz	NF_{avg}/ dB	P_{DC}/ mW	IIP3/ dBm	Size/ mm^2	F. O. M
[18] MWCL	0.13 μm CMOS	3-stage Common-source	18.75	34 ~ 44	7.15	36	−2.5	0.525	0.85
[17] TMTT	0.13 μm CMOS	1-stage Triple-Cascode	12.8	35 ~ 43	4	28.8	N/A	0.252	1.22
[19] EL	0.13 μm CMOS	3-stage Common-source	15.64	20 ~ 29	3.48	22.1	−12	0.518	2.57
[20] TMTT	90 nm CMOS	1-stage TF** − Quard-Cascode	18.8	32 ~ 43.3	>4.6	15	N/A	0.212	<4
[21] TMTT	90 nm CMOS	1-stage TF-Cascode	<13.8	29 ~ 44	>3.8	18	−1	0.483	<4.2
This work	90 nm CMOS	2-stage CG + Cascode	10.15	27 ~ 42	5.1	5.3	+2	0.278	7.01

* BW denotes the −3 dB bandwidth.　** TF stands for transformer.

4　Conclusion

In this paper, the CG in cascade with cascode configuration with bandwidth extension technique were proposed, analyzed and applied to implement a miniature CMOS LNA. The LNA was finally fabricated in a standard 90-nm CMOS process. The on-chip measurement results feature a flat gain of 10.15 dB within the 28.5 ~ 39 GHz range, an average NF of 5.1 dB across the 27 ~ 42 GHz range, an IIP3 of +2 dBm, and a relatively low power dissipation of 5.3 mW. The large bandwidth, mediate gain and NF, and low power dissipation result in a high F. O. M. The chip size of the LNA is 0.58 × 0.48 mm^2 including all testing pads.

References

[1] Doan C H, Emami S, Niknejad A M, *et al*. Millimeter-wave CMOS design [J]. *IEEE Journal of Solid-State Circuits*, 2005, **40**(1): 144−154.

[2] Masud M A, Zirath H, Ferndahl M, *et al*. 90 nm CMOS MMIC amplifier [C]. *IEEE RFIC Symp Dig*, 2004: 201−204.

[3] Ellinger F. 26 ~ 42 GHz SOI CMOS low noise amplifier [J]. *IEEE Journal of Solid-State Circuits*, 2004, **39**(3): 522−528.

[4] Cohen E, Ravid S, Ritter D. An ultra low power LNA with 15 dB gain

and 4.4 dB NF in 90 nm CMOS process for 60 GHz phase array radio [C]. *IEEE Radio Frequency Integrated Circuits Symposium*, 2008: 61-64.

[5] Lo C-M, Lin C-S, Wang H. A miniature V-band 3-stage cascode LNA in 0.13 μm CMOS [C]. *IEEE International Solid-State Circuits Conference*, 2006: 1245-1263.

[6] Woo S, Kim W, Lee C-H, *et al*. A 3.6 mW differential common-gate CMOS LNA with positive-negative feedback [C]. *IEEE International Solid-State Circuits Conference*, 2006: 218-219.

[7] Khurram M, Rezaul Hasan S M. Series peaked noise matched g_m-boosed 3.1 ~ 10.6 GHz CG CMOS differential LNA for UWB WiMedia [C]. *Electronics Letters*, 2011: 1346-1348.

[8] Chamas I R, Raman S. Analysis, design and X-band implementation of a self-biased active feedback G_m-boosted common-gate CMOS LNA [J]. *IEEE Transactions on Microwave Theory and Techniques*, 2009, **57**(3): 542-551.

[9] Jeong C J, Qu W, Sun Y, *et al*. A 1.5V, 140 μA CMOS ultra-low power common-gate LNA [C]. *IEEE Radio Frequency Integrated Circuits Symposium*, 2011: 1-4.

[10] Lee J-Y, Park H-K, Chang H-J, *et al*. Low-power UWB LNA with common-gate and current-reuse techniques [J]. *IET Microwave Antennas Propagation*, 2012, **6**(7): 793-799.

[11] Shaeffer D K, Lee T H. A 1.5-V, 1.5-GHz CMOS Low Noise Amplifier [J]. *IEEE Journal of Solid-State Circuits*, 1997, **32**(5): 745-759.

[12] Aldert Van Der Ziel. Noise in solid-state devices and lasers [J]. *Proceedings of IEEE*, 1962: 1801-1812.

[13] Aldert Van Der Ziel. *Noise in solid-state devices and Circuits* [M]. *Wiley*, *New York*, 1986.

[14] Shoji M. Analysis of high-frequency thermal noise of enhancement mode MOS field-effect transistors [J]. *IEEE Transactions on Electron Devices*, 1966, **13**(6): 520-524.

[15] Shim Y, Kim C-W, Lee J, *et al*. Design of full band UWB common-gate LNA [J]. *IEEE Microwave and Wireless Components Letters*, 2007, **17**(10): 721-723.

[16] Yu Y-H, Yang Y-S, Chen Y-J Emery. A compact wideband CMOS low noise amplifier with gain flatness enhancement [J]. *IEEE Journal of Solid-State Circuits*, 2010, **45**(3): 502-509.

[17] Huang B-J, Wang H, Lin K-Y. Millimeter-wave low power and miniature CMOS multi-cascode low noise amplifiers with noise reduction topology [J]. *IEEE Transactions on Microwave and Theory Techniques*, 2009, **57**(12): 3049-3059.

[18] Tsai J H, Chen W C, Wang T P, *et al*. A miniature Q-band low noise amplifier using 0.13-μm CMOS technology [J]. *IEEE Microwave Wireless Component Letters*, 2006, **16**(6): 327-329.

[19] Wang C-H, Chiu Y-T, Lin Y-S. 3.1 dB NF 20 ~ 29 GHz CMOS UWB LNA using a T-match input network [J]. *Electronics Letters*, 2010, **46**(19): 1312-1313.

[20] Yeh H C, Liou Z Y, Wang H. Analysis and design of millimeter-wave low power CMOS LNA with transformer-multi-cascode topology [J]. *IEEE Transactions on Microwave and Theory Techniques*, 2011, **59**(12): 3441-3454.

[21] Yeh H-C, Chiong C-C, Aloui S, *et al*. Analysis and design of millimeter-wave low-voltage CMOS cascode LNA with magnetic coupled technique [J]. *IEEE Transactions on Microwave and Theory Techniques*, 2012, **60**(12): 3441-3454.