第 38 卷第 4 期
2019 年 8 月

红 外 与 毫 米 波 学 报
J. Infrared Millim. Waves

Vol. 38, No. 4
August, 2019

文章编号: 1001 - 9014(2019)04 - 0426 - 07

DOI:10.11972/j.issn.1001 - 9014.2019.04.006

High efficiency 220 GHz frequency doubler based on discrete Schottky diodes

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Abstract: A high efficiency 220 GHz frequency doubler based on discrete diodes is presented in this paper. This doubler is realized with a 50 μm thick, 450 μm wide, and 2.7 mm long quartz substrate. The conversion efficiency is better than 16% over the frequency range from 214 to 226 GHz with pumping power of 46.4 ~ 164 mW at the indoor temperature. A peak output power of 32mW at 218 GHz with an input power of 161 mW, and several frequency points with efficiency high than 20% are realized. This doubler can act as the pumping stage of the 660 GHz multiplier chain.

Key words: 220 GHz, balanced doubler, Schottky, model
PACS: 85.30.Hi, 85.30.Kk, 84.30.Vn, 07.57.Hm

基于分离式二极管的 220 GHz 高效率倍频器

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摘要:在分离式二极管的基础上,实现了 220 GHz 高效率的二倍频器结构. 该倍频器的电路在 450 μm 宽,2.7 mm 长的 50 μm 石英基片上实现. 测试结果表明,在室温下当驱动功率在 46.4 ~ 164 mW 时,在 214 ~ 226 GHz 的频段内能够实现大于 16% 的倍频效率. 另外,当驱动功率在 161 mW 时,倍频器在 218 GHz 频点能够输出最高功率 32 mW,并且在多个频点拥有高于 20% 的倍频效率. 实验证明,所实现的二倍频器能够作为 660 GHz 倍频链路的驱动前级使用.

关 键 词:220 GHz;平衡式二倍频;肖特基二极管;模型

中图分类号:TN771 **文献标识码**:A

Introduction

Multipliers based on Schottky diodes have always been the most commonly used method of generating power at frequencies ranging from 100 to 1 000 GHz. Over the years, these devices play a critical role in terahertz system such as solid-state source for imaging and communication[1-3], which pushes the operating frequency exceeding 670 GHz[4].

The generation of waves at frequencies over 670 GHz typically requires several stages of multiplication. Although the efficiencies of the separated doubler can be 50% or more. The overall efficiency of the multiplier chain is usually as low as a few percent[5]. Serving as the driven stage multiplier in a THz frequency multiplier chain, doublers working in WR-4 band and WR-3 band should have enough bandwidth. The design of multipliers has been well understood since the work of Penfield[6], based on which several kinds of multiplier topologies were developed over these years. For example, the balanced doubler[7-8], tripler[9-11] and quadruplers[12] con-

Received date: 2018-12-20, **revised date**: 2019-05-26 **收稿日期**:2018-12-20, **修回日期**:2019-05-26

Foundation items: Supported by the National Key Basic Research Program of China (2015CB755406), the Defense Industrial Technology Development Program (JCKY2016212C045, JCKY2017212C002)

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figuration, utilizing the inherent isolation of even or odd order harmonics, realize the following outstanding multipliers operating in WR-5.1 and WR 3.4 band at room temperature. The balanced doubler in Ref. [8] has achieved an outstanding conversion efficiency of 20% ~ 45% over 175 ~ 195 GHz and an output power greater than 80 mW over 185 ~ 195 GHz. For triplers, output power near 200 mW has been achieved in Ref. [10] with ~ 20% efficiency over 105 ~ 120 GHz. At the meantime, 5% ~ 15% efficiency has been delivered in Ref. [11] across 265 ~ 330 GHz using the power combined structure. Finally, quadrupler in Ref. [12] generated output power of 70 mW with a maximum efficiency near 30%, which should be the best multiplier of four reported works in recent years.

In this paper, a fixed-tuned 220 GHz doubler circuit is developed based on the balanced doubler configuration. The symmetry conditions have been introduced to better analyze the whole networks, which significantly reduce the amount of calculation compared with the general method. Meanwhile, imbalance among six junctions also have been analyzed to minimum its negative impact on doubler performance with appropriate width of the diode location gap and reduced-height waveguide. The whole doubler consists of two discrete planar diodes containing six junctions altogether, an E-plane probe integrated with a RF choke filter and stepped-waveguide networks. The whole networks are analyzed and optimized by the co-simulation of HFSS and Agilent's ADS, with the symmetry boundary conditions. The best output power is 32 mW and the corresponding efficiency is 21.5% at 218 GHz with pumping power of 22 dBm. The typical tested efficiency and output power is 16% and 20 mW respectively over the range of 214 ~ 226 GHz.

1 Configuration

Generally, there are two configurations to build Schottky doublers, as shown in Fig. 1. And Fig. 1(a) is a traditional method of frequency multiplying, which always need high performance filters on both sides of the varactor pairs and suitable for all multiplication factor. The dependent on filters to extract the desired harmonics would result in long circuits, which introduces extra transmission loss and leads to higher conversion loss. Figure 1(b) is the so-called Erickson style structure, relying on the inherent mode and frequency isolation between the input and output port. When the input TE10 mode signal is pumped into the diodes in anti-series, only even-order harmonics can be delivered to output port, while the odd-harmonics would be cut off. Thus, the whole circuits do not need any filters on the RF signal path, which could greatly simply the circuit as well as maximum the conversion efficiency.

This work utilizes the balanced configuration in Fig. 1(b), and there are several critical circuits elements should be carefully considered. Firstly, the input reduced-height waveguide should be carefully calculated so that the field distribution called TM11 mode of the second harmonic can be totally cut off. And the generated second harmonic would be prevented from transferring to the input port. Secondly, the suspended circuit channel must be narrowed down enough to ensure the cutoff of the fundamental signal TE10 mode. The third element is the E-probe with a built-in DC bias filter, whose impedance presented on suspended stripline should be adjusted for better operating point. All of these considerations would be further discussed in the next section.

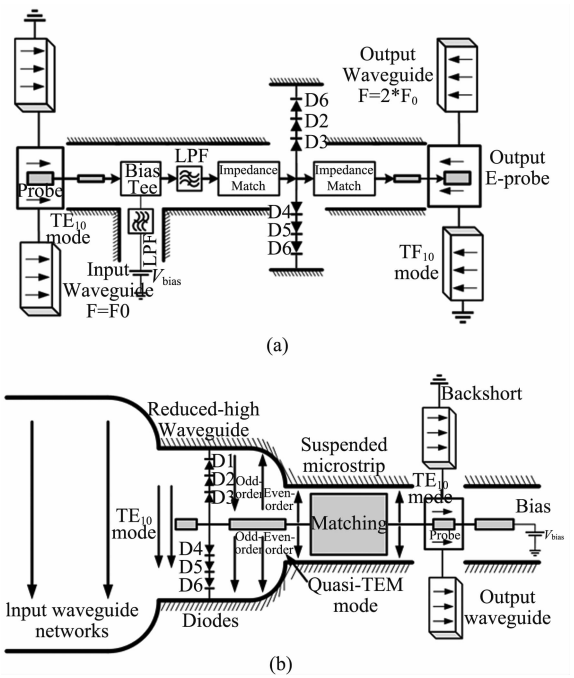

Fig. 1 Diagram of two doubler circuit architecture (a) traditional Schottky diode multiplier configuration, (b) Erickson style Schottky doubler structure

图 1 两种倍频器架构示意图(a)传统肖特基二极管倍频器架构,(b)Erickson 型肖特基二极管倍频器架构

2 Design

2.1 Embedding impedances

In this design, two discrete Schottky diodes containing six junctions altogether are adopted to achieve enough power handling capability. The GaAs diode is selected to have an epitaxial modulation layer 300 nm thick with doping concentration of 10^{17} cm^{-3} and an 8 μm thick highly doped buffer layer. With an anode diameter of 6 μm, these parameters are expected to yield diodes with zero-bias junction capacitance of 35 fF, reverse breakdown of approximately 10 V, and a series resistance of 5 Ω. Further details of the utilized varactors including model and structure have been discussed in our previous work[13].

The first step to design a doubler is determining the embedding impedances of each junction at the internal coaxial wave port. Dimension of the diode mounted on quartz substrate is 248 μm × 50 μm × 10 μm, which is comparable with the wavelength at 220 GHz. As a result, evaluation of the diode's optimum embedding impedances must take into account the influence in the field distribution caused by the diode itself. A co-simulation of the diode is carried out by HFSS and ADS to determine the optimum embedding impedances at each diode junction. The extracted results from full-wave simulation take

part in the calculation of optimum impedance with the nonlinear model of varactors. Finally, the determined diode optimum impedance to incident frequency $Z_{in}(f_0)$ is 17.17-j78, while to output the second harmonic $Z_{out}(2f_0)$ is 25.3-j52.8. According to that, the whole doubler circuit is cut into several passive sub-circuits in series during the design. And numerous electromagnetic analyses on these parts have been carried out with High Frequency Software Simulator (HFSS). Then the simulated results would be introduced into the harmonic balance analysis in Advanced Design System (ADS) from Keysight to ensure the optimum diode matching point and determine the circuit parameters.

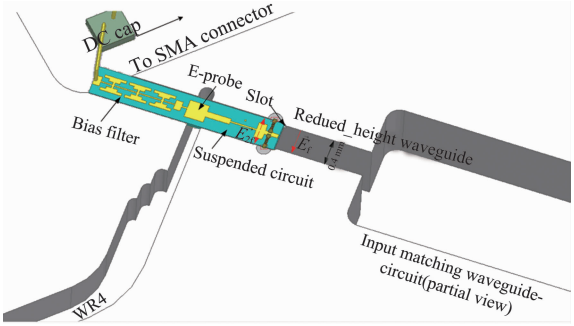

Fig. 2 Partial view of the proposed 220 GHz balanced doubler with a suspended 50 μm thick quartz substrate

图2 采用50 μm石英基板的220 GHz平衡式倍频器部分视图

2.2 Doubler circuits

Figure 2 shows an overview of the proposed 220 GHz symmetry doubler in half of the split block. Obviously, doubler contains input matching waveguide networks, a 50 μm-thick suspended quartz circuit and output waveguide networks. The quartz circuit is composed of impedance matching networks, an E-plane probe coupling to WR4 waveguide, and a DC biasing networks integrated with RF choke filter. The shallow slot, a bit wider than quartz substrate, provides enough space to locate the suspended circuits. To effectively suppress the high order TM11 field distribution, the waveguide height and suspended channel width are chosen to be 400 μm and 360 μm respectively. narrowed enough to block the power leak between input and output port. It can be seen that length of the diode pairs is larger than the width of channel and substrate, which means that one of the diode pads would be placed directly on split block. Direct contact of the diode and metal block exhibits a better thermal dissipation performance, which gets further improvement in power handling capacity.

To analyze fundamental and second harmonic signals individually, the dotted symmetry plane in Fig. 3(a) is introduced. For input fundamental signal, the symmetry plane equals to an electric wall, which leaves out the disturbing of second harmonic. And for second harmonic, the symmetry plane represents to a magnetic wall and eliminates the influence of fundamental signal[14]. In this way, the whole circuit could be cut into three parts, as shown in Fig. 3.

The first part is the section between plane A and A' in Fig. 3(a), in which geometry parameters of the circuit

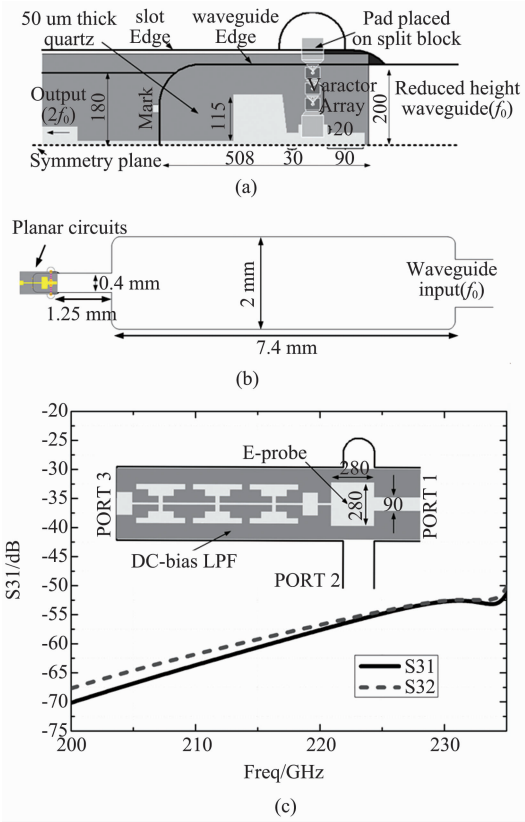

Fig. 3 Circuit geometry of the three primary sections of the 220 GHz doubler (a) input doubler circuit transitions from reduced-height waveguide to suspended stripline, (b) input stepped-waveguide matching networks, (c) output transition to WR-5.1 waveguide

图3 220 GHz倍频器电路三个主要部分的电路几何参数(a)从减高波导至悬着微带线转换结构电路,(b)输入端阶梯波导匹配网络,(c)输出端微带至波导转换结构

would have great influence on input and output impedance matching. The open stub close to the diode array on the circuit could cancel the excess inductance of the six varactors at the second harmonic frequency. Thus, circuit parameters determination in this section must utilize the co-simulation of electric wall and magnetic wall conditions. And the determined geometry parameters are illustrated in Fig. 3(a). The second part is input waveguide matching networks, which could be determined just based on electric wall condition because of the great suppression of second harmonic in reduced-height waveguide. Figure 3(b) shows the simulated waveguide matching networks in WR8 band, which are composed of three waveguide stages. The last part is E-probe section. Impedance matching in this section could leave out the input fundamental signals with magnetic wall condition. As the design objective is to minimum the power leaking from E-probe to DC-bias path, lowpass filter with high RF suppression was adopted. Geometry parameters and simulated results of the E-probe integrated with DC-bias filter are descripted in Fig. 3(c). It is clear that RF isolation of the DC path is more than 45 dB over the operating band.

2.3 Junction imbalance

In our previous design, it has been found that the conversion efficiency always appears about 5% ~ 10% decrease where a series of optimized matching networks were imported to instead the ideal port impedance at the first design step. Usually, that decrease in efficiency is always assumed to due to the insert loss of matching networks. However, similar phenomenon happens again with a bit lower decrease when setting gold to be perfect conductor as well as tuning dielectric loss tangent of the substrate to approximately zero.

Many simulations have been carried out to find out the decrease mechanism. It should be noted that the varactors array shown in Fig. 3(a) act as six loads in series for incident waves (TE10), which means that the input power would be divided into six parts to each junction. On the other hand, the varactors array equals to a series of sources presented to the excited second harmonic (TEM), which determines that the output power of second harmonic would be a combination of six sources located at six junctions. According to the power divider theory, imbalance among these junctions will have great impact on the power delivered to each junction at fundamental frequencies, which also decreases the power combining efficiency of the 6-ways combiner. Thus, passive circuits of the doubler, including matching networks and diode place location, could influence the field distribution around the diodes in some way. And some slight imbalances among six junctions would take place as a consequence. Width of the gap between two discrete diodes (W_g) and the reduced-height waveguide (W_b) would have are taken into account to analyze the impact of junction imbalance on doubler efficiency, utilizing the proposed symmetry condition.

Figure 4 (a) illustrates the imbalance incidence power delivered to each junction with a gap width (W_g) of 18 μm and waveguide width (W_b) of 400 μm. Six junctions can be simplified to three by using the symmetry condition method. In Fig. 4(a), power of the incidence is divided into three parts where each part represents to a pair of junctions located symmetrically. Obviously, great power imbalance over 0.8 dB between each diode pair has been simulated. With a pumping power of 22 dBm, a maximum imbalance of 1.46 dB is obtained between diode 1 and diode 2 shown in Fig. 4(a). As a result, power of the second harmonics also show a similar imbalance, which is shown in Fig. 4(b). An output power imbalance exceeding 1 dB over 214 ~ 225 GHz is simulated, with a max imbalance of 1.18 dB between diode 1 and diode 2. Meanwhile, the typical combining efficiency of those three diode pairs is proved to be 80% over the operating band. Also, peak of the decrease in conversion efficiency caused by imbalance is 5.35% with a typical value of 3.1 dB over 214 ~ 225 GHz. It could be concluded that the combining efficiency of six junctions is influenced by the power distribution on each diode. Moreover, values of W_g and Wb have been swept to evaluate the impact of junction imbalances on doubler efficiency. As shown in Fig. 5, junction imbalances change with the gap width (W_g) and the waveguide width (W_b) which results in different decreases in conversion efficiency. For different parameters, the simulated results show about 8 % decrease in combining efficiency, while the max conversion efficiency decrease about 3% ~ 4%. In a word, geometry parameters of doubler circuits show great influence on junction imbalance which directly changes the conversion efficiency. Thus, value of W_g and W_b should be chosen carefully to minimize the power imbalance.

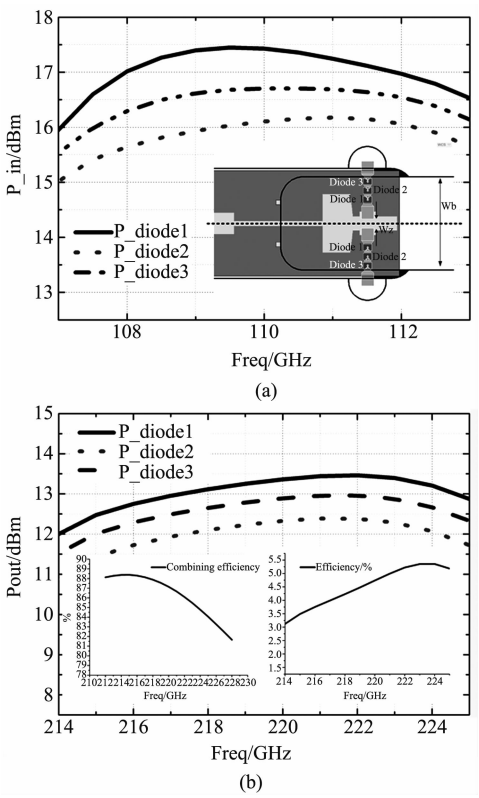

Fig. 4 Imbalances among diode junctions presents to input and output frequency (a) the imbalance incidence power delivered to each junction with a W_g of 18 μm and W_b of 400 μm, (b) output power imbalance of the second harmonics with efficiency decrease and combining efficiency

图 4 二极管结之间的不平衡性 (a) W_g 为 18 μm 和 W_b 为 400 μm 时输入功率传递至每个结区的不平衡度,(b)二极管结之间的输出功率不平衡度以及合成效率与倍频效率衰减值

3 Results and discussion

3.1 Assembly

An E-plane split-waveguide block with a volume of 20 mm × 20 mm × 15 mm is fabricated by computer numerical control milling technology without gold-plated. Meanwhile, the quartz circuit is fabricated by the thin-film technology. Then, the utilized discrete diodes are carefully mounted on the quartz circuit with high controlled W_g. The planar circuit is assembled above the split block by silver conductive paste and the DC-bias connection is carried out through bonding to the SMA-connector, as shown in Fig. 6.

3.2 RF Measurement

Characterization of the doubler is done using the ex-

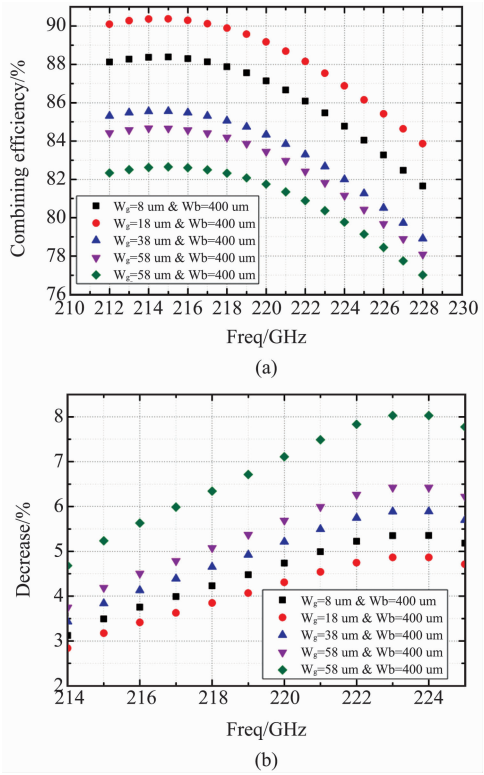

Fig. 5 Variation of the combining efficiency of six junctions and efficiency decrease with different W_g and W_b (a) the combining efficiencies present to the six junctions with changing W_g and W_b, (b) the decreases in conversion efficiency change with the gap width between two discrete diodes and the reduce-height waveguide width

图5 六个管结的合成效率及效率衰减值随 W_g 和 W_b 的变化 (a) W_g 和 W_b 变化时六个管结的合成效率曲线,(b) 倍频效率的衰减值随离散二极管间距和减高波导宽度的变化

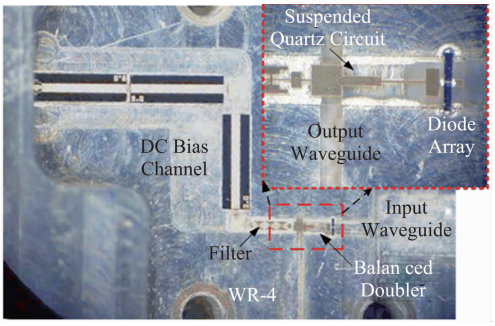

Fig. 6 Photograph of the doubler housing assembly showing the mounted 50 μm-thick quartz doubler circuit substrate

图6 装配50 μm石英基片电路后二倍频器腔体照片

perimental setup shown in Fig. 7. The input 13.4 ~ 14 GHz signals are supplied by an Agilent E8257D frequency synthesizer, while the output power of this 220 GHz doubler is measured by the Erickson-VDI power meter at room temperature. Measurement of the doubler was finished at the Microsystem and Terahertz research center.

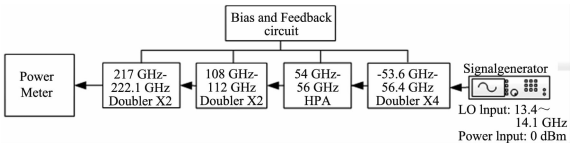

Fig. 7 Test configuration of the proposed 220 GHz doubler

图7 220 GHz倍频器的测试框图

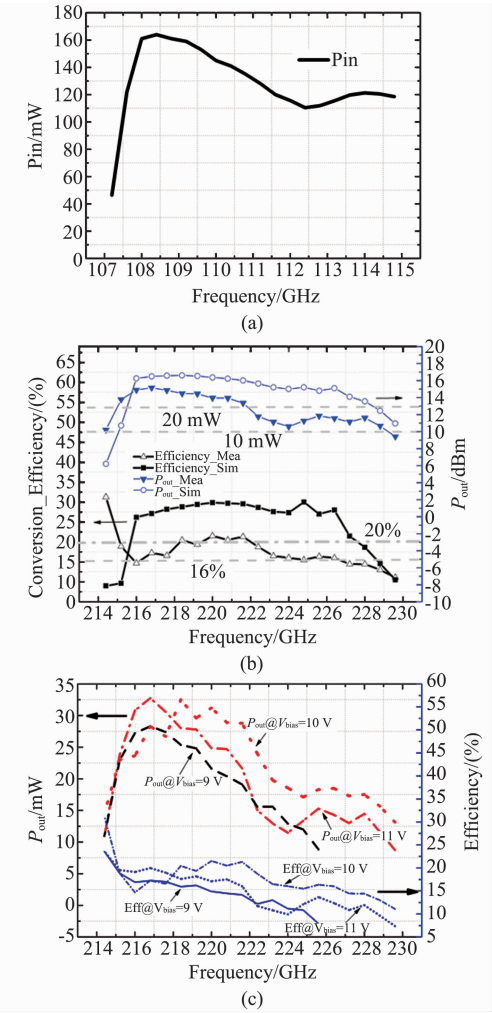

Fig. 8 Measurement of the 220 GHz doubler (a) available output power of the pumping stage of the proposed doubler, (b) doubler output power and efficiency, at a bias of +10 V as a function of frequency compared with the predicted performance from harmonic balance simulation, (c) three sets of output power data and efficiency data correspond to different positive bias voltage (+9 V, +10 V and +11 V)

图8 220 GHz二倍频器测试结果 (a) 驱动链路可提供的输出功率,(b) 偏压为10 V时倍频器的输出功率(仿真与测试结果)随频率的变化,(c) 在不同偏压下的三组输出功率和倍频效率测试曲线

During the test, a 107 ~ 112 GHz medium power driver chain is utilized for the pumping power of 22 dBm. As shown in Fig. 8(a), the input power of the 220 GHz doubler is basically lager than 110 mW in the band of 107 ~ 114.8 GHz except some points with output power lower than 60 mW. To place the varactors in reverse

bias, a voltage with positive polarity through the DC bias channel is required because of the diodes orientation.

The measured output power and conversion efficiency driven by 46 ~ 164 mW input power from 214 to 230 GHz are presented in Fig. 8(b). A peak output power of 32 mW(15.05 dBm) is achieved at 218 GHz with an optimized bias voltage, while the related conversion efficiency is 21.5%. And a high output power over 20 mW in the band of 215 ~ 222 GHz has been obtained on condition that the positive bias voltage is adjusted to 10 V. At the meantime, the typical value of the output power over 214 ~ 230 GHz is proved to be 10 mW. Moreover, the conversion efficiency of stably greater than 20% is reached in the band of 218 ~ 222 GHz, except some frequency points because of their input power less than 22 dBm. And the doubler efficiency could be improved by providing enough pumping power. Figure 8(c) exhibits the measured power of the 220 GHz doubler as the bias voltage to the diodes is varied from 9 to 11V, with available input power shown in Fig. 8(a). It can be seen that a bias voltage of 10 V leads to a higher output power and doubling efficiency.

In Fig. 8(b), there is a slight difference between the measured and simulated output power over the operating band from 215 to 222 GHz, which changes from 1.3 to 3.4 dB with different frequencies. One reason leading to the decrease in output power could be the mismatch between the proposed doubler and the adjacent driven multipliers in cascade, which can disturb the earlier stage and further reducing the efficiencies and output power. Moreover, another reason should be errors imported during circuit assembly, which makes the imbalance among junctions greater which directly decrease the output power and efficiency too. Interestingly, an output power of 14.5 mW is measured with a 46.4 mW input power at 214 GHz, which means an excellent peak efficiency of 31.25% is delivered, as shown in Fig. 8(b). The practical doubler exhibits higher output power and efficiency than the simulated one at this point. This interesting phenomenon might result from the undesired standing wave caused by circuits assembly, which pulls the impedance point towards the optimum operation point at 214 GHz and leads to a high conversion efficiency.

A summary of the comparison between measured performance with the reported frequency doublers is listed in Table 1, which indicates this doubler still needs some further improvement. At first, the doubler should be completed with gold-plated in future design, because the block without gold-plating might result in an imperfect diode grounding and lead to a decrease in efficiency. Then, substrates thinner than 50 μm would be tried to achieve less dielectric loss. Meanwhile, the diode welding process is under developing which provide a better stability compared with current adhesion process using the silver conductive epoxy. In this way, it is possible to improve the conversion efficiency and output power of this doubler.

4 Conclusions

A 220 GHz frequency doubler based on two discrete Schottky diodes with six junctions altogether has been developed. Influence of diode location and reduced-height waveguide have been discussed for high multiplying efficiency. Through the analysis of junction imbalance and optimization of matching networks, an output power of 32 mW and a peak efficiency of 21.5% have been reached at room temperature. The proposed doubler has delivered a high efficiency better than 16% over 214 ~ 226 GHz when pumped with 46 ~ 164 mW input power, which can be widely used in test instrument and radiometers.

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Table 1 Doubler performance comparison in WR-5.1 and WR-3.4 band
表 1 WR-5.1 和 WR-3.4 波段的倍频器性能比较

Ref.	Anodes	P_{in}/mW	Peak efficiency(P_{out})	Efficiency	Band(FBW%)	Comment
[7]	6	50 ~ 88	15%@190 GHz (13 mW)	7% ~ 15%	176 ~ 204 GHz (14%)	50 mm_quartz
[8]	6	100 ~ 200	40%@185 GHz (88 mW)	20% ~ 40%	172 ~ 190 GHz (15%)	-
[12]	6 * 3	175 ~ 325	29%@160 GHz (70 mW)	25%	144 ~ 172 GHz (13%)	Quadrupler
[17]	6	500	25%@190 GHz (120 mW)	~25%	170 ~ 200 GHz (16%)	50 μm_substrate
[18]	2	40 - 50	30%@332 GHz (14 mW)	15% - 30%	326 ~ 348 GHz (6.5%)	-
[19]	4	100 - 200	25%@160 GHz (35 mW)	15% ~ 30%	150 ~ 170 GHz (10%)	50 μm_substrate
[20]	6	20 - 60	30.5%@314 GHz (14.75 mW)	~16%	266 ~ 336 GHz (24%)	50 μm_substrate
This Work	6	46 - 164	21.5%@218 GHz (32 mW)	16% ~ 21.5%	214 ~ 230 GHz (8%)	50 μm_quartz

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