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STI-bounded single-photon avalanche diode with high photo current and low dark rate

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Abstract: A 0.18 μm CMOS process single photon avalanche diode (SPAD) was examined in this study in an effort to inhibit premature edge breakdown (PEB) and secure large photocurrent and low dark count rate (DCR). The SPAD consists of a p-well/deep n-well photosensitive junction and a guard ring as-formed by a deep n-well up-diffused region and an edge STI. The size of the STI layer related to the light current and dark rate was determined via test. The results indicate that the photocurrent and dark count of the SPAD are optimal when the overlapping length between the STI and guard ring is 1 μm at room temperature. The SPAD with 10 μm diameter has high photon detection probability (PDP), wide spectral response, dark count rate as low as 208 Hz, and 20.8% peak PDP when the wavelength is 510 nm. A 0.18 μm CMOS process single photon avalanche diode (SPAD) was examined in this study to inhibit premature edge breakdown (PEB) and secure large photocurrent and low dark count rate (DCR). The SPAD consists of a p-well/deep n-well photosensitive junction and a guard ring as-formed by a deep n-well up-diffused region and an edge STI. The size of the STI layer related to the light current and dark rate was determined via test. The results indicate that the photocurrent and dark count of the SPAD are optimal when the overlapping length between the STI and guard ring is 1 μm at room temperature. The SPAD with 10 μm diameter has high photon detection probability (PDP), wide spectral response, dark count rate as low as 208 Hz, and 20.8% peak PDP when the wavelength is 510 nm.

Key words: single-photon avalanche diode (SPAD), premature edge breakdown (PEB), dark count rate (DCR), complementary metal oxide semiconductor (CMOS), photon detection probability (PDP)

PACS: 85.60.Bt, 85.60.Dw, 85.30.-z

STI 埋层的高光电流和低暗计数率单光子雪崩二极管

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摘要:研究和分析了一种0.18 μm CMOS工艺单光子雪崩二极管(SPAD),其结构能抑制过早的边缘击穿(PEB),同时获得较大的光电流和低的暗计数率(DCR).该SPAD由p-well/deep n-well的感光结,deep n-well向上扩散形成的区域和边缘Shallow Trench Isolation(STI)共同形成的保护环组成.通过测试确定了与光电流和暗率有关的STI层的大小.结果证明,在STI层与保护环之间的重叠区域为1 μm时,SPAD的暗计数率和光电流最佳.此外,直径为10 μm的圆形SPAD器件的暗计数率为208 Hz,且在波长为510 nm时峰值光子探测概率为20.8%,此时具有低的暗计数率和高的探测效率以及宽的光谱响应特性.

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Biography: JIN Xiang-Liang (1974-), male, Professor. Research interests include MEMS and readout circuit design, CMOS image sensor design, ESD, and mixed-mode application-specific integrated circuits

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关 键 词:单光子雪崩二极管;边缘击穿;暗计数率;互补金属氧化物半导体;光子探测概率

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Introduction

Single-photon avalanche diodes (SPADs) are reversely biased PN junctions operating in Geiger-mode which are reverse-biased at voltages above the breakdown voltage. A sufficiently strong electric field in the depletion region makes an electron-hole pair trigger a self-maintained avalanche under large (i. e., above-breakdown) bias voltage which allows for the measurement of high current pulses[1]. SPADs are growing increasingly popular in a variety of scientific applications in chemistry, biology, and astronomy fields[2-3]. The CMOS SPAD, for example, containing a compact single chip has been utilized for quantum communication secrecy and photon counting applications such as infrared single photon detectors, fluorescence lifetime imaging microscopy, and 3D optical distance measurement[4-8]. Many researchers have explored SPADs with low DCR, low noise, small pixel size, and low breakdown voltage properties.

The PN junction SPAD with a narrow p+/n-well junction in deep sub-micrometer CMOS technology produces a high dark noise due to tunneling in the high n-well doping concentration[9-10]. Finkelstein *et al.* [9] fabricated the smallest SPAD structure to date, which has a 2 μm active diameter, by using a shallow trench isolation (STI) guard ring to prevent edge breakdown and increase fill factor. The DCR of this structure is extremely high (hundreds of kHz), however, due to the excess trap energy from the STI interface. The structure proposed by Richardson *et al.* in 2009[11] was later extensively researched[12]; it can be applied in 130-nm CMOS technology as-formed by lightly doped p-well and deep n-well layers with a virtual guard ring formed by a retrograde profile. The depletion region of the structure is wider than the p+/n-well SPAD, which minimizes tunneling noise and broadens the wavelength region due to the lower doping concentrations[11]. The SPAD structure can be reduced to a 2 μm active diameter with DCR of about 9 Hz[12].

STI significantly influences the dark count of SPAD devices; to be specific, upon connection to the device, STI increases the dark count. In this study, we tested several overlapping sizes of STI and guard ring (1 μm, 1.5 μm, 2 μm, and 2.5 μm) to explore the effects of STI in contact with the active region. We placed SPADs with different STI sizes in a 0.18 μm CMOS image sensor (CIS) technology in an effort to further scale down the DCR of the SPAD structure[12]. We were able to minimize the edge electric field and dark count when the active area was 10 μm and the STI/guard ring overlapping length was 1 μm, as discussed in detail below.

1 SPAD structure and simulation results

The SPAD depletion layer formed by the p^+/n-well becomes narrow and the breakdown voltage decreases with a decrease in the characteristic size and an increase in the doping concentration. These factors may produce a tunneling phenomenon rather than an avalanche breakdown. Here, we used a SPAD with a p-well/deep n-well junction in order to increase the breakdown voltage.

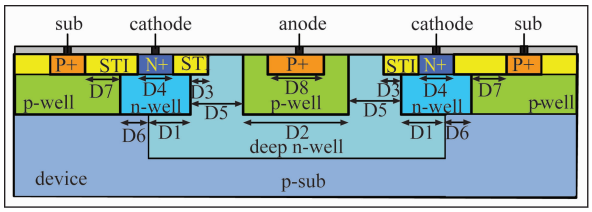


Fig. 1 The structure of SPAD

图 1 SPAD 结构图

As shown in Fig. 1, the SPAD consists of a p-well/deep n-well junction and an octagonal virtual guard ring formed by STI and a retrograde deep n-well. This structure design brings the doping concentration from a low level at the surface to a higher level deeper into the wafer. The p-well layer defines the active region for photodetection as it is the location of avalanche multiplication[11-12].

The doping concentration of the p-well and deep n-well is low, which creates a relatively wide depletion layer, weak electric field, and low probability of avalanche breakdown. The breakdown voltage of the device is relatively large. The high-efficiency SPAD with a narrow (2.5 μm) guard ring not only withstands high electric fields to prevent the edge breakdown, but also increases the filling factor. Here, we retain the STI on the outside of the guard ring for the sake of reducing its width. The various SPAD structure sizes we tested are described in table 1.

Table 1 The size of SPADs structure

表 1 SPADs 结构的尺寸

Device name	D1/μm	D2/μm	D3/μm	D4/μm	D5/μm	D6/μm	D7/μm	D8/μm
SPAD_STI_1	2.1	8	1.0	2.2	2.5	1.6	2.9	7
SPAD_STI_1.5	2.1	8	1.5	2.2	2.5	1.6	2.9	7
SPAD_STI_2.0	2.1	8	2.0	2.2	2.5	1.6	2.9	7
SPAD_STI_2.5	2.1	8	2.5	2.2	2.5	1.6	2.9	7

Several SPADs with different STI lengths were simulated in Silvaco TCAD. The structure of SPAD emulated in the Silvaco Altas is shown in Fig. 1. The cathode measures the output current while the anode and substrate are connected to the ground throughout the simulation process.

Figure 2 shows the electric field distributions under SPAD breakdown without STI and with STI. More importantly, it displays the field region located at the edge of the guard ring. Figure 2(a-b) shows that the center of the electric field is yellow, which reflects a higher elec-

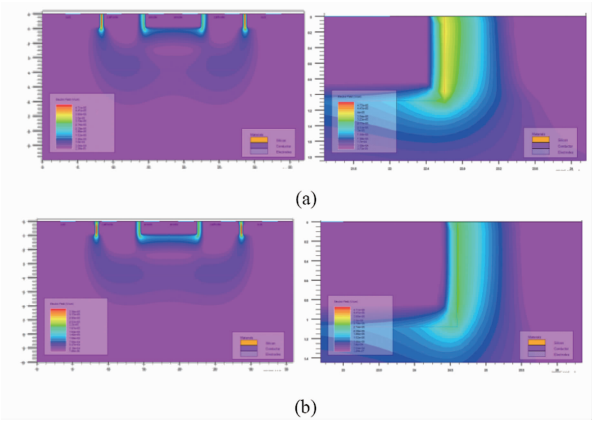


Fig. 2　The TCAD simulation results (a) SPAD without STI, and (b) SPAD with STI
图 2　TCAD 仿真结果(a)无 STI 的 SPAD,(b)有 STI 的 SPAD

tric field when the SPAD does not have an STI. Figure 3 shows the electric field around the anode in greater detail. The electric field of SPAD with STI is about 2.3×10^5 V/cm, 1.2×10^5 V/cm lower than the SPAD without STI, which is better resistant to edge breakdown effects as the dielectric strength of SiO_2 is 30 times higher than the breakdown field of silicon.

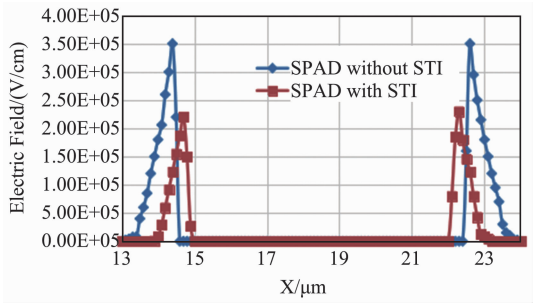


Fig. 3　Electric field around anode
图 3　阳极周围的电场分布

Figure 4 shows the 2D total current density profile at a 0.1 V excess bias voltage. There is a strong current density in the cathode region. Red circles mark regions with overlapping lengths between the STI and guard ring of 1.0 μm, 1.5 μm, 2.0 μm, and 2.5 μm corresponding to the current density of 0.6 A/cm^2, 0.4 A/cm^2, 0.2 A/cm^2, and 0.01 A/cm^2. The current density in the cathode region increases as the STI length decreases. The current density is largest when the overlapping length between the STI layer and the guard ring is 1 μm.

2　Experimental results and analysis of high photocurrent

A micrograph of the fabricated SPADs is shown in Fig. 5, in which the active regions are 10 μm, and different STI lengths are implemented in 0.18 μm CIS technology. The overlapping lengths between STI and the guard ring are 1.0 μm, 1.5 μm, 2.0 μm, and 2.5 μm.

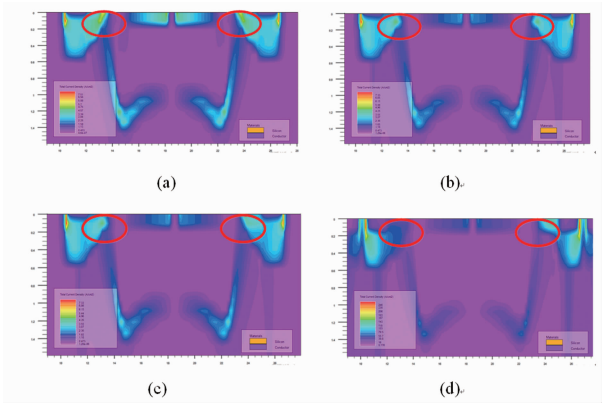


Fig. 4　The total current density of the overlapping length between STI and guard ring (a) 1.0 μm, (b) 1.5 μm, (c) 2.0 μm, and (d) 2.5 μm
图 4　STI 和保护环之间重叠长度(a)1.0 μm,(b)1.5 μm,(c)2.0 μm,(d)2.5 μm 的总电流密度

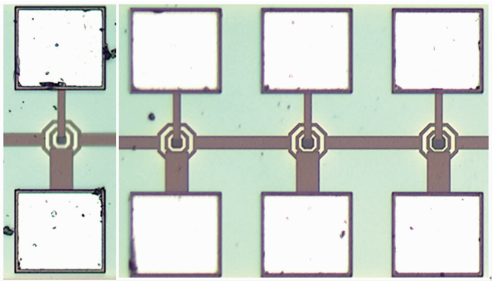


Fig. 5　Micrograph of the SPADs fabricated in 0.18 μm CIS technology
图 5　基于 0.18 μm 图像传感工艺的 SPAD 显微照片

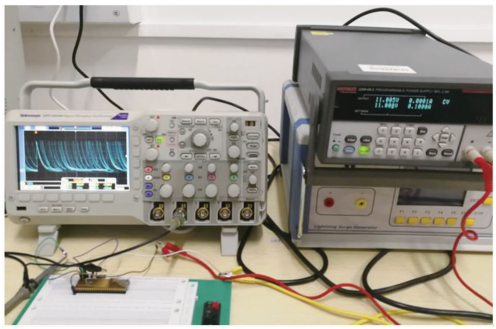


Fig. 6　Test platform of the SPAD with its quenching circuits
图 6　SPAD 的测试平台和淬灭电路

Figure 6 shows a test platform that consists of a DC power supply, digital oscilloscope, and the designed SPAD with its quenching circuits.

Figure 7 shows the reverse *I-V* characteristics of the SPADs measured with a Keithley B1505 A. The breakdown voltage of the SPADs is approximately 14.96 V, which exceeds the 14.36 V reported in the literature[11] due to the 0.13 μm CMOS technology, in which the doping concentration is relatively large and the breakdown voltage is small. The reverse *I-V* characteristic measure-

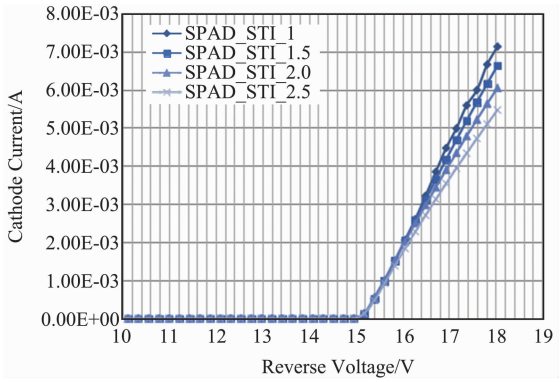


Fig. 7 *I-V* characteristics of the SPAD at room temperature
图 7 室温下 SPAD 的 *I-V* 特性

ments indicate that the SPADs with different STI lengths have the same breakdown voltage due to their uniform structure and impurity concentration distribution in the SPADs. The current increases as STI length decreases when bias voltage is kept constant.

Our results indicate that a current of the same excess bias voltage is maximized when the overlapping length between the STI and the guard ring is 1.0 μm. In other words, the length between the STI and p-well active region in the SPAD with 0.18 μm CIS technology can be scaled down to 1.5 μm.

3 Experimental results and low dark rate analysis

We conducted DCR measurements by counting the number of current pulses when the SPAD bias voltage exceeded the breakdown voltage in dark conditions. Figure 8 shows a diagram of the test circuit. The SPAD cathode was connected to a voltage source V_A ($V_A = V_{EX} + V_{BR}$), in which V_{EX} is the excess bias voltage and V_{BR} is the breakdown voltage. The SPAD anode was connected to the ground through a high-value quenching resistance

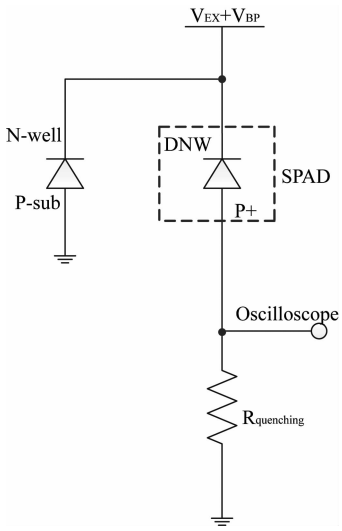


Fig. 8 Measurement circuit of the SPAD device
图 8 SPAD 的测试电路

$R_{quenching}$, which is usually tens of kΩ and here was 51 kΩ. The SPAD anode was also connected to a high resolution oscilloscope to count DCR; the SPAD substrate was connected to the ground.

The DCR of SPAD was measured at excess bias voltage V_EX (ranging from 0.1 V to 1.1 V with a 0.1 V step) at 25℃ as shown in Fig. 9. We found that the DCR increases linearly with increase in V_{EX} as avalanche breakdown probability increases and tunneling carrier is generated. The DCR also differs significantly with STI length at the same excess bias voltage. The DCR decreases as the size decreases as the active region and n-well are separated from the STI to prevent interface traps. A smaller overlapping size between the STI and guard ring makes for a lower DCR. The DCR, which varies from 0.02 kHz to 0.96 kHz, is lowest when overlapping size is 1.0 μm, at which point V_{EX} increases from 0.1 V to 1.1 V.

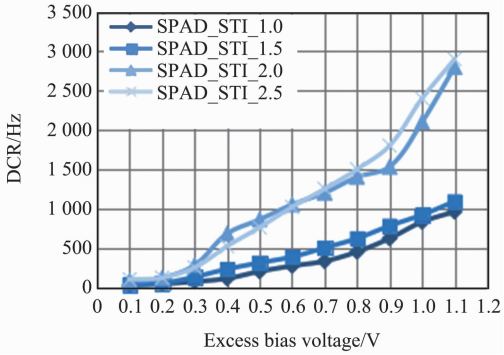


Fig. 9 The DCR of SPAD at different excess bias voltage
图 9 不同过偏置压时 SPAD 的 DCR 特性

Figure 10 shows the DCR of the SPADs, in which V_{EX} is constantly 1.0 V and temperatures range from 0 °C to 60 °C. The DCR is markedly enhanced at higher temperatures due to an improvement in the avalanche breakdown probability and band-to-band tunneling carrier generation under constant excess bias voltage[12, 14]. The lowest DCR of the four SPADs increases from 0.3 kHz to 2.01 kHz.

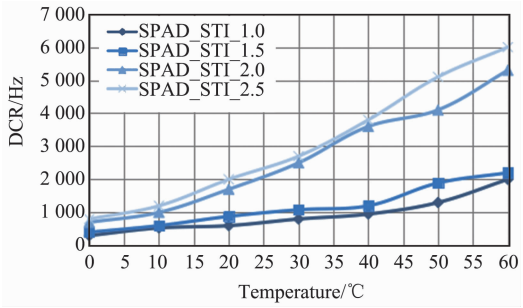


Fig. 10 DCR vs. temperature
图 10 不同温度对 SPAD 的 DCR 特性

4 Photon detection probability

Figure 11 shows the photon detection probability (PDP) of the SPAD, i.e., the ratio of the number of

photons detected and the number of photons emitted. We measured PDP over a wavelength ranging from 200 nm to 1 100 nm at room temperature with an excess bias voltage of 0.4 V. The overlapping length between the STI and guard ring appears to significantly affect PDP. The peak value wavelength of PDP increases as the STI length decreases. The peak PDP is 20.8% at 510 nm, which is higher than the previously reported 20%[15] when the excess bias voltage is 0.4 V. We also observed a broader spectral response moving towards longer wavelengths with a peak value wavelength of about 510 nm. The peak wavelength of SPAD published previously is 430 nm[15].

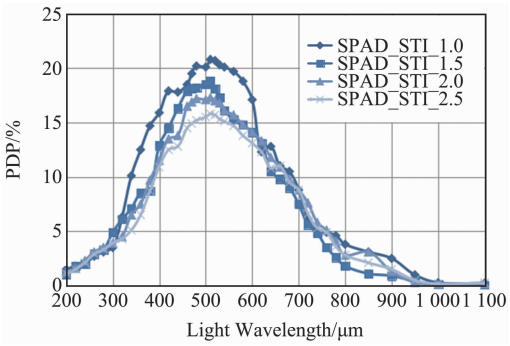


Fig. 11　Measured PDP of the SPADs with varied STI lengths

图 11　不同 STI 长度 SPAD 的光子探测概率测试结果

5 Conclusion

In this study, the SPAD with an overlapping length of 1 μm between the STI and guard ring was found to inhibit PEB and produce a larger photocurrent as well as lower DCR in comparison with other overlapping area sizes in 0.18 μm CIS technology. Our measurement results indicate that the DCR of SPAD is 208 Hz and that the PDP of SPAD is 20.8% at 510 nm wavelength and room temperature. The *I-V* curves demonstrate that the breakdown voltage is about 14.96 V. To this effect, the SPAD performance can be markedly improved and the SPAD can be effectively integrated with a readout circuit.

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