Simulation of the electrical properties of Al₂O₃/GaSb p-MOSFET

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Abstract: To study the high-field electrical property and the drain current $I_d/I_n$ ratio of Al₂O₃/GaSb p-MOSFET, the Poisson and continuity equations with carrier velocity saturation were solved consistently with two-dimensional numerical analysis. The simulation results show that a maximum drain current of 61.2 mA/mm has been reached for 0.75-μm-gate-length GaSb p-MOSFET device. The results have been compared with that of experiment. With change of the channel length and doping-level in substrate GaSb, the drain currents exhibit little change due to the effects of gate capacitance with high-$k$ dielectric and low-threshold voltage. In addition, a high $I_d/I_n$ ratio with more than three orders of magnitude and relatively low pinch-off leakage current $I_{off}$ with $10^{-5}$ A/μm are predicted in an ideal condition. The results indicate that GaSb-based MOSFET with high-$k$ dielectric is promising for future p-channel III-V device.

Key words: Al₂O₃/GaSb p-MOSFET, saturation current, the Poisson and continuity quations, $I_d/I_n$ ratios

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Al₂O₃/GaSb p-MOSFET 器件电学性质模拟

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摘要: 利用泊松方程和连续性方程对 Al₂O₃/GaSb p-MOSFET 进行二维数值分析, 研究其在高场和载流子速度饱和下的光电特性以及漏极电流的开关电流比, 与实验研究相对比, 源漏长度为 0.75 μm 的 GaSb p-MOS 器件获得漏极电流最大为 61.2 mA/mm, 改变源漏长度和 GaSb 导带的掺杂浓度, 由高 $k$ 介质层的的密度和低横向电压, 漏极电流变化不大, 在理想条件下, 该器件获得超过三个数量级的漏极开关电流比以及较低的开关漏电流 ($10^{-5}$ A/μm)。结果表明, 高 $k$ 介质的 GaSb MOSFET 是 III-V 族 p 沟道器件良好的候选材料。

关键词: Al₂O₃/GaSb p 型场效应晶体管; 饱和电流; 泊松方程与连续性方程; 开关电流比

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Introduction

In recent years, the III-V materials have been studied extensively in the application of complementary metal oxide semiconductor (CMOS) [12], playing important roles of generating channel materials and even excellent performance than silicon-based technology. Due to lack of high quality insulator-semiconductor interface with thermodynamic stability and lower trap density[13], the III-V materials technology are impeded in CMOS application. Until now, III-V compound semiconductors CMOS technology has made a significant progress. Structures have been improved through integration of high-$k$/III-V interface[43], by using high-quality growth process of high-dielectric insulator instead of SiO₂. The high-$k$ dielectric insulating layer can be thinner than SiO₂ without
introducing significant defects. Since the smaller feature size of MOSFET appeared and reducing thickness cause the tunneling leakage current, the high-k dielectric materials can overcome these obstacles to increase physical thickness of gate dielectric layer with the equivalent thickness unchanged. As for the surface channel transistors, the channel material must have appropriate band gap (E_g), in order to maintain a certain standard on-off ratio (I_on/I_off). Although most III-V materials do not reach particularly high hole-mobility, the III-V p-MOSFETs have made some progresses\(^6\).\(^4\)

Gallium antimonide (GaSb) is an attractive material for p-MOSFET devices. The hole mobility is 1 000 cm\(^2\)/Vs, much higher than most of other III-V materials\(^9\). The charge neutrality level for GaSb is 0.1 eV above the edge of valence band\(^10\), making it possible to obtain lower resistivity in the source/drain contacts of the GaSb p-MOSFET. In fact, it has been reported that the contact resistivity value of p-type GaSb is less than\(^11\) 1 \(\times 10^{-5}\) \(\Omega\) \(\cdot\) cm\(^2\). The band gap of GaSb is around 0.73 eV. These unique properties make hole transport of MOSFET easily to be achieved in strong inversion conditions. Compared with other III-V materials, GaSb-based optoelectronic integration achieves a minimum consumption of energy in the field of photoelectric communication and obtains higher switch-off ratio (I_off/I_on). Since the drain current (I_D) of a MOSFET depends not only on the carrier mobility and saturation velocity, but also depends on the charge density in inversion layer. It leads to the pursuit of GaSb-based p-type device due to the high effective density of states of the valence band. Therefore, GaSb is a potential candidate for future p-channel material\(^12\). Recent years have witnessed the experimental study on the Al\(_2\)O\(_3\)/GaSb p-MOSFET\(^13\), while it still lacks of the reliable numerical technique for performance estimation and structure optimization. To this regard, we deal with numerical analysis of the high-field electrical properties of Al\(_2\)O\(_3\)/GaSb p-MOSFET with a two-dimensional numerical simulation taking into account effects of electrical contact, device structure and doping of the charge-neutral region.

1 Device modeling and simulation

The Al\(_2\)O\(_3\)/GaSb MOSFET device was simulated by ISE-TCAD software. The basic equations for charge transport are the Poisson equation and the electron and hole continuity equations. The drift-diffusion model was used for the simulation of carrier transport. The generation-recombination models include Shockley-Read-Hall (SRH) recombination, which is considered as the recombination process through deep levels in the gap, and Auger recombination. Fermi statistics is activated for the whole device. High electric field saturation effect and doping dependence are considered in the mobility model. High field saturation is driven by a field computed as the gradient of the carrier quasi-Fermi level. In the mobility degradation model, electric field normal to GaSb-oxide interface is used. The band-gap narrowing that determines the intrinsic carrier concentration need to be considered as well.

With the theoretical model well-established, a two-dimensional Al\(_2\)O\(_3\)/GaSb MOSFET device simulation was performed. As shown in Fig. 1, the source/drain regions are p-type silicon, doping with boron (B). While the substrate is n-type GaSb, doping with arsenic (As), and the gate oxide is high-k dielectric of Al\(_2\)O\(_3\). We consider the channel doping concentration of 5.5 \(\times 10^{17}\) cm\(^{-3}\) and the oxide layer of 8 nm. The length of cross section is 2 \(\mu\)m with the channel length of 0.75 \(\mu\)m and the width of 0.6 \(\mu\)m. In order to demonstrate the reliability of device simulation results, similar experimental data of the Al\(_2\)O\(_3\)/GaSb p-MOSFET structure is shown along with our simulated results\(^13\), for the sake of comparison and contrast. However there is a little difference that we considered the source/drain regions as p-type Si with the same doping concentration of 5.5 \(\times 10^{17}\) cm\(^{-3}\) instead of a high Si implantation dose of\(^6\) 2 \(\times 10^{15}\) cm\(^{-2}\), for the temperature controlling is not taken into account in this paper.

2 Simulation results and discussion

2.1 Comparative analysis of the theoretical simulation with experimental result

With a similar structure to the experimental one, the DC output characteristics were demonstrated. Fig. 2 shows the output characteristic of simulated and experimental devices under different gate biases. Besides, it’s worth noting that the direction of current in this paper is from drain to source. From Fig. 2 (a), it can be seen that the drain current reaches 61.2 \(\mu\)A/\(\mu\)m at \(V_{DS} = -4\) V, \(V_{GS} = -3\) V. According to the results from experiments, the drain current reaches 70 mA/mm (Fig. 2 (b)), a maximum value under the same doping concentration of channel and bias as the simulation\(^13\). Although the saturation current in simulation is lower than the experimental one, the drain current is approximately the same trend in 0.5 V step of gate voltage when compared with the tested results. When the drain voltage approaches -3 V, current-voltage characteristic curve of analyzed devices becomes smoother and near good saturation, while the experimental data exhibits continuously increment.

Since the contact resistance of the drain/source electrodes can cause the drain voltage drop in series with channel resistance, the actual drain voltage is influenced by the contact resistance. The contact resistance inclu-
ding the tunneling, and depletion of carriers and short channel effects, would lead to the poor saturation in the experimental situation. In order to investigate whether the drain saturation current is 61.2 mA/mm with $V_{GS} = -4$ V, $V_{DS} = -3$ V, we decrease the contact resistance in the simulation process, so that the drain current can reach saturation as soon as possible. From the diagram in Fig. 3, we can see that the drain current reaches the maximum value of 74.1 mA/mm, which is larger than the value during experimental measurements.

![Fig. 2](image1.png)  
**Fig. 2** (a) Characteristic curves of $I_{DS}$-$V_{GS}$ in simulation, (b) Characteristic curves of $I_{DS}$-$V_{DS}$ in experiment

2.2 Simulation results and discussion in different conditions

2.2.1 Changes in channel length

Based on the above device structure, we tried to discuss about the effect of channel length on I-V characteristics. In Fig. 4 (a), obviously, there is no rigid change of current through increasing the gate length. Fig. 4 (b) depicts the transfer characteristics with the change of channel length under the same gate bias sweeping. The drain current of 0.6 μm is larger than other ones at the beginning, but when the gate bias swept over -3.5 V, the current of 0.75-μm gate length is the biggest. While, the figure in the inset of Fig. 4 (B) shows that the threshold voltage is almost the same under different channel length.

To demonstrate the above phenomenon qualitatively, we simplified the analysis of Poisson equation and continuity equations, the DC output characteristics of p-MOSFETs in linear region can be written as:\(^{(14)}\)

$$I_{DS} = \frac{C_0 \mu_p Z}{L} \left( (V_{GS} - V_{TH}) V_{DS} - \frac{V_{DS}^2}{2} \right), \quad (1)$$

where $C_0$ is per unit area of gate capacitance, $\mu_p$ represents the mobility of holes, $V_{TH}$ is threshold voltage. The values of $Z/L$ adopted are 0.6/0.6, 0.6/0.75, 0.6/1 respectively. The threshold voltage value is invariant under different channel length. From equation (1-1), $C_0$ needs to be considered under different channel length. Fig. 4C shows the high frequency (1MHz) C-V (gate capacitance-gate voltage) curves for the device with different channel length. With increasing channel length, the corresponding $C_g$ value increased regularly. Thus, with the values of $Z/L$ progressively decreased and Cg values increased non-monotonously, we can explain the phenomenon from Fig. 4 (a) that the maximum drain current is a 0.75-μm-gate-length device with $V_{GS} = -4$ V, $V_{DS} = -3$ V, but at the bias of $V_{TH} = -3$ V, $V_{DS} = -3$ V, the maximum drain current is the device of 0.6-μm-gate-length. Therefore, the drain current depends non-monotonously on the gate voltage, which is due to the contact at source and drain.

In addition, the 0.6-μm-gate-length drain current is 54.5 μA/μm at a gate bias of -4 V and a drain bias of -3 V, which is greater than or equal to saturation current of other III-V materials. The $I_{DS}$ is indeed larger than the value reported on GaAs p-MOSFET ($I_{DS} \sim 50$ mA/mm with $L_g = 0.6$ μm) by Passlack et al\(^{(8)}\).

2.2.2 Changes in doping concentration

Based on the above simulation structure, the effects of doping levels on the electrical properties of GaSb p-MOSFET was studied in this section. In this paper, doping concentration is changed both in the n- and p-type regions. After comparing the output characteristics of GaSb p-MOSFET with different doping concentration un-
increasing the doping in the GaSb neutral region. To analyze further the results, we calculate the transfer characteristics as well (Fig. 5 (b)). The transfer characteristics results show that the drain current with lowest doping contents is larger than other ones at the beginning, but when the gate bias added up to over -3.25 V, the middle value of doping contents is the largest. The figure in the inset also shows that the threshold voltage value is increased by increasing doping concentration. In addition, increasing doping concentration in n-type region can cause the reduction of the hole mobility, although p-type region is highly doped to increase the carrier concentration. Hence, combined with Eq. (1), the drain current does not increase monotonously while increasing doping levels. So choosing advisable doping doses should be taken into account in order to reach drain current as high as possible.

Fig. 4 (a) The $I_{ds}$-$V_{ds}$ curves of different channel length; (b) The transfer characteristics curves of different channel length at $V_{ds} = -3$ V. The inset at the top-right corner is the same transfer characteristics curves with gate bias between -1.6 V to -2.0 V; (c) High frequency (1MHz) gate capacitance-gate voltage measurement on GaSb p-MOSFET with different channel length

2.3 The on-and-off-state performance of GaSb p-MOSFETs simulation

The on-and-off-state can be described by the $I_d/I_{off}$ ratio. The current is measured under the bias of gate voltage above threshold and below the threshold with the
same drain bias. A high \( I_{on}/I_{off} \) ratio is anticipated to make good gate control in logic application.

The on/off ratio in different gate voltages is simulated and the corresponding \( V_{GS}-I_{on}/I_{off} \) curve is demonstrated (Fig. 6). With increasing gate bias, the \( I_{on}/I_{off} \) ratios demonstrate more than three orders of magnitude and the off state current is \( 10^{-15} \) A/\( \mu \)m. According to the requirement of manufacture process, transistors must have high \( I_{on}/I_{off} \) ratio and low off state. The on/off ratio of the device evidently meet the demand. GaSb p-MOSFET, therefore, performs a good controllability.

3 Conclusions

The simulation of Al\(_2\)O\(_3\)/GaSb p-MOSFET device has been accomplished to study the electrical property and the drain current \( I_{on}/I_{off} \) ratio of Al\(_2\)O\(_3\)/GaSb p-MOSFET. The maximum drain current of 61.2 mA/mm has been obtained for 0.75-\( \mu \)m-gate-length device. The saturation drain current can be increased by reducing the contact resistances between the drain/source electrode and channel. With change of channel length and doping concentration in substrate, the drain currents demonstrate non-monotonously change due to the interplay effect of gate capacitance, threshold voltage, and contact resist-ance. In addition, high \( I_{on}/I_{off} \) ratios with more than three orders of magnitude and a lower off state with \( 10^{-15} \) A/\( \mu \)m were obtained in an ideal simulation condition.

The results of simulation show that GaSb based p-MOSFET integrated with high-k dielectric is a good candidate for logic application.

References