Design of a D-band balanced frequency doubler with quartz substrate

GUO Jian, XU Zheng-Bin, QIAN Cheng, DOU Wen-Bin
(State Key Laboratory of Millimeter Waves, Southeast University, Nanjing 210096, China)

Abstract: A D-band frequency doubler with quartz substrate is proposed in this paper with commercial planar Schottky diodes DBES105a. The balun in the doubler is implemented by fine-line-suspended-stripline coupler (FSSC). The waveguide-to-fine line transition suit for quartz substrate has only 0.15 dB measured insertion loss. Compared with traditional coupler in balanced doubler and mixer designs, it has the advantage of easier bias for the diodes. Measured results of the doubler showed that the maximum output power is 3.39 mW with 0.4 V reverse bias voltage and 26.3 mW drive power. Its corresponding peak efficiency is 12.9%. The output power of the doubler is reduced from 3.1 mW to 2.0 mW when the bias voltage deviates from its optimum bias condition. The finding shows that proper external DC bias for Schottky varistor multiplier is as important as for the varactor diode frequency multiplier.

Key words: D-band; balanced frequency doubler; quartz substrate; fine-line-suspended-stripline coupler; DC bias

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Introduction

Used as local oscillator (LO) for the heterodyne receivers in Millimeter-wave and submillimeter-wave systems, solid-state frequency multipliers using planar schottky diodes are becoming more popular, especially in high resolution atmosphere and astronomy fields[1-2]. Performances of these multipliers have been kept improving for the last two decades, with the development of advanced process and design approach. One example is that, the output frequency of the schottky varactor multiplier can reach around 3 THz with 0.1 μW output power[3]. It is powerful enough to drive hot electron bolometer (HEB). Other types of frequency sources, such as backward oscillator (BWO) and far-infrared (FIR) laser, will be gradually substituted by Schottky diodes multipliers. This is because of the advantages of Schottky multipliers: more compact, less power consuming, and more reliable. These make them especially suitable for airborne and space application, such as SOFIA[2] and Herschel Observatory[1] and so on.
Generally there are two types of Schottky diodes for the design of frequency multiplier: Schottky varactor and Schottky varistor. Varactors are adopted for high power and high efficiency frequency multipliers, while the varistors could be used for broadband application. Researchers at Jet Propulsion Laboratory (JPL) and Virginia Diode Inc. (VDI) benefited from their extraordinary Schottky varactor diode and multiplier chip process, and outstanding performances have been fulfilled. European scientists have designed and fabricated mixers and multipliers with their local diode process for the past few years, which is the berried-epilayer-Schottky (BES) varistor from UMS, France.

The D-band frequency doubler in this paper adopted the commercial schottky varistor DBES105a. It is also fabricated by UMS BES process. It is widely believed that the DC bias is vital for varactor frequency multipliers to achieve optimum performance, but few of the published varistor multipliers are working under DC bias. In this paper, DC bias for the varistor frequency multipliers has been investigated and the findings are described in later sections of this paper.

The remainder of this paper is organized as follows. Section 1 describes the design of proposed balun coupler. Section 2 illustrates the design of waveguide-to-finline transition. Section 3 focuses on the design of balanced frequency doubler. Section 4 are the measurements and findings. Conclusions are drawn in Section 5.

1 Design of the balun coupler for balanced frequency doubler

Balun coupler is the heart of a balanced frequency doubler, while finline-suspended-stripline coupler (FSSC) is a popular implementation, because of the quasi-planar configuration and the ease of fabrication and mounting. As balanced frequency doubler only produces even harmonics, it can simplify the design of the idler circuits. Comparisons between the architecture of balanced frequency doubler using traditional FSSC and the proposed one in this paper are shown in Fig. 1. The traditional frequency doubler with anti-parallel-series diodes is shown in Fig. 1 (a), where the suspended stripline (SSL) operates as the input port and the finline as the output port. The configuration proposed in this paper with anti-series diodes is merely on the contrary, as shown in Fig. 1 (b). In both of the configurations, input signals arrive at the two diodes out of phase, while the output second harmonics produced by the diodes are combined in phase. However, the anti-series configuration in Fig. 1 (b) is the better choice in terms of getting the two diodes easily biased by an external DC voltage. The cathodes of the two diodes connected to two fins are in the same voltage potential, as they are bonded to the same metal channel. Thus the metal channel provides both DC and RF grounding. The DC bias is fed to the diodes via a hammer-head low-pass filter connected to the probe for SSL-to-waveguide transition.

Fig. 1 Architectures for balanced frequency doubler (a) anti-parallel-series diodes, (b) anti-series diodes

2 Design of the waveguide-to-finline transition

The waveguide-to-finline transition should provide both RF and DC groundings as mentioned above. Serrated-end finline tapper is usually adopted for waveguide to finline transition, either open-ended or short-ended style. The short-ended one is preferred because the fins are bonded to RF and DC ground. However, experimental results show that the short-ended one has higher insertion loss. That means neither of these two transitions is suitable for this balanced frequency doubler application. The finline transition with vias is also popular for soft substrate. Two rows of vias are arranged on both ends of the finline, which are then bonded to the metal block by conductive epoxy. But this transition still could not be applied on quartz substrate, as the via process on quartz substrate is not available under most situation.

The transition method adopted in this paper is il-
The measured two port S-parameters agree well with simulated ones. The return loss ($S_{11}$) is more than 15 dB from 75 to 90 GHz, and the insertion loss ($S_{21}$) is less than 0.3 dB (0.15dB for each transition) at 75 GHz, which verifies the validity of the transition method.

3 Design of the balanced frequency doubler

The doubler design begins with the modeling of the diode DBES105a. This diode uses the UMS BES process, so the three-dimensional (3D) architecture is slightly different from the traditional Schottky diodes. The Epilayer of the BES diodes is buried in the buffer layer without air channel in the surface. The 3D modeling of the BES diode in HFSS is similar to the one described by Saini\textsuperscript{[15]} by treating the buffer layer as perfect conductor and adopting a coaxial port at the Schottky contact. The chip DBES105a actually includes two diodes in series. In order to extend the application frequency, the chip was usually cut into two halves to reduce the parametric capacitance and inductance\textsuperscript{[15-16]}. Similar manipulation has been done in this paper by shorting one of the diodes with conductive epoxy.

The key step of the doubler design is to derive the input and output matching impedances. To do this, the models of FSSC and the diode were built in HFSS, which is a 4-port network, including the input finline port, the output SSL port and two coaxial ports each for two diodes. Then, the simulated 4-port S parameters were exported to ADS. The optimum impedances are obtained by the optimization for maximum doubling efficiency. The optimum input impedance is ($10 + j5$) Ohm and output impedance is ($249 + j167$) Ohm. Third, the matching circuits were designed in HFSS according to the optimum impedances. The input matching circuit was fulfilled by step impedance finline, while the output matching circuit was realized by step impedance SSL.

<table>
<thead>
<tr>
<th>Table 1 Dimensions of D-band frequency doubler</th>
<th>表 1 D 频段倍频器的主要尺寸</th>
</tr>
</thead>
<tbody>
<tr>
<td>Parameters</td>
<td>$a_1$</td>
</tr>
<tr>
<td>Sizes/mm</td>
<td>2.54</td>
</tr>
</tbody>
</table>
Finally, all the models in HFSS were combined and simulated in HFSS. The structures are shown in Fig. 4. The key parameters of the channel and matching circuits are listed in Table 1.

4 Test of the D-band frequency doubler

The quartz substrate and the module for the D-band doubler were fabricated and tested. The test bench is illustrated in Fig. 5. An E-band MMIC frequency doubler is excited by Agilent signal generator E8257D to drive the D-band doubler under test. Power meter PM4 with waveguide transition from WR-28 to WR-6 is used to measure the output power of the D-band frequency doubler. The output power of the E-band MMIC frequency doubler is given in Fig. 6.

Measured results of the doubler are illustrated in Fig. 7. The output power without the input isolator presents more than 12 dB ripple. One main reason is poor output VSWR of the E-band drive doubler. And the ripple is obviously reduced after adding an E-band isolator with 75 GHz center frequency and 2 GHz bandwidth, with only 4 dB range now. However the output power is reduced because of the 1 dB insertion loss of the isolator. The maximum output power without the isolator is 3. 39 mW when the diodes is reverse biased at 0. 4 V with 14. 4 dBm drive power.
and the peak conversion efficiency is about 12.9% calculated from:

\[
\eta = \left( \frac{P_{in}}{P_{out}} \right) \times 100\% \tag{1}
\]

where \( P_{in} \) is the input power of the doubler, and \( P_{out} \) is the output power of the second harmonic. The output power with the input isolator is 1.05 to 1.97 mW at the frequencies from 147.6 to 152.4 GHz, and the corresponding efficiency is 4.9% to 9.2%.

The measured output power of the doubler at 150 GHz with different diode bias voltages is shown in Fig. 8. The drive power is 26.3 mW. It can be seen that the optimum diode bias voltage is about -0.2 V with 3.1 mW output power. Any bias voltage higher or lower than -0.2 V will decreases the output power, which verifies that the varistor frequency doubler could achieve higher output power with an external bias.

The comparisons between the performance of our doubler and other reported ones are listed in Table 2. It shows that our doubler presents higher output power and conversion efficiency than the ones also designed with DBES105a varistor, but not as good as the varactor frequency doubler both in output power and conversion efficiency.

![Figure 8: Output power vs. bias voltage of the D-band frequency doubler](image)

**Table 2: Summary of previously reported frequency multipliers and this work**

<table>
<thead>
<tr>
<th>Harmonics</th>
<th>Devices</th>
<th>( f_{out} ) GHz</th>
<th>( P_{out} ) dBm</th>
<th>Conversion Efficiency (%)</th>
<th>Year</th>
</tr>
</thead>
<tbody>
<tr>
<td>2</td>
<td>VDI</td>
<td>190 – 200</td>
<td>185 – 195</td>
<td>9 – 10</td>
<td>1999</td>
</tr>
<tr>
<td>2</td>
<td>JPL</td>
<td>180 – 260</td>
<td>180 – 198</td>
<td>18.6 – 21.1</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>Varactor</td>
<td>2 – 11</td>
<td>12 – 18</td>
<td>0.6 – 2.1</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>VDI</td>
<td>180 – 190</td>
<td>114 – 135</td>
<td>30.6 – 33.5</td>
<td>2001</td>
</tr>
<tr>
<td>2</td>
<td>Varactor</td>
<td>140 – 160</td>
<td>133 – 160</td>
<td>10 – 15</td>
<td></td>
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<tr>
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<td>13.3</td>
<td>3.5</td>
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</tr>
<tr>
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<td>Varactor</td>
<td>13.3</td>
<td>0.2 – 2.9</td>
<td>12.9</td>
<td></td>
</tr>
</tbody>
</table>

**5 Conclusions**

The design of the D-band frequency doubler with quartz substrate has been introduced in this paper. The structure and assembly of the waveguide-to-fineline transition were also introduced. The effectiveness of the transition has been verified by simulation and measurement, with only 0.15 dB insertion loss. Based on the transition, the frequency doubler was built using FSSC. It has the advantages of biasing the diodes easily. Measured results show that the maximum output power is 3.39 mW with 12.9% conversion efficiency. Compared with other reported frequency multipliers also designed with varistors, it shows higher output power and conversion efficiency. That means by finding the optimum bias voltage, the doubler’s power performances can be improved correspondingly.

**REFERENCES**


[18] [OL]. http://vadiodes.com/

