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A high output power 340 GHz balanced frequency doubler designed based on linear optimization method

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Abstract: In this paper, a linear optimization method (LOM) for the design of terahertz circuits is presented, aimed at enhancing the simulation efficacy and reducing the time of the circuit design workflow. This method enables the rapid determination of optimal embedding impedance for diodes across a specific bandwidth to achieve maximum efficiency through harmonic balance simulations. By optimizing the linear matching circuit with the optimal embedding impedance, the method effectively segregates the simulation of the linear segments from the nonlinear segments in the frequency multiplier circuit, substantially improving the speed of simulations. The design of on-chip linear matching circuits adopts a modular circuit design strategy, incorporating fixed load resistors to simplify the matching challenge. Utilizing this approach, a 340 GHz frequency doubler was developed and measured. The results demonstrate that, across a bandwidth of 330 GHz to 342 GHz, the efficiency of the doubler remains above 10%, with an input power ranging from 98 mW to 141mW and an output power exceeding 13 mW. Notably, at an input power of 141 mW, a peak output power of 21.8 mW was achieved at 334 GHz, corresponding to an efficiency of 15.8%.

Key words: linear optimization method (LOM), three-dimensional electromagnetic model (3D-EM), Harmonic impedance optimization, Schottky planar diode, Terahertz frequency doubler

基于线性优化法设计的高输出功率340GHz平衡式二倍频器

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摘要:报道了一种用于太赫兹电路设计的线性优化方法,以提高仿真效率,缩短整个电路设计流程的时间。该方法通过谐波平衡仿真来快速得到在相应带宽内二极管的最佳效率的嵌入阻抗,然后通过该阻抗进行线性匹配电路的优化,从而将倍频电路的线性部分与非线性部分的仿真分离,极大地提高了仿真速度。片上线性匹配电路设计采用分块电路设计的方法,引入了固定负载电阻以简化匹配问题。基于该方法设计了一款340 GHz二倍频器并进行了验证。测试结果显示,在330 GHz到342 GHz的带宽内,倍频器的效率在10%以

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上,输入功率的范围在98 mW到141 mW之间,输出功率在13 mW以上。当输入功率为141 mW,在334 GHz处测得峰值输出功率为21.8 mW,对应的效率为15.8%。

关 键 词:线性优化法;三维电磁场模型;谐波阻抗优化;肖特基平面二极管;太赫兹二倍频器
中图分类号:TN771 **文献标识码**:A

Introduction

In recent decades, the demand for millimeter-wave and submillimeter-wave power sources has surged, driven by the expanding application of terahertz technology in fields such as remote sensing, high-speed communication, and radio astronomy[1-4]. Currently, there are two primary methods for generating terahertz sources: optical solutions, including far-infrared lasers, femtosecond infrared lasers, photoconductors, and Quantum Cascade Lasers (QCLs)[5-7], and electronic solutions, comprising vacuum electronic devices[8-11]and solid-state circuits[12, 13]. Due to the high quality, low cost, high reliability, and compact structure of frequency multiplier chains made from Schottky diodes, they have emerged as the leading choice for terahertz source solutions.

As the mainstream technological solution for terahertz sources, research on Schottky diode frequency doublers has been increasing. The principle of frequency doubling with Schottky diodes primarily utilizes the diode′s nonlinear characteristics, including varactor and varistor properties, to generate harmonic components at corresponding frequencies, which are then extracted and output through an E-plane waveguide probe structure. Varactor diodes excel in delivering higher power outputs with superior efficiency, whereas varistor diodes are distinguished by their ability to provide wider bandwidths. Balanced frequency doublers[14-18] and balanced triplers [19-23] have become standard topological structures for frequency multiplication, as their inherent topologies suppress unneeded harmonics and reduce the need for filtering structures, thereby enhancing broadband characteristics and greatly improving frequency multiplication efficiency. To date, all-solid-state frequency multiplier chains utilizing Schottky diodes have reached operational frequencies of up to 2.7 THz [24]. To ensure sufficient driving power for the final stage of the frequency multiplier chain, it is crucial that the driving power input by the preceding stages is adequately high. However, limitations due to the number of anode junctions and the power capacity of the materials impose an upper limit on the power capacity of individual circuits. Techniques such as in-phase power combining[25-29]and on-chip power combining[30] have been proposed to solve this problem. However, this results in a considerable expansion of the circuit′s scale, subsequently leading to a marked increase in the duration required for nonlinear simulations throughout the design process. Consequently, optimizing simulation design methods is crucial for enhancing the design efficiency.

The popular approach in terahertz circuit design combines three-dimensional electromagnetic field models with diode SPICE models through the coaxial probe method, enabling accurate prediction of the circuit performance. However, the specific implementation processes of different methods each have their own variations. The subdivision design method (SDM) [31, 32]divides the circuit into multiple independent unit structures, each optimized through 3D-EM simulations. The global design method (GDM)[33] deconstructs the entire circuit into a series of variables that can be optimized, increasing the degree of freedom for optimization but also the computational load, requiring substantial system resources. The half-global design method (HGDM)[34] merges these strategies, balancing computational load with optimization flexibility.

However, regardless of how 3D-EM is segmented into units in these mentioned design methods, the final simulation optimization still occurs within harmonic balance simulation software, thus the simulation speed is constrained by the speed of harmonic balance simulations. Recently, some efforts have been made to separate linear and nonlinear circuits [35, 36] to increase simulation speed. However, these methods only separate the waveguide and circuit components, resulting in the inability to optimize the matching structures near the diode units within the linear circuit. This limitation, crucial for frequency doubling circuit performance, consequently increases the workload.

This paper introduces an impedance matching method that distinctly separates linear circuits from nonlinear circuits. The principal concept isolates the nonlinear circuit from the impedance matching process, connecting the two through the diode′s harmonic embedding impedance in the linear circuit as determined by nonlinear simulations. This approach significantly improves simulation speed. To validate the accuracy and practicality of this design concept, a 340 GHz balanced frequency doubler circuit was designed and fabricated.

1 Linear impedance matching method

The balanced frequency doubler consists of a pair of in-phase, parallel-connected diodes mounted on the E-plane of the input waveguide, with the output signal transmitted to the output waveguide by means of an E-plane probe. Its unique topological structure allows the currents generated by odd harmonics to circulate between the diodes and the ground provided by the cavity, effectively making the entire diode unit act like a dipole antenna that excites TE modes in the waveguide. Meanwhile, the currents from even harmonics can generate TEM modes along the direction of the transmission line. This configuration results in mode isolation between the input fundamental signal and the output second harmonic signal, as well as impedance isolation. Consequently, in-

put and output matching can be designed independently without concern for their coupling effects.

According to the principles, the design of a balanced frequency doubler circuit can be segmented into three parts: initially, individual harmonic balance simulations of the diodes are performed to determine their best operating harmonic embedding impedance; subsequently, the previously determined harmonic embedding impedance is utilized to design the input and output matching circuits separately; finally, the input and output matches are integrated into a complete circuit, and a comprehensive harmonic balance simulation is performed to predict the circuit's performance. The design process is illustrated in Fig. 1.

1.1 Extraction of diode harmonic embedding impedance

For frequency doublers based on Schottky diodes, the diode's parasitic and intrinsic parameters significantly impact the performance of the frequency doubler. To ensure the doubler operates optimally at 340 GHz, with the maximum output under a standardized 100 mW input, we optimized the intrinsic parameters of the diode based on measured data from a series of Schottky diodes with different diameters. The final intrinsic parameters of the diode are presented in Table 1.

Table 1 Intrinsic SPICE parameters of the diodes
表1 二极管的本征SPICE参数

Parameters	Value
Diameter, d	5 μm
Reverse saturation current, I_s	22.8 fA
Zero bias junction capacitance, C_{j0}	21.6 fF
Ideal factor, η	1.1
Series resistance at DC measurement, R_s	3.8 Ω
Reverse breakdown voltage, V_b	12 V
Barrier voltage, V_j	0.77 V
Grading coefficient, M	0.418

Subsequently, harmonic balance simulations are performed on the diode model to extract both the fundamental and second harmonic embedding impedances, as depicted in the HB simulation section of Fig. 1. Sampling of the optimal harmonic embedding impedances within the 155-185 GHz frequency range was carried out through harmonic balance simulations, targeting the desired output efficiency at these frequencies. This process ultimately yielded a series of embedding impedances, which represent the diode's optimal embedding impedances within this frequency band. Given the continuity of embedding impedances and their gradual variation with frequency, as illustrated on the Smith chart, larger steps can be taken between frequency points to reduce simulation time without compromising the accuracy of the results. The final normalized embedding impedances are shown in Fig. 2.

1.2 Input matching network

As mentioned in Section 2.1, the input fundamental signal operates in the TE_{10} mode, while the output second harmonic signal travels in the TEM mode. Their mode orthogonality ignores the need for an additional filter, reducing the complexity of the matching process. Moreover, the isolation between input and output impedances minimizes their mutual influence, allowing for the independent optimization of the input matching network.

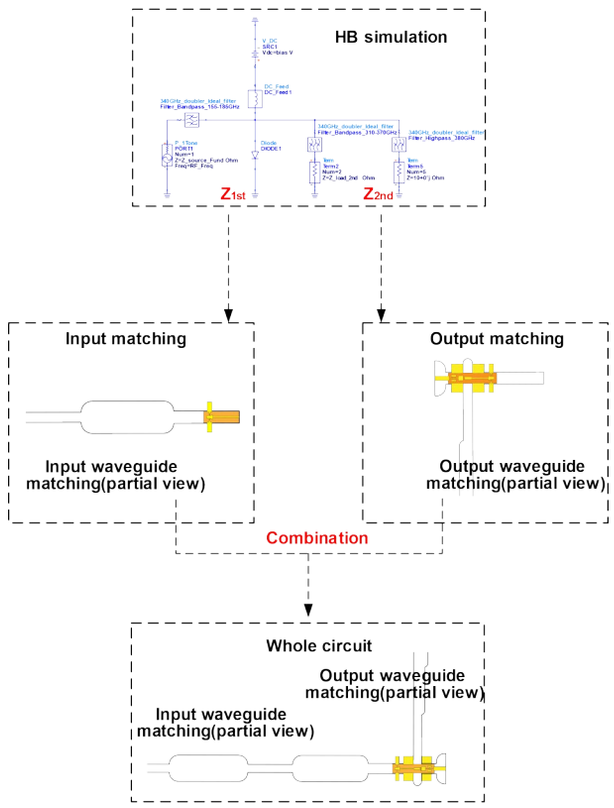


Fig. 1 Linear optimization method design flow diagram (HB: Harmonic Balance)
图1 线性优化法的设计流程图

As shown in Fig. 3, the initial step involves determining the parameters of the waveguide cavity where the diode cell is suspended. The width of the waveguide, a, is primarily determined by the input frequency, while the height of the waveguide, b, is influenced by the ease of impedance matching as well as the cutoff concerns of the TM_{11} mode at the output frequency. Other parameters that significantly affect the input impedance, such as the distance from the diode plane to the short-circuit plane of the input waveguide and the dimensions for the input matching waveguide, can be optimized in an *S*-parameter simulation after parameterization, as illustrated in the schematic in Fig. 4. Connecting the AC source to the diode's port optimizes their average impedance. It is crucial to note that the source impedance here is conjugate to the impedance extracted from the previous harmonic balance simulations. Incorrect setting of this impedance may lead to discrepancies from expected results.

Furthermore, the transmission structures in the output matching circuit might affect the field distribution of the TE_{10} mode, thereby influencing the transmission constants and characteristic impedance of the TE_{10} mode, as

shown in Fig. 5(b). To prevent the transmission line structure of the output circuit from affecting the input impedance, two methods can be used: the first is to determine the maximum line width that does not affect the TE_{10} mode through simulation; the second is to incorporate this transmission line into the input matching circuit after obtaining the output matching circuit, and then iterate to eliminate this effect.

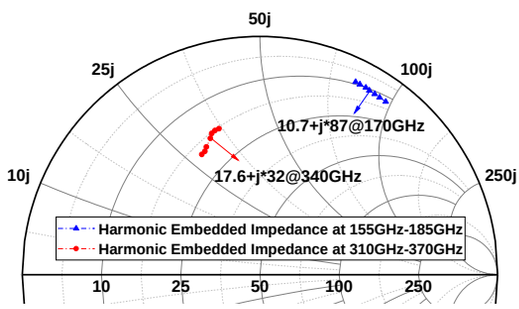


Fig. 2 Optimal input and output embedding impedances for the diode
图2 二极管的最佳输入输出嵌入阻抗

Ultimately, the dimensions of the various parts of the input matching circuit obtained through simulations are shown in Fig. 5(a). It is worth noting that the transmission line in Fig. 5(a) is primarily used for output circuit matching. However, considering the effect on the input mode TE_{10}, as shown in Fig. 5(b), this effect needs to be reflected in the input circuit to iterate the dimensions of the input matching waveguide, thereby eliminating the influence. Consequently, the dimensions are determined by the output matching circuit. Additionally, Fig. 5(c) illustrates the relationship between the impedance provided by the input matching network and the optimal input impedance of the diode. The blue line represents the impedance provided by the input matching network, while the red circle represents the optimal embedded impedance of the diode extracted through harmonic balance simulation.

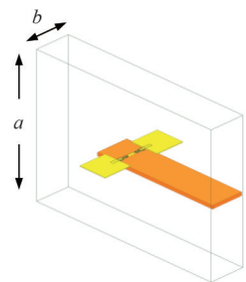


Fig. 3 Schematic of the waveguide cavity where the diode cell is suspended
图3 二极管单元悬置于波导腔体的示意图

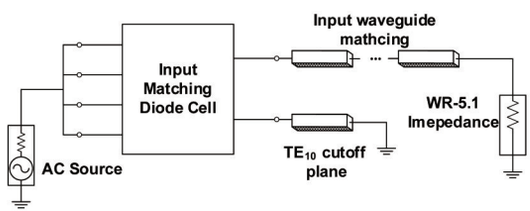
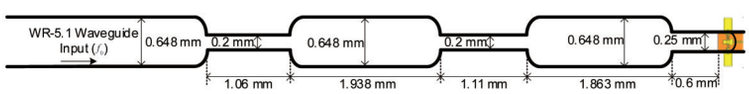


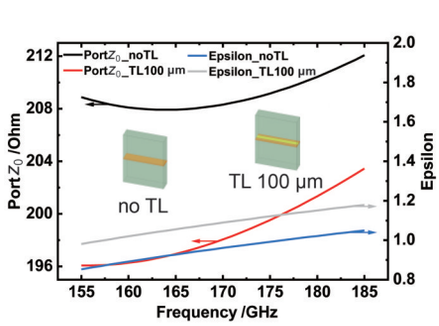
Fig. 4 Schematic for optimization of the input matching network circuit
图4 输入匹配电路优化的原理图

1.3 Output matching network

The output matching circuit can be divided and designed in two parts: one from the diode to the suspended microstrip line in the channel, and the other encompassing the output probe transition, which includes a DC filter. These two parts are connected by introducing a fixed



(a)



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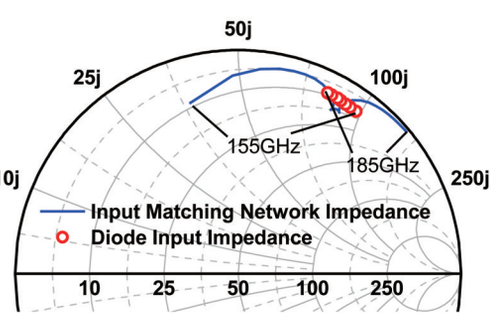

(c)

Fig. 5 Design of input matching network: (a) detailed dimensions of the input matching network; (b) comparison of PortZ_0 and Epsilon for suspended and non-suspended microstrip lines with a width of 100 μm for the TE_{10} mode; (c) comparison of the diode's input embedding impedance with the impedance provided by the input matching network
图5 输入匹配网络的设计:(a)输入匹配网络的具体尺寸;(b)线宽 100 μm 的悬置微带与非悬置微带在 TE_{10} 模下的 PortZ_0 和等效介电常数的比较;(c)二极管的输入嵌入阻抗与输入匹配网络提供的阻抗之间的比较

load impedance, Z_L, in the middle to simplify the complexity of output matching. The load impedance is determined by the suspended microstrip line in the channel. Thus, when combining the two circuit parts, merely adjusting the length of the suspended microstrip line can minimize reflections between the two subcircuits. The specific principle is illustrated in Fig. 6. The principle of the matching circuit for the first section, from the diode to the suspended microstrip line in the channel, is shown in Fig. 6. The second part of the matching circuit, including the output probe transition, DC filter, and the output waveguide matching section, is illustrated in Fig. 7(a). The connecting part between them is represented by Z_L.

Diverging from traditional high-low impedance filters, this design employs a CMRC (Compact Microstrip Resonant Cell) filter for the DC filtering section, aiming to minimize the overall length of the chip while ensuring robust RF suppression capabilities to ease assembly challenges. The resulting integrated output circuit's waveguide matching section is displayed in Fig. 7(a), with details of the monolithic integrated circuit shown in Fig. 7(b). Additionally, the relationship between the impedance achieved by the output matching network and the diode's output impedance is illustrated in Fig. 7(c).

2 Assembly and measurement

After separately designing the input and output matching circuits, combining these two sections forms the complete frequency doubler circuit, which includes the monolithic circuit and the metal cavity. An E-plane split-waveguide block is produced through computer numerical control (CNC) milling technology and is further processed by electroplating. The diode chip is mounted

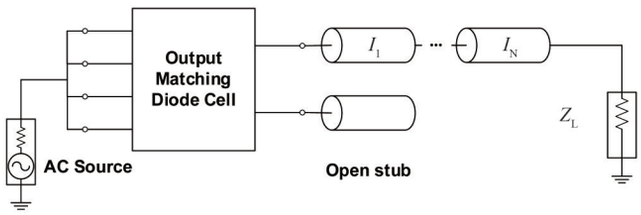

Fig. 6 Schematic for optimization of the output matching network circuit
图6 输入匹配电路优化的原理图

on the split block and aligned through beam leads to ensure its correct placement. This step is critical, as the accuracy of alignment directly influences performance. Subsequently, the DC beam leads are connected to the chip capacitors and through capacitors to establish the DC pathway for the frequency doubler. Lacking thermocompression bonding facilities, conductive adhesive is used to attach the beam leads to the cavity. However, this approach does not offer sufficient strength, making the chip prone to shifting during the disassembly of the cavity. This may also explain the significant discrepancies between our empirical results and the simulations. The fully assembled frequency doubler is illustrated in Fig. 8.

The constructed test system is shown in Fig. 9. The driver source chains includes a synthesizer, followed by an 81-86 GHz sextupler module, which is then connected to a 170 GHz doubler. The output signal is amplified by a GaN-based HEMT amplifier with a gain of about 10dbm, allowing the chains to provide an output power of approximately 72-150 mW in the 162-175 GHz band. Both the source power calibration and the output power measurement are performed by an Erickson PM4 power

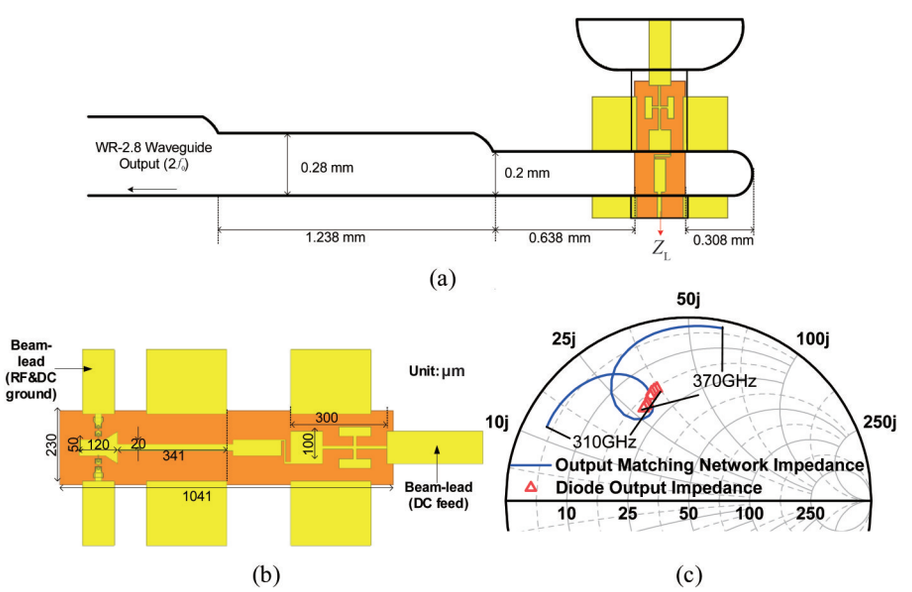

Fig. 7 Design of the output matching network: (a) detailed dimensions of the output waveguide matching; (b) the detail of the 340 GHz frequency doubler chip; (c) comparison of the diode's output embedding impedance with the impedance provided by the output matching network
图7 输出匹配电路的设计:(a)输入波导匹配的具体尺寸;(b)340 GHz二倍频芯片的具体细节;(c)二极管输出嵌入阻抗与输出匹配网络提供的阻抗之间的比较

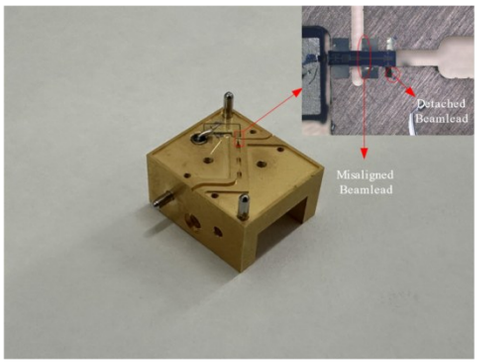

Fig. 8 Assembled frequency doubler
图8 装配好的二倍频器

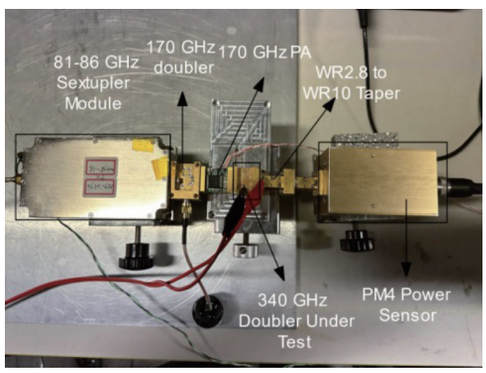

Fig. 9 Diagram of the frequency doubler test setup
图9 二倍频器测试系统原理图

meter. To achieve optimal performance of the doubler, we measured the output power and frequency characteristics of the frequency multiplier at a series of different bias points, and the final output curve represents the maximum output power recorded at each frequency point.

Figure 10(a) displays the actual input power versus the measured output power of the 340 GHz frequency doubler. Within the range of 330-342 GHz, the output power exceeds 13 mW, reaching a maximum output power of 21.8 mW at 334 GHz. Figure 10(b) shows a comparison between the measured efficiency and the simulated efficiency using different series resistances. It is known from Refs. [19, 37] that series resistance is crucial to circuit performance, and the resistance obtained from DC measurement is often underestimated for RF simulations. According to the comparison, we found that the simulation results using the adjusted series resistance align better with the test results. Moreover, the test results indicate a sharp decrease in output power above 344 GHz, while a slight increase in output efficiency is observed below 330 GHz.

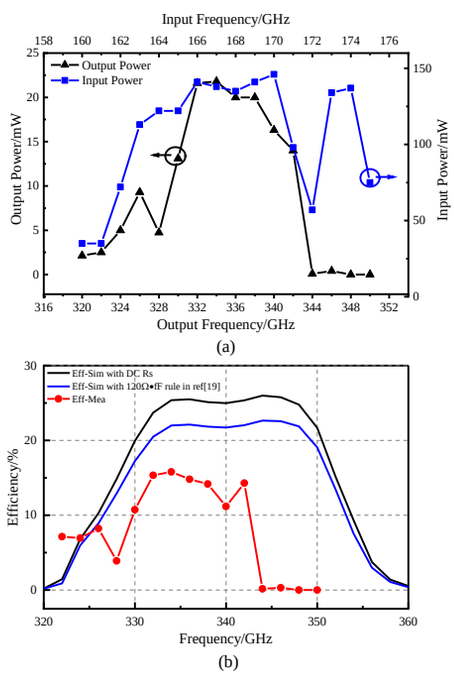

Fig. 10 Test results of the 340 GHz doubler: (a) measured input power and output power versus frequencies; (b) comparison of measured efficiency and simulated efficiency with different series resistances (simulated input power P_{in}=150 mW)
图10 340 GHz二倍频器的测试结果:(a)测量的输入功率和输出功率随频率的变化;(b)不同串联电阻下测量效率与仿真效率之间的比较(仿真输入功率P_{in}=150 mW)

As shown in Fig. 8, the supporting beam lead is not aligned with the output waveguide but is instead shifted

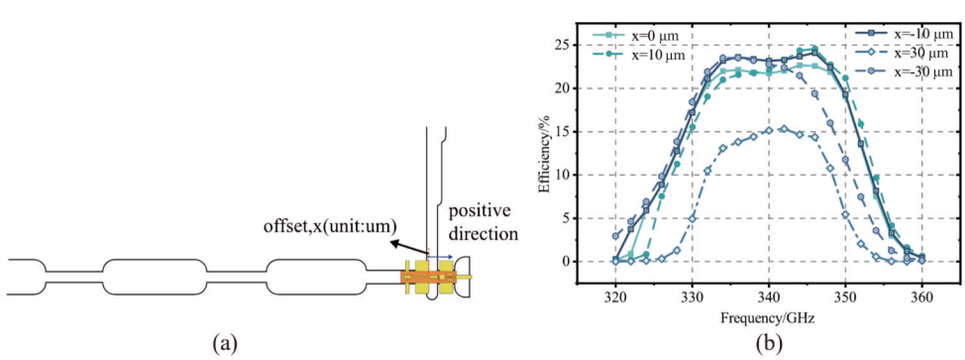

Fig. 11 The effect of assembly errors on output: (a) schematic of the lateral assembly error; (b) impact of different offset values on the output efficiency, with R_s•C_{j0} = 120 Ω•fF and P_{in}=150 mW
图11 装配误差对输出造成的影响:(a)横向装配误差示意图;(b)不同的偏移值对输出效率的影响,R_s•C_{j0} = 120 Ω•fF and P_{in}=150 mW

into the input waveguide, which may be the main cause of the sharp drop in output. Based on this issue, we conducted a simulation analysis of the impact of lateral assembly errors of the doubler chip on the performance of the frequency doubler, as shown in Fig. 11. It can be observed that when the lateral shift is around 10 μm, the output results do not change significantly. However, when the shift exceeds 10 μm, both the output efficiency and bandwidth of the doubler start to decline, especially in the case of forward shifting, where the beam lead moves toward the output waveguide. In this case, the decline in output efficiency and bandwidth becomes very noticeable, which aligns well with the situation shown in Fig. 8. Therefore, during the manufacturing process of the frequency doubler, it is crucial to control the assembly error tolerance within 10 μm as much as possible. Additionally, as shown in Fig. 12, there is a notch in the output waveguide of the machined lower half of the cavity, which could unpredictably affect the output.

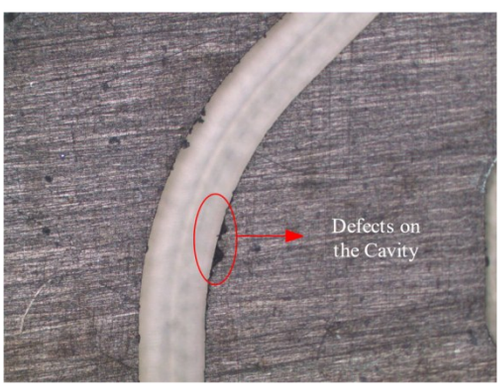

Fig. 12 Defects on the surface of the output waveguide
图12 输出波导表面的缺陷

Table 2 presents a comparison between the frequency doubler proposed in this paper and those designed using other methods. Unlike approaches that optimize linear and nonlinear circuits together, the method of separating linear and nonlinear circuits adopted in this work ensures both efficiency and flexibility while achieving commendable performance.

Table 2 Comparison with other doubler designs
表2 与其他倍频器设计的比较

Ref.	Output Frequency (GHz)	P_{in} (mW)	Peak P_{out} (mW)	Design Method
[38]	177-202	50-95	13	SDM
[31]	200-240	20-120	5	SDM
[39]	135-190	30-174	17.8	GDM
[35]	210-234	42-97	16	FHIMO
[36]	205-225	10-50	13	FMWW
[23]	135-150	10-70	3.5	Quality factors scaling
This work	322-342	35-146	21.8	LOM

3 Conclusions

In this paper, a strategy to boost the design efficiency of terahertz frequency multipliers is proposed. This method separates the circuit into linear and nonlinear parts for distinct simulations. By using the diode's nonlinear properties in the linear circuit's embedding impedance, it connects the two parts. This separation of harmonic balance from S-parameter simulations helps to reduce simulation time. Following this strategic framework, a 340 GHz frequency doubler was developed and subjected to empirical validation. Performance evaluations revealed that within a bandwidth of 330 GHz to 342 GHz, the efficiency of the device consistently surpasses 10%, with the input power oscillating between 98 mW and 141 mW, and the output power starting from 13 mW. Remarkably, with an input power set at 141 mW, the device achieved a peak output of 21.8 mW at 334 GHz, translating to an efficiency rate of 15.8%. The practical application of this frequency doubler effectively demonstrates the viability of the suggested approach. This technique promises adaptability for a wide range of applications in terahertz circuits, particularly for complex harmonic structures like mixers and compact modules.

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