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Semi-Floating Gate Ferroelectric Phototransistor Optoelectronic Integrated Devices

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Abstract: In the realm of optoelectronics, photodetectors play pivotal roles, with applications spanning from high-speed data communication to precise environmental sensing. Despite the advancements, conventional photodetectors grapple with challenges with response speed and dark current. In this study, we present a photodetector based on a lateral $MoTe_2$ p-n junction, defined by a semi-floating ferroelectric gate. The strong ferroelectric fields and the depletion region of the p-n junction in the device are notably compact, which diminish the carrier transit time, thereby enhancing the speed of the photoelectric response. The non-volatile $MoTe_2$ homojunction, under the influence of external gate voltage pulses, can alter the orientation of the intrinsic electric field within the junction. As a photovoltaic detector, it achieves an ultra-low dark current of 20 pA, and a fast photo response of 2 μs. The spectral response is extended to the shortwave infrared range at 1550 nm. Furthermore, a logic computing system with light/no light as binary input is designed to convert the current signal to the voltage output. This research not only underscores the versatility of 2D materials in the realm of sophisticated photodetector design but also heralds new avenues for their application in energy-efficient, high-performance optoelectronic devices.

Key words: Photodetectors, p-n junction, ferroelectric field, high-speed photodetector

半浮栅铁电光电晶体管光子集成器件

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摘要:在光电子领域中,光电探测器扮演了关键的角色,应用范围从高速数据通信到精确的环境感测。尽管取得进步,传统的光电探测器在响应速度和暗电流方面仍面临挑战。在本研究中,我们提出了一种基于面内$MoTe_2$ p-n结的光电探测器,该探测器由半浮铁电栅控制。强铁电场使得器件中的p-n结耗尽区较短,有助于减少载流子传输时间,从而提高光电响应速度。这种非易失性$MoTe_2$同质结在外部栅压的作用下,能够改变

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内建电场的方向。作为光伏探测器,它实现了20 pA的极低的暗电流和2μs快速的光响应时间。光谱响应扩展到1550 nm的短波红外范围。此外,还展示了设计了一个有光/无光作为二进制输入,将电流信号转化为电压输出的逻辑运算系统。这项研究不仅展示了二维材料在复杂光电探测器设计领域的多功能性,还为其在能效高、性能优的光电设备中的应用开辟了新途径。

关 键 词:光电探测器;p-n结;铁电场;高速光电探测器

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Introduction

In recent years, with the breakthrough of emerging technologies such as photonic integrated circuits, photodetectors, as a component of many optical and optoelectronic devices, have made great progress. [1-3] These technological advances have not only enhanced the performance of photodetectors but also expanded their application scope. They continually drive the development of photodetectors towards faster response speeds, lower dark currents, and broader spectral responses. Nevertheless, conventional photodetectors utilizing bulk substrates such as silicon[4], germanium[5], and III-V group semiconductors[6] encounter challenges in concurrently achieving a swift photonic response, minimizing dark current, and ensuring a broad spectral sensitivity. An emerging and viable alternative is found in the realm of two-dimensional (2D) materials. These materials are characterized by their robust interaction with light, adjustable energy bandgaps, and harmonization with current semiconductor manufacturing processes, alongside the considerable advantages presented by their atomically precise heterointerfaces[7-8]. For instance, 2D material-based photodetectors with ultra-high response speeds (up to 500 GHz) have been well-documented, achieving high-speed responses through the exceptionally high mobility of graphene[9]. However, these devices also exhibit milliampere-level dark currents. To reduce the dark current and enhance the response speed of these devices, researchers have employed p-n junctions[3,10]. However, due to material growth and the extended length of the depletion zone, there is potential for further improvement in the response speed of the devices[10-11].

In this work, we report a photodetector fabricated using multilayer $MoTe_2$ to form a p-n homojunction and photovoltaic mechanism. By adopting a poly(vinylidene fluoride-trifluoroethylene) (P(VDF-TrFE)) ferroelectric field and a semi-floating gate structure composed of graphene and hexagonal boron nitride, we successfully reduced the junction length, achieving ultra-low dark current and high-speed response. The unique properties of 2D materials allowed us to modulate doping of electrons or holes simply by applying an electrostatic field. The floating gate part, made of graphene and hexagonal boron nitride, effectively shielded the $MoTe_2$ channel from the polarization effects of P(VDF-TrFE), efficiently forming an in-plane p-n junction. Unlike traditional rigid ferroelectric materials like $LiNbO_3$ and $BiFeO_3$, organic ferroelectric copolymers such as P(VDF-TrFE) exhibit exceptional flexibility, transparency, retention, and durability, offering new possibilities for the widespread application of 2D material-based p-n junctions[12-14]. These materials can be easily prepared through low-temperature and simple processes like spin-coating, potentially reducing the cost and simplifying the manufacturing process for large-scale production of 2D material p-n junctions. Leveraging the depolarization field of P(VDF-TrFE)[15], we altered the bandgap of $MoTe_2$, achieving efficient photodetection at a wavelength of 1550 nm.

1 Results and Discussion

Fig. 1(a) presents a schematic of the proposed device structure. The layered composition, from bottom to top, consists of an aluminum (Al) gate electrode, a P(VDF-TrFE) dielectric layer, a partially covered graphene floating gate, and a h-BN tunneling layer. Such a configuration facilitates efficient charge storage and enables effective modulation of carrier concentration in the $MoTe_2$ channel. In this structure, $MoTe_2$ serves as the photosensitive channel layer, responsible for sensing optical signals. Analogous to the structure of MoS_2, $MoTe_2$ comprises Te-Mo-Te layers bonded by van der Waals forces[16]. $MoTe_2$ is a two-dimensional semiconductor with a bandgap ranging from 0.93 to 1.1 eV as its thickness decreases from bulk to a single layer[17]. The bipolar characteristics of $MoTe_2$ makes it easy to modulate to a p-type or n-type semiconductor by ferroelectric polarization. Other bipolar two-dimensional materials such as WSe_2 and BP were considered but they are vulnerable to ambient environment. It is noteworthy that the graphene and h-BN layers only cover half of the channel, indicating that the floating gate exerts control over only half of the channel region. This design feature allows for selective doping of the channel region through the ferroelectric polarization effect or gate voltage, thereby tuning its conductive properties.

In the device architecture, the P(VDF-TrFE) layer serves a dual purpose. Firstly, it provides a ferroelectric field which electrostatically dopes the $MoTe_2$, inducing selective doping due to the influence of the graphene and h-BN floating gate, resulting in the formation of a p-n junction. Secondly, the electric field generated by the P(VDF-TrFE) layer modifies the energy bandgap of the $MoTe_2$, thereby extending its spectral response. [15,18]The strategic placement and engineering of the P(VDF-TrFE) layer are critical to achieving the desired modulation of the device's electrical and optical properties. First, the two-dimensional materials were characterized by Raman spectroscopy, as shown in Fig. 1c. Individual $MoTe_2$ exhibited typical Raman peaks, indicating they are few-layer structures[19]. The precise thicknesses were

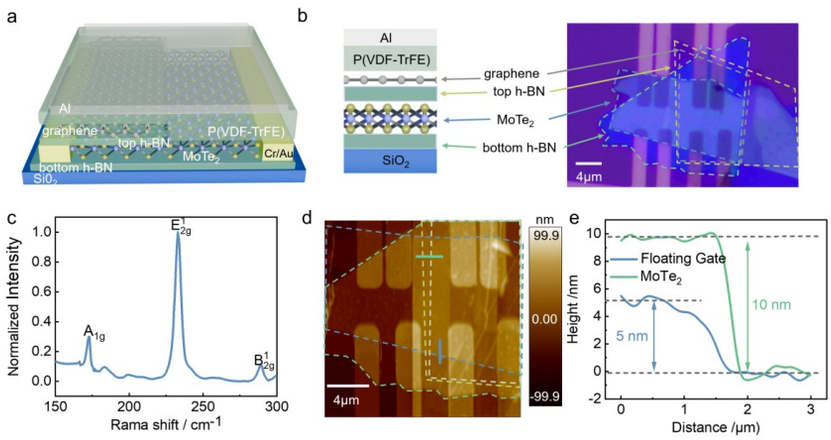

Fig. 1　Characterization and Device Structure of Two-Dimensional Material Detectors:(a) schematic illustration of the device structure; (b) optical image showing the top aluminum electrode used for polarizing the ferroelectric film; (c) Raman spectrum of $MoTe_2$, highlighting its characteristic peaks; (d) atomic force microscope image of the device, with the red and black lines indicating the locations where the height was measured; (e) characterization of the material's thickness

图1　二维材料探测器的表征与器件结构:(a)器件结构示意图;(b)用于使铁电薄膜极化的顶部铝电极的光学图像;(c) $MoTe_2$的拉曼光谱,突出其特征峰;(d)该装置的原子力显微镜图像,红色和黑色线条表示测量高度的位置;(e)材料厚度表征

further studied through Atomic Force Microscopy measurements, revealing that the thickness of molybdenum ditelluride is 10nm, and the thickness of the floating gate is 5 nm. To gain a deeper understanding of the regulatory effect of the P(VDF-TrFE) dielectric layer on the electrical properties of two-dimensional $MoTe_2$, this study systematically analyzed the transfer characteristic curves of the channel under different coverage conditions.

In the transfer characteristic curve depicted in Fig. 2(a), the device is characterized by a channel that is not encapsulated by graphene and boron nitride, employing solely P(VDF-TrFE) as the dielectric layer in the Ferroelectric Field-Effect Transistor (FeFET). Under a source-drain bias (V_{sd}) of ±0.1 V, the transfer characteristic curve distinctly exhibits the bipolar semiconductor properties of $MoTe_2$[20]. The counterclockwise hysteresis observed in the current reflects the ferroelectric nature of P(VDF-TrFE)[18]. Changes in the gate voltage alter the polarization direction of P(VDF-TrFE), and upon the removal of the gate bias, the residual polarization of P(VDF-TrFE) leads to the counterclockwise hysteresis in the current-voltage curves. In the experiments presented in Figs. 2b and 2c, we initially applied gate voltages of -20 V and +20 V to polarize P(VDF-TrFE). Subsequently, we tested the back-gate transfer characteristics of the floating gate ferroelectric field-effect transistors (FGFeFET) and FeFET under various polarization states (V_{sd} set at 0.5 V). In Fig. 2b, the minimum points of the back-gate transfer curves for channels under different control methods were -3.3 V and 8.6 V, respectively. In Fig. 2c, these points were -4.3 V and 0.5 V, respectively. The concentration and type of carriers were calculated using the following formula[21]: $n = q \times (V_g - V_{ng}) \times C_g$. Here, V_g represents the applied back-gate voltage, which was set to zero (V_g=0 V) in this experiment, and V_{ng} is the gate voltage corresponding to the lowest channel conductance. C_g indicates the capacitance of silicon dioxide (SiO_2), and q is the charge carried by an electron. The sign of n indicates whether the majority carriers are electrons or holes. The results show that under different polarization states of P(VDF-TrFE), channels not covered by graphene and hexagonal boron nitride exhibited different types of carriers compared to those that were covered.

The types of majority carriers in the $MoTe_2$ channels under different polarization states are shown in Fig. 2d. When the P(VDF-TrFE) is in the Pup state, the majority carriers in the FGFeFET are holes, with a concentration of 2.41×10^{17} cm^{-3}; in the FeFET field-effect transistor, the majority carriers are electrons, with a concentration of 5.78×10^{17} cm^{-3}. In the SFGFeFET, the depletion width of the p-n junction is 193 nm, with a barrier height of 0.74 eV. When the P(VDF-TrFE) is in the P_{down} state, the majority carriers in the FGFeFET are electrons, with a concentration of 6.06×10^{16} cm^{-3}; in the FeFET, the majority carriers are holes, with a concentration of 3.41×10^{17} cm^{-3}. In the SFGFeFET, the depletion width of the p-n junction is 167 nm, with a barrier height of 0.68 eV. The distinct carrier concentrations and types in the FeFET and FGFeFET are attributed to the change in graphene's Fermi level under the influence of the gate voltage and ferroelectric field, allowing carriers in the $MoTe_2$ channel to tunnel into the graphene. When the gate voltage is removed, the electric field generated by the graphene partially shields the effect of the P(VDF-TrFE) electric field. This results in different concentrations and types of majority carriers in the $MoTe_2$ channels covered and not covered by graphene, thus forming a p-n junction within the device.

Fig. 2 (e) presents the transfer characteristics curves of the SFGFeFET under $\pm V_{sd}$ conditions. A significant shift in the rectification direction of the device is observed when the gate voltage is switched from positive to negative. Additionally, the device exhibits a stable cur-

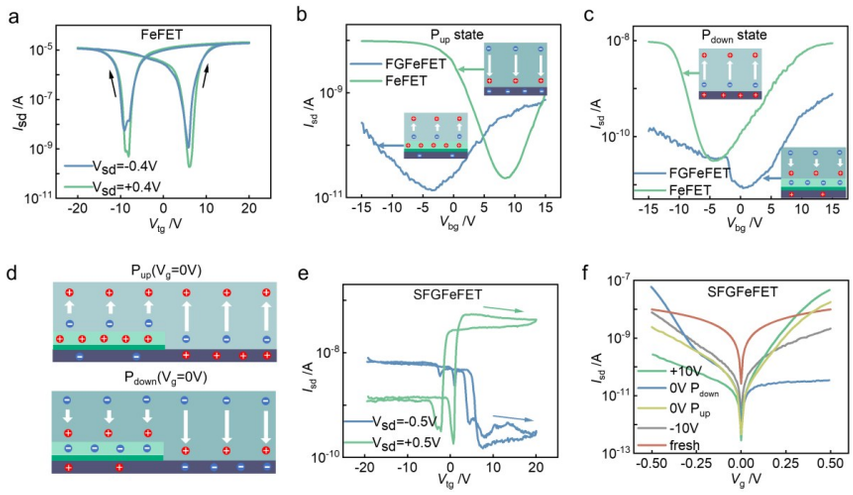

Fig. 2 Device Electrical Performance Characterization: (a) transfer characteristics curve of a FeFET with the channel solely covered by P(VDF-TrFE); (b) transfer characteristics of the FGFeFET and FeFET at the P_{up} state, with the inset depicting the type of charge carriers in the channel at a back-gate voltage (V_{bg}) of 0 V; (c) transfer characteristics of the FGFeFET and FeFET at the P_{down} state, with the inset indicating the type of charge carriers in the channel at a back-gate voltage (V_{bg}) of 0 V; (d) the types of most carriers in $MoTe_2$ channel under different polarization conditions; (e) transfer characteristics curve of a SFGFeFET with partial channel coverage by P(VDF-TrFE) and graphene/hexagonal boron nitride; (f) I_{SD}-V_{SD} curves of the SFGFeFET under various gate voltages

图2 器件电学性能表征：(a)通道完全被P(VDF-TrFE)覆盖的FeFET的转移特性曲线；(b) FGFeFET和FeFET在P_{up}状态下的转移特性，插入图描绘了在0 V的后门电压(V_{bg})下通道中的载流子类型；(c) P_{down}状态下FGFeFET和FeFET的转移特性，图中插入部分表示0 V电压下通道中电荷载流子的类型；(d)不同极化条件下$MoTe_2$通道中大多数载流子的类型；(e) P(VDF-TrFE)和石墨烯/六方氮化硼覆盖部分通道的SFGFeFET转移特性曲线；(f)不同栅极电压下SFGFeFET的I_{SD}-V_{SD}曲线

rent response within the gate voltage ranges of -10 V to -20 V and 10 V to 20 V, indicating that the P(VDF-TrFE) ferroelectric layer possesses excellent data retention characteristics, and the floating gate structure provides a stable electric field environment. We also measured the output characteristics (I_{sd} – V_{sd}) of the SFGFeFET under various states, as shown in Fig. 2(f). The output characteristics under different gate voltages exhibit similar rectifying behavior, with the magnitude and direction of rectification changing with the gate voltage. This shows that the direction of the built-in electric field of our device changes with the change of gate voltage. In conclusion, through the design of a P(VDF-TrFE) dielectric layer and a graphene/h-BN semi-floating gate, we can effectively modulate the $MoTe_2$ channel, achieving precise control of in-plane structures. This finding provides new strategies and theoretical foundations for the design and optimization of electronic devices based on two-dimensional materials

To verify the existence of the junction region within our device, we conducted photovoltaic current mapping at zero source-drain bias (V_{sd}=0 V). The scanning photocurrent measurement principle diagram of SFGFeFET device is shown in Fig. 3(a). The scan results are shown in Fig. 3(b). Notably, a significant positive photocurrent is discernible at the boundaries of graphene, indicative of a depletion zone at these interfaces. The inherent electric field present facilitates the separation of photogenerated carriers, resulting in the generation of a spontaneous photocurrent. This effect is also observed near the right electrode, where the photocurrent emerges spontaneously and aligns with the electric field direction of the junction region. This phenomenon is attributed to a Schottky junction formed between the metal electrode and the molybdenum telluride, generating a current that must coincide with the direction of the p-n junction to yield spontaneous photocurrent. Furthermore, the optoelectronic performances were measured and depicted in Fig. 3(c). The device exhibited robust responses across different light intensities. Additionally, we scrutinized the pure photocurrent response at 1 550 nm, as shown in Fig. 3(d). Given that 1 550 nm does not fall within the intrinsic response spectrum of $MoTe_2$, these observations suggest that our device has successfully extended the responsive spectral range of molybdenum telluride. This extension is attributable to the Stark effect, where the depolarization field of of the P(VDF-TrFE) alters the bandgap of molybdenum telluride,[30] consequently broadening its spectral bandwidth[31]. The Stark effect engenders a shift in the energy levels of the electronic states, thus enabling the absorption of photons with lower energies than the original bandgap, which is a remarkable demonstration of the tunable optoelectronic properties of our device. In Fig. 3(e), the photogenerated current signals exhibited rise and fall times of 2 μs each, with the limiting factor being attributed to our test equipment. However, with a device capacitance of only 1.79×10^{-5} pF, the equivalent RC circuit response time is approximately 27 ps. Given a junction length of about 167 nm and an electric field strength of 4×10^4 V·cm^{-1}, the carrier transit time is calculated to be around 3.7 ps. Consequently, this suggests a dynamic response bandwidth of approximately 5.8 GHz.

As revealed in Fig. 3(f), both the short-circuit current (I_{sc}) and open-circuit voltage (V_{oc}) exhibited an increasing trend with the enhancement of 520 nanometer

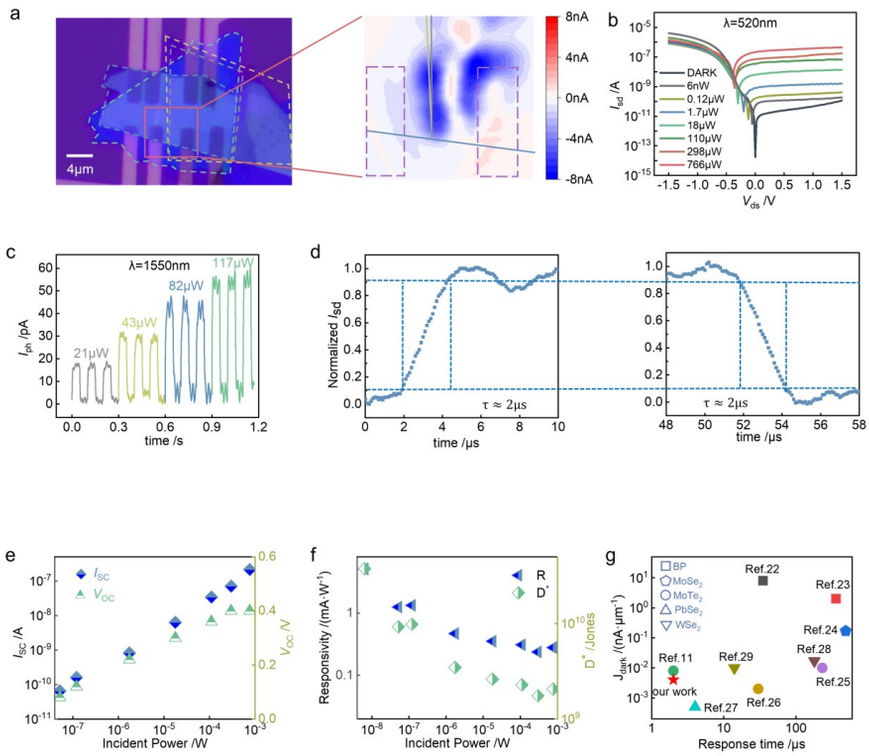

Fig. 3　Photocurrent measurement and response characteristics of the device: (a) schematic diagram of scanning photocurrent measurement of a SFGFeFET device; (b) photocurrent mapping at V_{DS}=0 V. Scale bar is 2 μm; (c) I_{SD}-V_{SD} curves of the $MoTe_2$ p－n junction under different laser powers at a wavelength of 520 nm; (d) response curves under different light powers at V_{DS}=0.2 V and λ=1 550 nm; (e) rise and decay times of photocurrent from 10% to 90% under λ=520 nm illumination; (f) power dependency of the short-circuit current and open-circuit voltage under λ=520 nm illumination; (g) power dependency of the photoresponsivity and detectivity under λ=520 nm illumination; (h) compare the response time and dark current density of photodetectors made of in-plane homojunction made of different materials. Different shapes in the figure mean different materials. References: BP[22-23]; $MoSe_2$[24]; $MoTe_2$[11,25-26]; $PbSe_2$[27]; WSe_2[28-29]

图3　器件的光电流测量与响应特性：(a) SFGFeFET 器件扫描光电流测量示意图；(b) V_{DS}=0 V时的光电流图。标尺为2 μm；(c) 520 nm波长下不同激光功率下 $MoTe_2$ p-n结的 I_{SD}-V_{SD} 曲线；(d) V_{DS}=0.2 V、λ=1 550 nm时不同光功率下的响应曲线；(e)在λ=520 nm照明下，光电流的上升和衰减时间从10%到90%；(f) λ=520 nm光照下短路电流和开路电压的功率依赖性；(g) λ=520 nm照明下的光响应性和探测性的功率依赖性；(h)比较不同材料平面内均结光电探测器的响应时间和暗电流密度。图中不同的形状代表不同的材料。引用: BP[22,23]; $MoSe_2$[24]; $MoTe_2$[11,25,26]; $PbSe_2$[27]; WSe_2[28,29]

light illumination power. When the device reached saturation, the V_{oc} attained a maximum of 0.4 V, and the saturation current was measured at 71 nA. Fig. 3(g) details the power dependency of the photoresponsivity (R) and detectivity (D^*) under zero bias (V_{sd}=0 V). The photoresponsivity is calculated using the formula $R = I_{ph}/p$, where I_{ph} represents the photogenerated current and p denotes the power of illumination. Due to the depletion of carriers in the space charge region of the photodiode, thermal noise and generation-recombination (G-R) noise are negligible[32]. The intrinsic noise is primarily contributed by shot noise in the junction current. Thus, the detectivity (D^*) of our photovoltaic detector is calculated using the formula $D^* = A^{1/2}R(2qI_{dark})^{-1/2}$, [33] where A is the effective area of the photodetector (20×10^{-8} cm^2), q is the elementary charge, and I_{dark} is the dark current (0.1 pA). At an illumination of 520 nm with a light power of 2.1 nW, the photodetector demonstrated a maximum photoresponsivity of 5 mA·W^{-1} and a detectivity of 3.7×10^{10} Jones. To evaluate the performance of our SFGFeFET photodetector, Fig. 3(h) compares planar homojunction photodetectors made of different two-dimensional materials in terms of response time and dark current density. The ultra-low dark current density in our device may be attributed to the passivation of surface defects by P(VDF-TrFE) and boron nitride at the bottom, which suppresses the generation-recombination current, thereby reducing the dark current. The faster response speed of our device may be due to the short depletion region of the p-n junction due to the strong iron electric field in the device, which helps to reduce the carrier transfer time and thus improve the photoelectric response speed. The response speed, responsivity, and detectivity of the device can be further enhanced by selecting electrode materials that reduce contact resistance, or by extending the thickness $MoTe_2$ to increase light-matter interaction.

Fig. 4(a), we present the current characteristics of our device under various gate voltages (V_g) and source-drain biases (V_{sd}), at a wavelength of 1 270 nm and under an illumination of 560 mW, contrasted with its dark

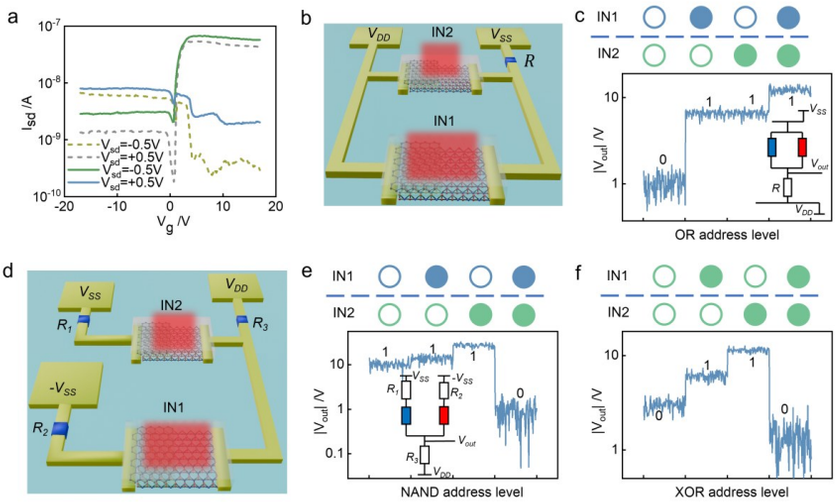

Fig. 4 Current Characteristics and Logic Gate Functionality of the Device: (a) The wavelength of incident light is 1 270 nm, the intensity of incident light is 560 μW, and the current characteristics of different gate and source drain voltages are compared with the dark state. The dashed line is the dark current and the realization is the photocurrent; (b) Circuit diagram of the OR gate; (c) Logic "OR" gate the output voltage of the four input states. Insert: Equivalent circuit diagram; (d) Circuit diagrams for NAND and XOR gates; (e) Logic "NAND" gate the output voltage of the four input states. Insert: Equivalent circuit diagram; (f) Logic "XOR" gate the output voltage of the four input states

图4 器件的电流特性与逻辑门功能:(a)入射光波长为1 270 nm,入射光强度为560 μW,在暗态下比较不同栅极和源极漏极电压的电流特性。虚线为暗电流,实现为光电流;(b)或门电路图;(c)逻辑“或”门四个输入状态的输出电压。插入:等效电路图;(d)NAND和XOR门的电路图;(e)逻辑“NAND”门控四个输入状态的输出电压。插图:等效电路图;(f)逻辑“异或”门的输出电压的四个输入状态

state. The measurements reveal distinctive behavioral characteristics of the photocurrent and dark current in response to changes in V_g and V_{sd}, laying the experimental groundwork for the device's potential application in logical computation. In the configuration shown in Fig. 4 (b), we utilized two structurally identical devices and selected an appropriate resistor R, based on the V_{SS} magnitude, to maintain operation at a source-drain bias of -0. 5 V and a gate voltage of 8 V. With V_{SS} set at 5 V and V_{DD} at 0 V, the ideal resistance was determined to be 1 GΩ, correlating with the current levels derived from the transfer characteristics. We have defined the illuminated state (filled circles) as a logical '1' and the dark state (unfilled circles) as a logical '0', thus creating a binary input system based on the presence or absence of light. The equivalent circuit diagram and the computational results, as demonstrated in Fig. 4(c), indicate that the currents from both devices merge through a common resistor R, converting the current signal into a voltage output, culminating in a singular output signal. The results depicted in Fig. 4(c) confirm that if either device is illuminated, the output signal reaches a high level, effectively implementing an 'OR' logic operation.

Fig. 4(d) illustrates the circuitry devised to perform 'NAND' and 'XOR' logical operations. By connecting the source electrodes of the devices to positive and negative voltage sources, V_{DD} and $-V_{DD}$, respectively, and assuming a total bus voltage of 10 V, we can set V_{DD} to 10 V and $-V_{DD}$ to 0 V, with V_{SS} at 5 V to achieve the desired bias. Appropriate resistor values ensure that both devices operate at source-drain voltages V_{SD} of +0. 5V with a gate voltage V_g of -10 V, and V_{sd} of -0. 5 V with V_g of +7 V, respectively. The equivalent circuit diagram and outcomes of these operations are presented in Fig. 4 (e), where the devices under varying light input conditions yield distinct voltage outputs, thus realizing 'NAND' logic gate operations. By employing the same circuit design and setting the gate voltages of the two devices to -8 V and 5 V, we can switch the logic operation mode to an 'XOR' gate, as depicted in Fig. 4(f). The flexibility of this design supports various logic computations, underscoring the potential of our device architecture for applications in photonic integrated circuits where light serves as the control parameter for executing logic tasks. The distinct voltage output levels under different light input conditions clearly delineate logical states, affirming the design's accuracy in performing complex logical operations.

2 Conclusion

The $MoTe_2$ p-n junction controlled by semi-floating ferroelectric gate is achieved. The diode exhibits robust rectification characteristics with a rectification ratio exceeding 10^4. As a photodetector, our device demonstrates a high photoresponsivity of 5 mA·W^{-1}, a rapid response time of 2 μs, an open-circuit voltage of 0. 4 eV, and a high specific detectivity of 3. 7 × 10^{10} Jones for visible light (520 nm), all achieved without bias or gate voltage, implying low power consumption. Notably, at room temperature, the response spectrum extends to the short-wave infrared (SWIR) range (1 550 nm), thereby addressing the limitations of traditional Si-based and infra-

red photodetectors. Building upon our device architecture, we constructed a binary input system based on the presence or absence of illumination. These devices operate under specific voltage conditions, converting the current signals passing through them into voltage outputs to perform basic logic operations. Such a photonic-controlled logic computation system demonstrates significant potential in optoelectronic integrated circuit design. In this system, light signals are utilized not only for sensing information but also for directly participating in the logical decision-making process. The distinct voltage output levels under different light input states clearly delineate the logic states, affirming the high accuracy and reliability of this design in executing complex logic operations.

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