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An improved method for determination of extrinsic resistances for HEMT devices based on 110 GHz S-parameters on-wafer measurement

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Abstract: An improved method for determination of extrinsic resistances for 70 nm InP high electron mobility transistor (HEMT) is proposed in this paper. A set of expressions have been derived from the equivalent circuit model under operating bias points ($V_{gs} > V_{th}$, $V_{ds} = 0$ V). The extrinsic resistances are iterative determined using the discrepancy between simulated and measured *S*-parameters as an optimization criterion using the semi-analytical method. Good agreement between simulated and measured *S*-parameters under multi bias over the frequency range up to 110 GHz verifies the effectiveness of this extraction method.

Key words: InP high electron mobility transistor (HEMT), equivalent circuit model, extrinsic resistances, modeling

一种改进的基于110GHz在片S参数测试的HEMT器件寄生电阻提取方法

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摘要:提出了一种改进的高电子迁移率晶体管寄生电阻提取方法,该方法利用了特殊偏置点($V_{gs}>V_{th}$, V_{ds}=0V)的等效电路模型,推导了寄生电阻的表达式,采用半分析法对寄生电阻进行了优化。1~110 GHz *S*参数实测结果和仿真的*S*参数一致,证明该方法是有效的。

关 键 词:InP高电子迁移率晶体管;等效电路模型;寄生电阻;器件建模

中图分类号:TN215 **文献标识码**:A

Introduction

Accurate extrinsic resistances extraction for modeling InP HEMT devices is a crucial step in the design and production of high-yield, low-cost millimeter wave circuits [1]. The common used methods mainly include numerical optimization method, cold FET method and cutoff method. In optimization method, the extrinsic resistances extraction result strongly depends on the initial value and suffers from non-uniqueness and non-physical meaning [2]. In cold FET method, the large gate currents caused by forward-biased run through the gate Schottky junction, which leads to degradation of the gate [3-6]. To avoid degradation of device characteristics, some authors proposed cutoff method to extract extrinsic resistances. However, this method is valid only at high frequency (> 18 GHz), and the extracted resistances fluctuate widely over the whole frequency range of interest [7-9].

In order to overcome these limitations, an improved method for determination of extrinsic resistances is proposed. In contrast with previous publications, this extraction method offers the following advantages.

1) Under operating bias point ($V_{gs} > V_{th}$, $V_{ds} = 0$V), the effect of channel between source and drain can be modeled by resistance R_{ch}, while the capacitance will be dominant under cutoff bias condition.

2) The semi-analytical method which is a combination of optimization method and analytical direct extrac-

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tion method has been used to determine the extrinsic resistances.

3) This extraction method is verified with *S*-parameters on-wafer measurement up to 110 GHz.

Section Ⅱ gives the equivalent circuit model under operating bias point ($V_{gs} > V_{th}$, $V_{ds} = 0$V) as well as the derivation of analytical expressions. Section Ⅲ gives the procedure of intrinsic parameters extraction. The measured and simulated results are presented in Section Ⅳ. The conclusion is given in Section Ⅴ.

1 Extrinsic resistances extraction

1.1 Equivalent circuit model

Fig. 1 shows the small-signal equivalent circuit model under operating bias point ($V_{gs} > V_{th}$, $V_{ds} = 0$ V). C_{pgd}, C_{pg}, and C_{pd} represent the extrinsic capacitances due to the pad connections. L_g, L_d, and L_s represent the extrinsic inductances of the gate, drain, and source feedlines. R_s and R_d represent the extrinsic resistances of the source and drain. R_g is the distributed gate resistance. C_{gsa} and C_{gda} represent intrinsic gain-source and gain-drain capacitances respectively. R_{ch} is the channel resistance when the channel between drain and source is open at zero drain bias and gate voltage above threshold voltage.

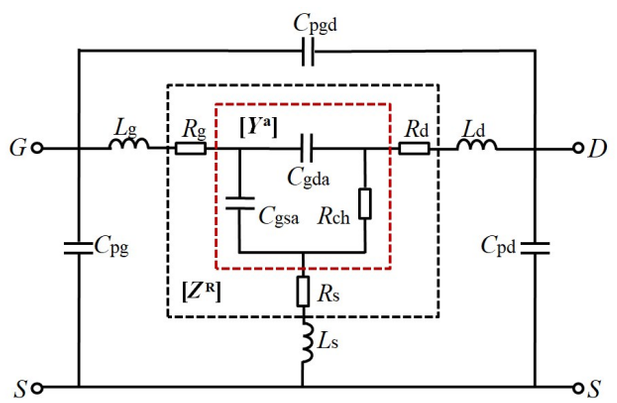


Fig. 1 The small-signal equivalent circuit model under operating bias point ($V_{gs} > V_{th}$, $V_{ds} = 0$ V)

图 1 偏置点（Vgs > Vth, Vds = 0 V）下的小信号等效电路模型

The intrinsic part of the equivalent circuit model, which exhibits a PI topology, so it is convenient to describe it by a *Y* matrix as

$$[Y^a] = \begin{bmatrix} Y_{11}^a & Y_{12}^a \\ Y_{21}^a & Y_{22}^a \end{bmatrix} = \begin{bmatrix} j\omega C_{gsa} + j\omega C_{gda} & -j\omega C_{gda} \\ -j\omega C_{gda} & j\omega C_{gda} + \dfrac{1}{R_{ch}} \end{bmatrix}, \quad (1)$$

Convert Y^a-parameters to Z^a −parameters:

$$Z_{11}^a = \frac{Y_{22}^a}{Y_{11}^a Y_{22}^a - Y_{12}^a Y_{21}^a} = \frac{1 + j\omega C_{gda} R_{ch}}{j\omega(C_{gsa} + C_{gda}) - \omega^2 C_{gsa} C_{gda} R_{ch}}, \quad (2)$$

$$Z_{12}^a = \frac{-Y_{12}^a}{Y_{11}^a Y_{22}^a - Y_{12}^a Y_{21}^a} = \frac{j\omega C_{gda} R_{ch}}{j\omega(C_{gsa} + C_{gda}) - \omega^2 C_{gsa} C_{gda} R_{ch}}, \quad (3)$$

$$Z_{21}^a = \frac{-Y_{21}^a}{Y_{11}^a Y_{22}^a - Y_{12}^a Y_{21}^a} = \frac{j\omega C_{gda} R_{ch}}{j\omega(C_{gsa} + C_{gda}) - \omega^2 C_{gsa} C_{gda} R_{ch}}, \quad (4)$$

$$Z_{22}^a = \frac{Y_{11}^a}{Y_{11}^a Y_{22}^a - Y_{12}^a Y_{21}^a} = \frac{j\omega R_{ch}(C_{gda} + C_{gsa})}{j\omega(C_{gsa} + C_{gda}) - \omega^2 C_{gsa} C_{gda} R_{ch}}, \quad (5)$$

The *Z*-parameters of intrinsic part with extrinsic resistances can be expressed as following:

$$Z_{11}^R = R_g + R_s + Z_{11}^a, \quad (6)$$

$$Z_{12}^R = R_s + Z_{12}^a, \quad (7)$$

$$Z_{21}^R = R_s + Z_{21}^a, \quad (8)$$

$$Z_{22}^R = R_d + R_s + Z_{11}^a, \quad (9)$$

Therefore, we have

$$\mathrm{Re}(Z_{11}^R - Z_{12}^R) = R_g - \frac{\omega^2 C_{gsa} C_{gda} R_{ch}}{\omega^4 C_{gsa}^2 C_{gda}^2 R_{ch}^2 + \omega^2 (C_{gsa} + C_{gda})^2}, \quad (10)$$

$$\mathrm{Re}(Z_{12}^R) = R_s + \frac{\omega^2 C_{gda} R_{ch}(C_{gsa} + C_{gda})}{\omega^4 C_{gsa}^2 C_{gda}^2 R_{ch}^2 + \omega^2 (C_{gsa} + C_{gda})^2}, \quad (11)$$

$$\mathrm{Re}(Z_{22}^R - Z_{12}^R) = R_d + \frac{\omega^2 C_{gsa} R_{ch}(C_{gsa} + C_{gda})}{\omega^4 C_{gsa}^2 C_{gda}^2 R_{ch}^2 + \omega^2 (C_{gsa} + C_{gda})^2}, \quad (12)$$

By neglecting the high order term $\omega^4 C_{gsa}^2 C_{gda}^2 R_{ch}^2$, the extrinsic resistances can be obtained by analytical expressions from real part of Z^R-parameters:

$$R_g = \mathrm{Re}(Z_{11}^R - Z_{12}^R) - \alpha R_{ch}, \quad (13)$$

$$R_d = \mathrm{Re}(Z_{22}^R - Z_{12}^R) - (1 - \beta) R_{ch}, \quad (14)$$

$$R_s = \mathrm{Re}(Z_{12}^R) - \beta R_{ch}, \quad (15)$$

Where

$$\alpha = -\frac{C_{gs} C_{gd}}{(C_{gs} + C_{gd})^2}, \quad (16)$$

$$\beta = -\frac{C_{gd}}{C_{gs} + C_{gd}}, \quad (17)$$

C_{gsa} and C_{gda} can be determined at low frequencies:

$$C_{gsa} = \left.\frac{\mathrm{Im}(Y_{11}^a + Y_{12}^a)}{\omega}\right|_{\omega \to 0}, \quad (18)$$

$$C_{gda} = \left.-\frac{\mathrm{Im}(Y_{12}^a)}{\omega}\right|_{\omega \to 0}, \quad (19)$$

1.2 Extrinsic parameters extraction

The pad capacitances can be determined by measuring an open test structure:

$$C_{pg} = \frac{1}{\omega}\mathrm{Im}(Y_{11} + Y_{12}), \quad (20)$$

$$C_{pd} = \frac{1}{\omega}\mathrm{Im}(Y_{22} + Y_{12}), \quad (21)$$

$$C_{pgd} = -\frac{1}{\omega}\mathrm{Im}(Y_{12}) = -\frac{1}{\omega}\mathrm{Im}(Y_{21}), \quad (22)$$

The extrinsic inductances L_g, L_d, and L_s can be determined from the imaginary part of *Z*-parameters (trans-

formed from measured *S*-parameters) of the short test structure directly:

$$L_g = \frac{1}{\omega}\mathrm{Im}(Z_{11} - Z_{12}), \tag{23}$$

$$L_d = \frac{1}{\omega}\mathrm{Im}(Z_{22} - Z_{21}), \tag{24}$$

$$L_s = \frac{1}{\omega}\mathrm{Im}(Z_{12}) = \frac{1}{\omega}\mathrm{Im}(Z_{21}), \tag{25}$$

The extraction of extrinsic resistances can be based on the semi-analytical method which is a combination of optimization method and analytical direct extraction method. Fig. 2 shows the flow of the algorithm. The extraction procedure is as follows.

1) De-embedding the pad capacitances and feedline inductances.

2) Set the initial value of the channel resistance R_{ch}.

3) Calculate the extrinsic resistances R_g, R_d, and R_s using (13)-(15) which can be expressed as functions of R_{ch} as well as frequency.

4) Set error criteria as follows:

$$\varepsilon(R_{ch}) = \sum_{p=1}^{2}\sum_{q=1}^{2}\sum_{i=1}^{N} W_{pq}\left| S_{pq}^{c}(\omega_i, R_{ch}) - S_{pq}^{m}(\omega_i)\right|^2, \tag{26}$$

5) If error criteria are small enough, the iterative process will be end.

Where $S_{pq}^{c}(\omega_i, R_{ch})$ represents the calculated *S*-parameters, and $S_{pq}^{m}(\omega_i)$ represents the measured *S*-parameters. $\varepsilon(R_{ch})$ represents the discrepancy between simulated and measured *S*-parameters. W_{pq} are the weighting factors.

2 Intrinsic parameters extraction

The small-signal circuit model of intrinsic part of InP HEMT devices is illustrated in Fig. 3 after de-embedding the extrinsic parameters, and the intrinsic *Y*-parameters are described as [3]:

$$Y_{11}^{int} = \frac{R_i C_{gs}^2 \omega^2}{D} + j\omega\left(\frac{C_{gs}}{D} + C_{gd}\right), \tag{27}$$

$$Y_{12}^{int} = -j\omega C_{gd}, \tag{28}$$

$$Y_{21}^{int} = \frac{g_m \exp(-j\omega\tau)}{1 + j\omega R_i C_{gs}} - j\omega C_{gd}, \tag{29}$$

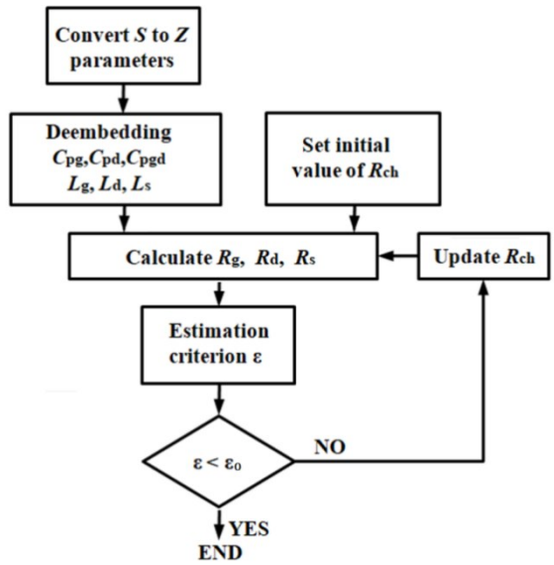


Fig. 2 Flowchart of the algorithm
图 2 算法流程图

$$Y_{22}^{int} = g_{ds} + j\omega(C_{gd} + C_{gs}), \tag{30}$$

With $D = 1 + R_i^2 C_{gs}^2 \omega^2$

From the analytical expressions (27)-(30), the intrinsic element values can be obtained directly.

3 Results and discussion

In this paper, 70 nm InP HEMT devices have been used with 2 × 30μm gate width (number of gate fingers×unit gate width). The *S*-paremeters on-wafer measurement up to 110 GHz using N5247 network analyzer with DC bias by an Agilent B1500A.

Fig. 4 shows the plot of extracted extrinsic resistances versus frequency using the presented semi-analytical method and cutoff method[9]. As can be seen from Fig. 4, the extracted R_d and R_s using semi-analytical method are nearly constant versus frequency, while extracted R_d and R_s using cutoff method fluctuate widely versus frequency. These results verify that the proposed extraction method is better than cutoff method [10].

Table 1 gives the values of extrinsic resistances extracted using semi-analytical method. The values of extrinsic capacitances and inductances are given in Table

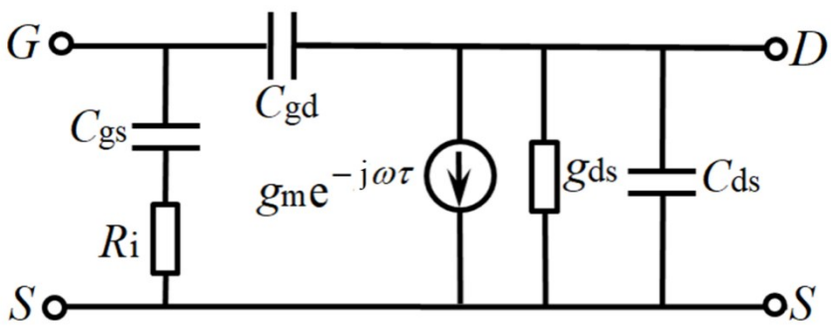
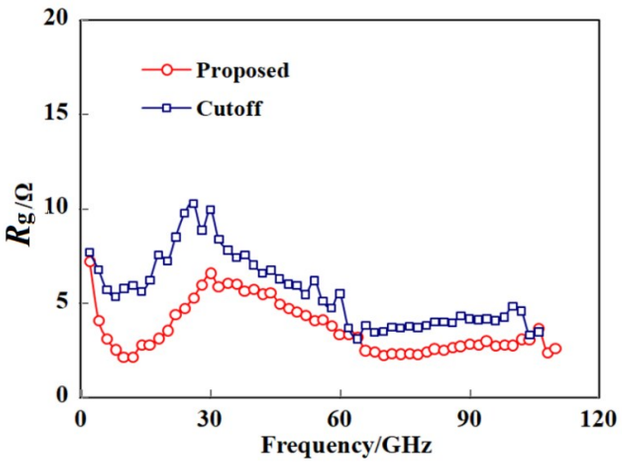
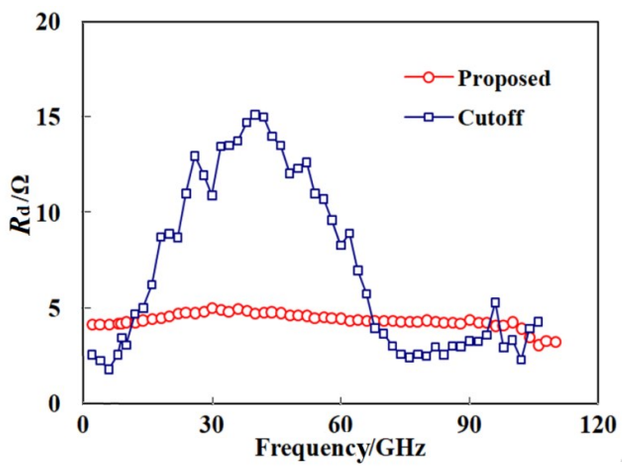


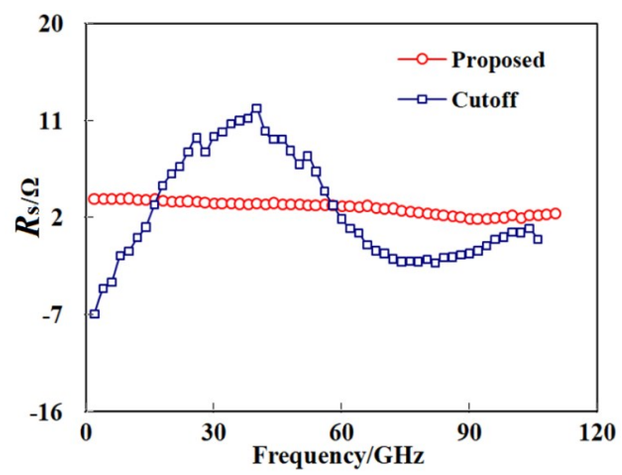
Fig. 3 The small-signal circuit model of intrinsic part
图 3 本征部分的小信号等效电路模型



(a)



(b)



(c)

Fig. 4 Extracted extrinsic resistances using the proposed semi-analytical method and cutoff method
图 4 半分析方法和截止方法提取的寄生电阻数值对比

2. The extracted intrinsic parameters in Section III are shown in Table 3.

Table 1 The values of extrinsic resistances
表1 寄生电阻数值

Element	Value
R_g/Ω	2.66
R_d/Ω	4.18
R_s/Ω	3.80

Table 2 The values of extrinsic capacitance and inductance
表 2 寄生电容和寄生电感数值

Capacitance	Value	Inductance	Value
C_{pg}/fF	13.26	L_g/pH	22.7
C_{pd}/fF	13.19	L_d/pH	28.5
C_{pgd}/fF	0.416	L_s/pH	3.25

Table 3 The values of intrinsic parameters
表3 本征元件数值

Element	Value	Element	Value
C_{gs}/fF	46.97	g_m/mS	82.2
C_{gd}/fF	9.69	g_{ds}mS	5.20
C_{ds}/fF	15.78	R_i/Ω	3.46

The intrinsic elements listed in Table 2 are substituted into the equivalent circuit model for simulation. Fig. 5 shows the comparison between simulated and measured *S*-parameters under multi bias. Good agreement between simulated and measured *S*-parameters are observed in the frequency range of 1 GHz to 110 GHz, which verifies the validity of this developed method to determine the extrinsic resistances.

Table 4 outlines a selection of the accuracy of *S*-parameters for four different bias points. As can been seen from this table, S_{11} and S_{21} maintain an accuracy of around 5%, S_{12} has an accuracy of less than 5%, and S_{22} has an accuracy of between 2%~5%.

4 Conclusion

An approach for determination of extrinsic resistances for 70 nm InP HEMT devices is proposed in this paper. Extrinsic resistances are described as functions of the intrinsic channel resistance, and optimum values can be obtained using semi-analytical method under operating bias point($V_{gs} > V_{th}$, $V_{ds} = 0$V). Verification of this extraction method is presented by the good agreement between the simulated and measured *S*-parameters under multi bias over the frequency range up to 110 GHz.

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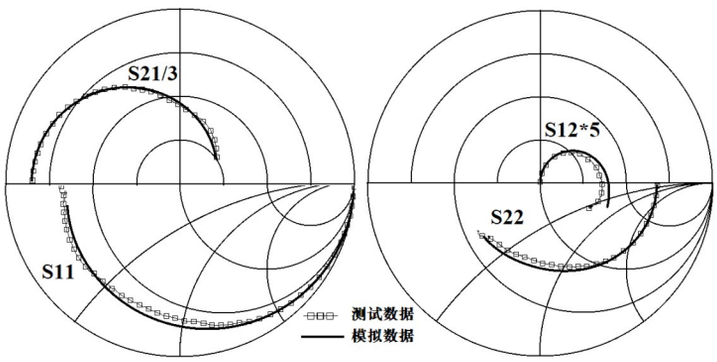
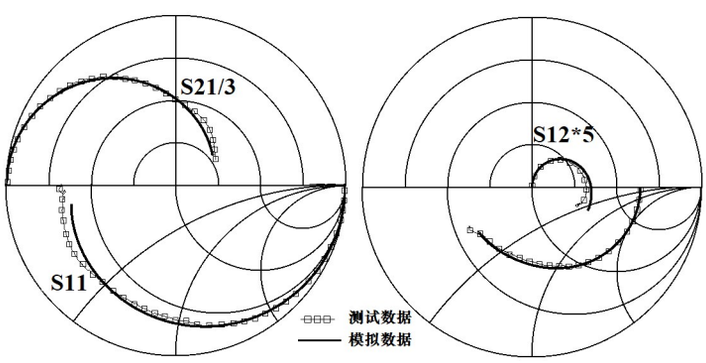
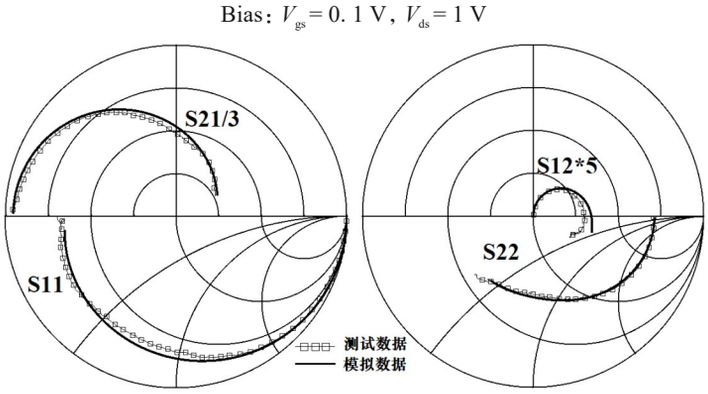


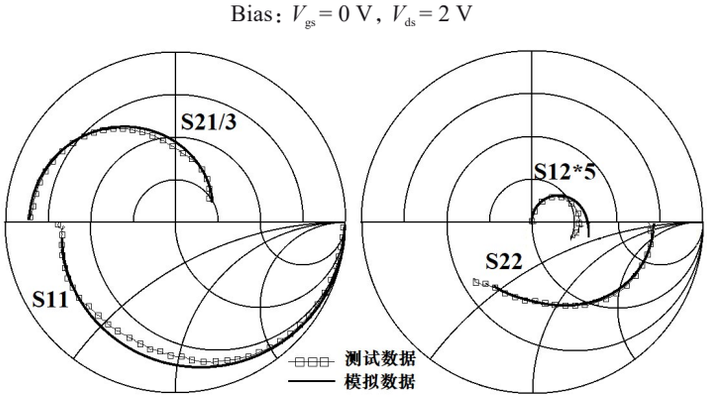
Bias: V_{gs} = 0 V, V_{ds} = 1 V



Bias: V_{gs} = 0. 1 V, V_{ds} = 1 V



Bias: V_{gs} = 0 V, V_{ds} = 2 V



Bias: V_{gs} = 0. 1 V, V_{ds} = 2 V

Fig. 5 Comparison between simulated (lines) and measured (squares) *S*-parameters over the frequency range going: from 1 GHz to 110 GHz under multi bias

图 5 1 ~110 GHz 频率范围内多偏置下模拟和测量S参数对比曲线

Table 4 Accuracy of *S*-parameters
表 4 S参数精度

Bias Condition	S_{11}	S_{12}	S_{21}	S_{22}
V_{ds} = 1V, V_{gs} = 0V	5.45%	1.55%	4.37%	2.59%
V_{ds} = 1V, V_{gs} = 0.1V	5.46%	1.46%	4.26%	2.45%
V_{ds} = 2V, V_{gs} = 0V	4.99%	1.85%	4.80%	2.74%
V_{ds} = 2V, V_{gs} = 0.1V	5.82%	1.97%	4.97%	4.04%

tionbased parameter-extraction procedures for FET small-signal models[J]. *IEEE Transactions on Microwave Theory and Techniques*, 1998, **46**(11):1620-1627.
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