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InGaAs/InAlAs InP-based HEMT with the current cutoff frequency of 441 GHz

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Abstract: In this letter, an $In_{0.53}Ga_{0.47}As/In_{0.52}Al_{0.48}As$ InP-based HEMT with $f_T > 400$ GHz was designed and fabricated successfully. A narrow gate recess technology was used to optimize the parasitic resistances. The gate length is 54.4 nm, and the gate width is 2 × 50 μm. The maximum drain current $I_{DS.max}$ is 957 mA/mm, and the maximum transconductance $g_{m.max}$ is 1 265 mS/mm. The current gain cutoff frequency f_T is as high as 441 GHz and the maximum oscillation frequency f_{max} reaches 299 GHz, even at a relatively small value of V_{DS} = 0.7 V. The reported device can be applied to terahertz monolithic integrated amplifiers and other circuits.

Key words: InP HEMTs, InGaAs/InAlAs, current gain cutoff frequency (f_T), maximum oscillation frequency (f_{max}), gate recess

电流增益截止频率为 441 GHz 的 InGaAs/InAlAs InP HEMT

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摘要:本文设计并制作了$f_T > 400$ GHz 的 $In_{0.53}Ga_{0.47}As/In_{0.52}Al_{0.48}As$ 铟磷高电子迁移率晶体管(InP HEMT)。采用窄栅槽技术优化了寄生电阻。器件栅长为 54.4 nm,栅宽为 2 × 50 μm。最大漏极电流 $I_{DS,max}$ 为 957 mA/mm,最大跨导 $g_{m.max}$ 为 1 265 mS/mm。即使在相对较小的 V_{DS} = 0.7 V 下,电流增益截止频率 f_T 达到了 441 GHz,最大振荡频率 f_{max} 达到了 299 GHz。该器件可应用于太赫兹单片集成放大器和其他电路中。

关 键 词:铟磷高电子迁移率晶体管(InP HEMTs);InGaAs/InAlAs;电流增益截止频率(f_T);最大振荡频率(f_{max});栅槽

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Introduction

The InP based terahertz monolithic integrated circuit (TMIC) have potentials for applications in plenty of fields, such as high-resolution security imaging systems[1], revolutionary communication networks[2], and radio astronomy[3]. InP-based InGaAs/InAlAs HEMTs have demonstrated high operating frequency, low noise, high-gain performance, as well as good radiation resistance[4], making them an important device for InP based TMIC.

In recent years, the requirements for higher operation frequency and larger output power of TMIC result in a strong push of THz transistor technologies with current gain cutoff frequency (f_T) and maximum oscillation frequency (f_{max}). The operating frequencies of integrated circuit amplifiers have seen corresponding increase to as high as 1 THz, with InP HEMTs reaching 1.5 THz f_{max} and 610 GHz f_T[5]. And the recent literature reported the current record of f_T = 738 GHz with a gate length of 19 nm[6]. Various efforts have been made to improve the f_T of InP based HEMTs, such as reducing the gate length (L_g)[7], source-to-drain spacing (L_{SD})[8], and gate-to-channel dis-

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tance (t_{ins})[9], as well as optimizing the channel layer[10-11] and the gate recess[12]. All the above measures are for minimizing the parasitic resistances, capacitances and increasing the transconductance.

In this letter, a narrow gate recess technology was used to optimize the parasitic resistances of InP based HEMTs. The $In_{0.53}Ga_{0.47}As/In_{0.52}Al_{0.48}As$ HEMTs with gate length of 54.4 nm were fabricated. The values of f_T and f_{max} are as high as 441 GHz and 299 GHz, the maximum drain current $I_{DS.max}$ is 957 mA/mm, and the maximum transconductance $g_{m.max}$ is 1265 mS/mm. The InP based HEMTs with such high performances can be applied to terahertz monolithic integrated (TMIC) amplifiers and other circuits.

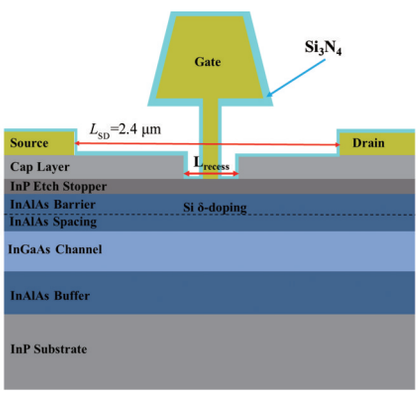


Fig. 1 A schematic cross-section of InP-based HEMT
图1 InP HEMT的截面示意图

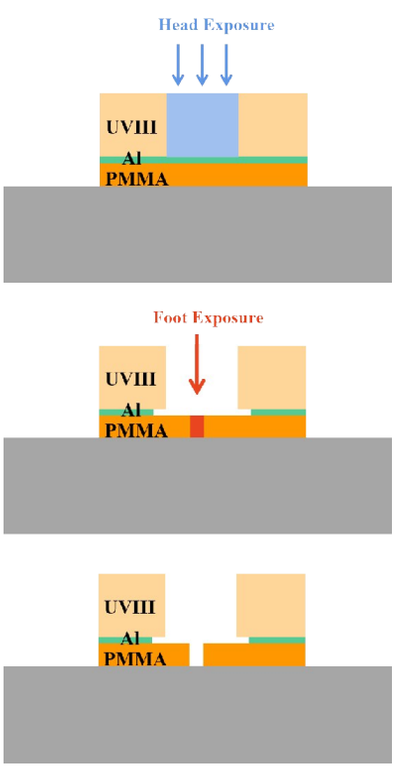


Fig. 2 The EBL process with a PMMA/Al/UVIII resist stack
图2 PMMA/Al/UVIII光刻胶堆叠的电子束光刻工艺

1 Experiment

The Schematic cross-section of InP-based HEMTs is shown in Fig. 1. The epitaxial layers of the devices were grown by gas source molecular beam epitaxy (GSMBE) on 3 inch semi-insulating InP (100) substrates. From bottom to top, the layers consists of a 500-nm $In_{0.52}Al_{0.48}As$ buffer layer, a 10-nm $In_{0.53}Ga_{0.47}As$ channel layer, a 3-nm unstrained $In_{0.52}Al_{0.48}As$ spacer layer, Si delta doping layer with $5\times10^{12}cm^{-2}$ doping concentration, a 8-nm unstrained $In_{0.52}Al_{0.48}As$ Schottky barrier layer, a 4-nm InP etch-stop layer for preventing over etching and a 40-nm multi-layer cap layer that combines heavily-droped $In_{0.52}Al_{0.48}As/In_{0.53}Ga_{0.47}As$ and a heavily-droped $In_{0.65}Ga_{0.35}As$ upper cap layer. Hall measurements from a Hall calibration epitaxial layer structure were made at room temperature, showing a carrier mobility of over 10 000 $cm^2/(Vs)$.

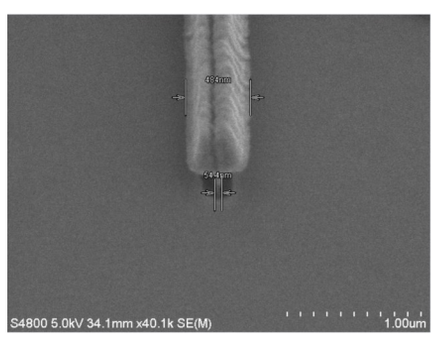


Fig. 3 SEM photograph of the T-Gate and gate recess of the InGaAs/InAlAs HEMT
图3 InGaAs/InAlAs HEMT的T型栅和栅槽的SEM照片

The fabrication process of InP HEMTs mainly contains five steps, including mesa isolation, ohmic contact formation, gate recesses, T-Gates, and connection pads, which is similar to our previously reported devices[13]. Isolating mesa was formed by phosphoric acid-based wet etching down to the InAlAs buffer layer. Source and drain electrodes were defined by electron beam lithography (EBL) with a 2.4-μm distance. Ti/Pt/Au (15 nm/15 nm/50 nm) was evaporated and lifted off to form the source and drain contacts, with contact resistance measured to be 0.023 Ω•mm and the specific contact resistivity 8.75E-8 Ω•cm^2 by TLM method.

Subsequently, the trilayer e-beam resist process was applied to fabricate 50-nm-gate-length T-gates. The gate process was developed by EBL with a PMMA/Al/UVIII (200 nm/10 nm/800 nm) resist stack, which is shown in Fig. 2. The top UVIII resist was exposed by a small dose and wide line. After that, the gate head was determined by TMAH development and rinsed in DI water. Subsequently, the gate foot was defined on a single layer of PMMA resist and was exposed by a big dose and narrow line. This approach allows better focusing at the gate foot exposure step because of the thin PMMA resist. As a result, this process scheme allows a small L_g. After that, the 200 nm gate recess was etched to InP etch-stop layer by H_3PO_4-solution, and a Ti/Pt/Au (25 nm/25 nm/

350 nm) T-gate was evaporated and lifted off. The length of the T-Gate is 54.4 nm, as shown in Fig. 3. Finally, the Ti/Au (15 nm/400 nm) connection pads were evaporated for on-wafer DC and RF characteristics measurements.

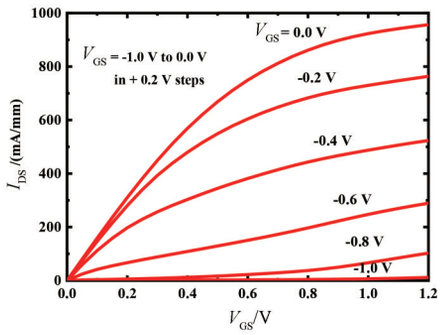
2 Results and Discussion

DC properties were characterized by using a HP4142 semiconductor parameter analyzer at room temperature. Figure 4(a) shows the current-voltage (I–V) characteristics of the HEMT with L_g = 54.4 nm and gate width W_g = 2×50 μm at room temperature. The gate-source voltage (V_{GS}) is increased from -1.0 V to 0.0 V with step of +0.2 V, and the drain-source voltage (V_{DS}) changes from 0 V to 1.2 V. The $I_{DS.\,max}$ @ V_{GS} = 0.0 V is 957 mA/mm. The $I_{DS.\,max}$ is enhanced compared to our previously reported InP HEMTs[14] and is attributed to the reduction of gate length. The device shows a small value of ON-resistance (R_{ON} = 0.667 Ω•mm) due to a relatively narrow gate recess. Because the narrow gate recess leads to reduction of R_S and R_D[15]. Moreover, the kink effect of the device is negligible due to the introduction of the InP etching-stopper layer.

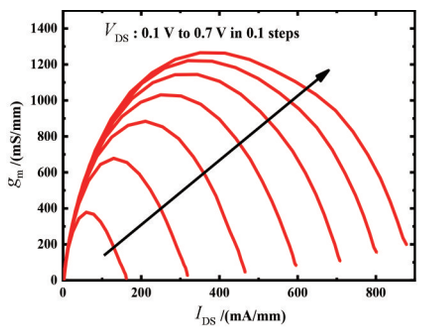
Figure 4(b) plots the measured transconductance (g_m) of the L_g = 54.4 nm device as a function of I_{DS}, for various vaules of V_{DS} from 0.1 V to 0.7 V in + 0.1 V steps. A maximum extrinsic transconductance $g_{m.\,max}$ of 1 265 mS/mm is achieved at V_{DS} = 0.7 V. The pinch-off voltage is about -0.73 V at V_{DS} = 0.7 V as shown in Fig. 3(c).

The RF characteristics were measured using an Agilent E8363B PNA vector network analyzer from 0.1 GHz to 50 GHz. Before the RF test, the equipment was calibrated to eliminate systematic errors due to the environment or test equipment. In order to accurately obtain the S-parameter of the device, we calibrated the test reference surface to the GSG test probe tip. The open and short structures were used to substract pad-related capacitance and inductance components from measured S-parameters. Then, the values of a short-circuit current gain (H_{21}), a maximum available gain and a maximum stable gain (MAG/MSG), and a Mason's unilateral gain (U) were plotted in Fig. 5(a). The bias condition was at V_{GS} = -0.35 V and V_{DS} = 0.7 V.

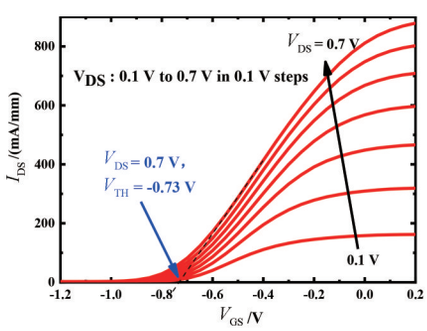
Since the test frequency range was limited from 0.1 GHz to 50 GHz, we obtained a value of f_T = 441 GHz by extrapolating the measured H_{21} with a slope of -20 dB/dec. Regarding f_{max}, it cannot be directly extracted from the measured U or MAG/MSG. This is because it is difficult to observe a decline in the MAG/MSG frequency curve with a slope of -20 dB/dec in a limited test range. Therefore, if the frequency curve of MAG/MSG is extrapolated with -20 dB/dec at 50 GHz, the f_{max} obtained is a conservative result. So, we constructed a small-signal model that yielded a well behaved U with a single-pole system, as shown in Fig. 5(b)[16]. Using the small-signal model, the values of f_{max} = 299 GHz and f_T = 443 GHz were estimated accurately. The measured $f_{T\_measure}$ and the modeled f_{T_model} are similar, increasing the credibility of our model.



(a)



(b)



(c)

Fig. 4　(a) DC output characteristics, (b) g_m against I_{DS}, and (c) transfer characteristics of the HEMT
图4　HEMT的 (a)直流输出特性,(b)跨导, (c) 传输特性

The f_T and f_{max} are expressed as equtions (1) and (2):

$$f_T = \frac{g_{mi}}{2\pi\{(C_{gs}+C_{gd})[1+g_{ds}(R_s+R_d)]+C_{gd}g_{mi}(R_s+R_d)\}} \quad ,(1)$$

$$f_{max} = \frac{f_T}{\sqrt{4g_{ds}(R_g+R_i+R_s)+\frac{2C_{gd}}{C_{gs}}\left(\frac{C_{gd}}{C_{gs}}+g_{mi}(R_i+R_s)\right)}} \quad ,(2)$$

Where C_{gs} and C_{gd} are the capacitances in between gate to source and gate to drain; R_g, R_S, and R_D are the parasitic resistances of gate, source and drain; g_{mi} is the intrinsic transconductance; g_{ds} is the conductance between drain and source.

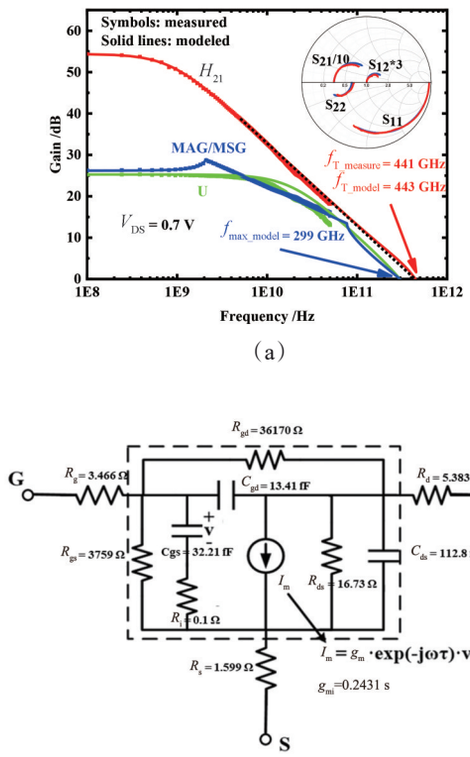


Fig. 5 (a) The measured and modeled H_{21}, MAG/MSG and U gains versus frequency for the L_g = 54.4 nm InGaAs/InAlAs HEMT at V_{GS} = -0.35 V and V_{DS} = 0.7 V, and (b) small-signal equivalent circuit model used in pervious work[16]

图5 (a)在 V_{GS} = -0.35 V 和 V_{DS} = 0.7 V 时,栅长为 54.4 nm 的 InGaAs/InAlAs HEMT 器件,其 H_{21}、MAG/MSG 和 U 的测试结果和模型结果与频率的关系,以及(b)小信号等效电路模型[16]

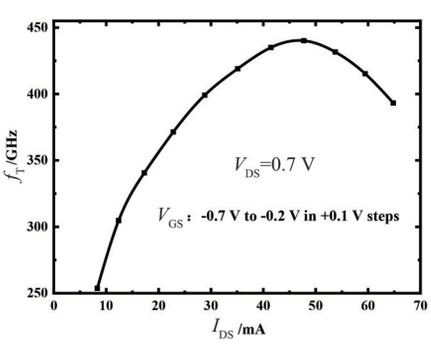


Fig. 6 Measured f_T against I_{DS} of the L_g = 54.4 nm InGaAs/InAlAs HEMT with V_{DS} = 0.7 V

图6 在 V_{DS} = 0.7 V 时,InGaAs/InAlAs HEMT 的 fT 随 I_{DS} 的变化

Equations (1) and (2) suggest that C_{gs}, C_{gd}, R_S, R_D, g_{mi} and g_{ds} are the key parameters that affect f_T and f_{max}. Table 1 shows small-signal model parameters. These key parameters are all related to the size of the gate recesse and gate length. In terms of f_T, the small gate length reduces capacitances and increases g_{mi}. At the same time, the narrow gate recess also reduces the R_S and R_D. So, these affects lead to a higher f_T = 441 GHz. However, the narrow gate recesse correspond to larger values of C_{gd}/C_{gs}, and the shorter gate length leads to larger R_g and g_{ds}, which leads to a smaller f_{max} = 299 GHz.

Figure 6 plots the extracted f_T as a function of I_{DS} for the same device at V_{DS} = 0.7 V, which consists with the g_m against I_{DS} in Fig. 4. The f_T of the device exceeds 400 GHz over a wide range of I_{DS}.

Table 2 shows the reported the performance of InGaAs/InAlAs HEMTs with L_g from 50 nm to 75 nm. What these devices have in common is that the channel of devices are indium-rich InGaAs. And Pt buried gate technology is used to decrease the gate-to-channel distance, resulting the excellent RF performance. Although the values of $g_{m.max}$ and f_T are quite different, the larger $g_{m.max}$ corresponds to higher $f_T$in this table. Compared with these results, our device achieved the f_T of over 400 GHz with the lowest $g_{m.max}$, and we need to improve f_T through further increasing $g_{m.max}$ in the future.

3 Conclusion

In summary, we have successfully designed and fabricated a 54.4 nm T-gate InGaAs/InAlAs InP-based HEMT with f_T > 400 GHz. In order to optimize the parasitic resistances, we adopt a narrow gate recess technology. As a result, the f_T reaches as high as 441 GHz with a $g_{m.max}$ of 1265 mS/mm. The f_T is expected to be promoted through further increasing $g_{m.max}$ by adopting an Indium-rich channel and a Pt buried gate technology.

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Table 1　Small-signal model parameters of the L_g = 54.4 nm InGaAs/InAlAs HEMTs at V_{DS} = 0.7 V, with different structures

表1　V_{DS} = 0.7 V时,栅长为54.4 nm的 InGaAs/InAlAs HEMT的小信号模型参数

C_{gs}[fF/mm]	C_{gd}[fF/mm]	C_{ds}[fF/mm]	g_{mi}[mS/mm]	g_{ds}[mS/mm]	R_i[Ω•mm]	R_g[Ω•mm]
322. 1	134. 1	1 124	2 431	597. 7	0. 01	0. 346 6
C_D[Ω•mm]	R_S[Ω•mm]	R_{gs}[Ω•mm]	R_{gd}[Ω•mm]	$f_{T\_measure}$[GHz]	f_{T_model}[GHz]	f_{max_model}[GHz]
0. 538 3	0. 159 9	375. 9	3 617	441	443	299

Table 2　Comparison with published InGaAs(InAs)/InAlAs HEMTs with L_g from 50 nm to 75 nm

表2　与已发表的栅长从50 nm到75 nm的InGaAs(InAs)/InAlAs HEMT性能的比较

Ref.	L_g/nm	Gate metal	Channel	g_m/(mS/mm)	f_T/GHz (V_{DS}/V)	f_{max}/GHz (V_{DS}/V)
17	50	Pt/Ti/Pt/Au	InAs	2 000	496 (0. 6)	400 (0. 6)
18	50	Pt/Ti/Pt/Au	$In_{0.7}Ga_{0.3}As$	1 750	465 (0. 75)	1 060 (0. 75)
19	60	Pt/Ti/Pt/Au	InAs	2 100	580 (0. 6)	675 (0. 6)
20	60	Pt/Ti/Pt/Au	InAs	2 114	710 (0. 5)	478 (0. 5)
21	70	Ti/Pt/Au	$In_{0.7}Ga_{0.3}As$	1 600	310 (1. 2)	540 (1. 2)
22	75	Ti/Pt/Au	InAs	1 331	260 (1. 0)	800 (1. 0)
This work	54. 4	Ti/Pt/Au	$In_{0.53}Ga_{0.47}As$	1 265	441 (0. 7)	299 (0. 7)

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