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High efficiency 285 GHz tripler based on face-to-face differential configuration

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Abstract: A high efficiency 285 GHz Schottky diode tripler has been demonstrated based on the face-to-face differential configuration. The proposed concept could improve the power handling capability by a factor of two compared to the traditional balanced circuit based on on-chip capacitors. Meanwhile, the tripler could provide improved DC bias networks with perfect amplitude and phase balance, which shows lower insert losses by leaving out the high required on-chip bypass capacitor. The proposed triple frequency multiplier features inherent suppression on even-order harmonics with the face-to-face differential topology, which ensures better conversion efficiency with doubled anodes. The fabricated tripler has been proved to exhibit a 12% peak efficiency for a nominal driven power of 140~210 mW.

Key words: balanced, frequency tripler, THz, power handling, Schottky diode

PACS: 85.30.Hi, 85.30.Kk, 84.30.Vn, 07.57.Hm

基于对差分结构的高效率285GHz三倍频器

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摘要:实现了一种基于“对差分”结构的高效率285 GHz三倍频器。相比于传统的基于片上旁路电容的平衡式三倍频电路,这种理念能够将电路的功率容量提高一倍。同时,这种结构的三倍频能够提供高度的幅度和相位平衡性,进而实现更好的直流馈电回路,并通过省去高工艺需求的片上电容而降低了相应的插入损耗。同样,这种电路能够通过“对差分”结构实现偶次谐波的本征抑制,从而保证了在管结数量倍增前提下的更高变频效率。测试结果表明该三倍频器能够在140~210 mW的驱动功率条件下提供12%的最高效率。

关 键 词:平衡式;三倍频器;太赫兹;功率容量;肖特基二极管

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Introduction

Act as the local oscillator sources of heterodyne transceiver, Schottky diode based sources continue to be the most preferred devices for power generation at frequencies from 100 GHz to 1THz in variety of applications. The coming terahertz heterodyne array applications such as radar imagers[1] and high data rate communication systems[2] certainly put forward the requirement for higher power levels provided by Schottky-based multipliers operating in the 100~300 GHz.

Typically, Schottky-based doublers and triplers play critical roles in the commonly applied terahertz multiplier sources. In general, imbalanced multiplies always need a pair of filtering networks at the input and output to achieve the harmonic selection. As a result, these cir-

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cuits always suffer from poor conversion efficiencies and bandwidth properties due to the insert loss and quality factor of filters[3]. Thus, balanced multipliers have become the standard topology for frequency multiplication due to their good performance[4]. The design of balanced doubler has been well-developed based on the so called Erickson-style circuits, which exhibits high efficiency with low fabrication process requirement[5-6]. On the contrary, the classical balanced triple frequency multipliers[6] certainly rely on an on-chip capacitor to fulfill the RF grounding as well as dc biasing requirements (as shown in Fig. 1), which could not be fabricated by the conventional thin-film process with discrete Schottky diodes. Thus, this kind of balanced triplers might be more suitable for MMIC technology since their requirement on a high performance on-chip metal-insulator-metal (MIM) capacitor for biasing. Moreover, Kamaljeet S. Saini[7] has proved the equivalent series resistances and Q factor of the on-chip capacitors to be 3.5~20 Ω and 2~7.2, respectively. Thus, the Metal-Insulator-Metal (MIM) bypass capacitor used in the classical tripler features significant series resistance which could introduce the unwanted imbalance effect and reduce the conversion efficiency as a result. Thus, several biasing schemes without bypass capacitor for balanced frequency tripler have been presented in recent years[7]. However, these configurations always require coupled lines to provide circuit balances and DC path, which suffer limited bandwidth and conversion efficiencies with separate biases in different polarity.

This work demonstrates a 285 GHz triple frequency multiplier based on the face-to-face differential configuration. The proposed configuration is absolutely symmetrical which features simple DC-bias path without the on-chip capacitor and increase the power handling by a factor of two compared to the topology in Fig. 1. Due to this novel architecture, the proposed tripler are able to be fabricated with the conventional thin-film process and discrete Schottky diodes. Moreover, this work applies the proposed architecture to fabricate a balanced frequency tripler with output frequency from 265 to 296 GHz based on discrete GaAs varactors glued on a 30 μm-thick quartz substrate. At room temperature, the achieved peak efficiency is proved to be 12.5% at 294 GHz with a related output power of 21 mW.

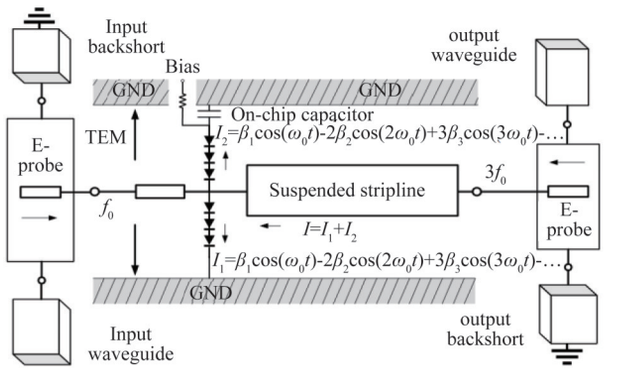


Fig. 1 Diagram of the classical balanced tripler relying on on-chip MIM capacitor
图1 基于片上MIM电容的经典平衡式三倍频电路图

1 Architecture

The proposed face-to-face differential tripler configuration is motivated by the requirement of replacing redundant bypass capacitor in terahertz frequency range, which is first reported in our previous work[10]. Figure 2 (a) shows the basic topology of the face-to-face differential tripler demonstrated in this work. The proposed face-to-face differential configuration means the 180-degree power splitter (*E*-plane *Y*-junction structure) and *E*-plane probe-based 180-degree dividing/combing structure which are arranged face to face for suppression on odd-order harmonics. As shown in Fig. 2, the *E*-plane *Y*-junction structure could divide the input signals into a pair of differential outputs at f_0, which would be transferred into the suspended microstrip networks by the *E*-plane probes. Thus, two diode pairs with the same polarity in Fig. 2(a) would be excited by the driven powers (f_0) with opposite phase and same amplitude. According to Ref. [11], the upper and lower diode pair in Fig. 2 (a) would generate the harmonic current I_1 and I_2, respectively. Expressions of I_1 and I_2 are illustrated in Fig. 2, which means the generated signals are out-of-phase ((2*n*+1) *180deg) at odd-order harmonics and in-phase (2*n**180deg) at even order harmonics due to the

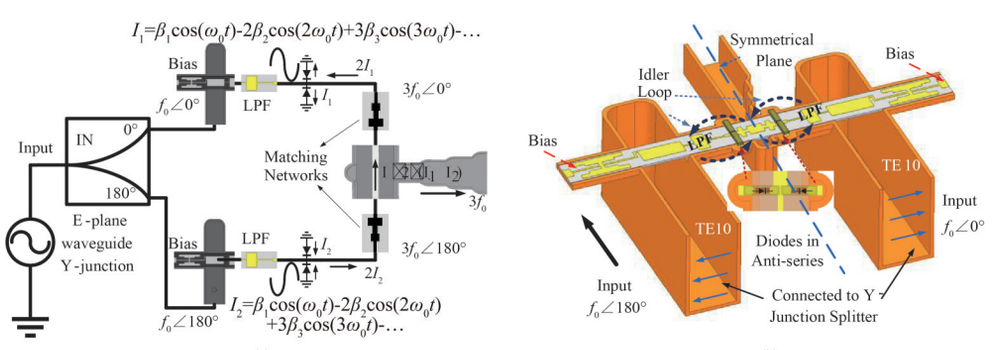


Fig. 2 (a) Diagram of the face-to-face balanced tripler architecture, (b) 3D-view of the proposed configuration
图2 (a)对差分平衡式三倍频电路图,(b) 电路三维示意图

frequency multiplication. Meanwhile, the output power combination structure exhibits a phase difference of 180deg (at $f_0, 2f_0, 3f_0, 4f_0$) between its two stripline ports. As a result, even-order harmonics would be highly suppressed at output *E*-probe. Thus, the combined current in the E-plane probe-based combining structure at the output could be expressed as $I=I_1+I_2$, which only comprises the odd harmonics and result in a balanced frequency tripler. So, this topology establishes the balance through a couple of differential input and output structures rather than a bypass capacitor required in traditional circuit. And the symmetrical plane in Fig. 2(b) can be regarded as a virtual ground for even harmonics, which traps the second harmonics in Loop1 and Loop2 with the low pass filters(LPF).

2 Design

The first step to design the balanced circuit is determining the optimum embedding impedances presenting to each varactor at the fundamental, second and third harmonics. As the design objective was to maximize conversion efficiency, a harmonic balance analysis by Advanced Design System (ADS) from Keysight has been performed to ensure the optimum embedding impedances to present to each junction. Dimensions of the adopted diodes are 230 μm*45 μm*20 μm, which should be comparable with the wavelength at 285 GHz. Thus, evaluation of the optimum embedding impedances must consider the influences of the diode on field distribution. These determined impedances to fundamental waves (95 GHz) have been simulated to be 23.5+*j**49.3 (Ω), while to second and third harmonics are 0.5+*j**41.2 (Ω) and 19.86+*j**52 (Ω), respectively. In order to achieve the proposed impedances matching, the whole circuit could be divided into three parts: 1) an *E*-plane *Y*-junction power splitter integrated with waveguide-to-microstrip transition structures; 2) suspended matching and filtering networks; and 3) an E-plane probe-based power differential combining structure in the WR-3.4 waveguides (f_cTE10=174 GHz). According to the power over 30 mW dissipated per junction in 90~100 GHz range, the discrete Schottky diodes are selected to have a zero-bias junction capacitance of 25 fF, reverse breakdown voltage of about 10 V, and a series resistance approximately 4 Ω. The diode model used in this work comes from our previous work, which extracted the parameters from measured *I*/*V* and *C*－*V* curves [13]. Extensive simulations were done to maximum tripler efficiency. The design process is iterative, including 3-D electromagnetic simulations using Ansoft's High-Frequency Structure Simulator (HFSS) and harmonic balance analysis using Keysight's Advanced Design System (ADS).

As mentioned above, the input signals operating in WR10 waveguide should be divided into two parts with equal amplitude and opposite phase at f_0 over the bandwidth through the *E*-plane *Y*-junction waveguide power splitter shown in Fig. 3(a). Arrows in black represent the electrical field distributions of the power splitter. It could be noted that the designed *Y*-junction splitter features almost the same amplitude with a phase difference of 180 degrees. Then, a pair of E-plane probes (integrated with dc path) in mirror symmetry are driven by the differential waves in Port2 and Port3, which couples the fundamental signals in TE10 mode to the suspended networks which operating in quasi-TEM mode and result in the differential outputs in Port4 and Port5 (shown in Fig. 3(b)). The amplitude and phase relations at Port4 and Port5 are indicated by different waveforms in Fig. 3(b), which act as the driven signals to the diode pairs.

The suspended networks feature a series of high and low impedance sections which could match the varactors and prevent the high order harmonics including $2f_0$ and $3f_0$ from leaking into the input waveguide. As shown in Fig. 4, the directions of *E*-fields in this mirror-symmetric networks are totally opposite, which results in the related harmonic currents represented by the arrows in red. As a result, diode pair on left side and right side would be excited under different polarity, which results in the expressions of I_1 and I_2. The same signs in the expressions of I_1 and I_2 indicates the same harmonic current directions, while the different ones represent different current at the

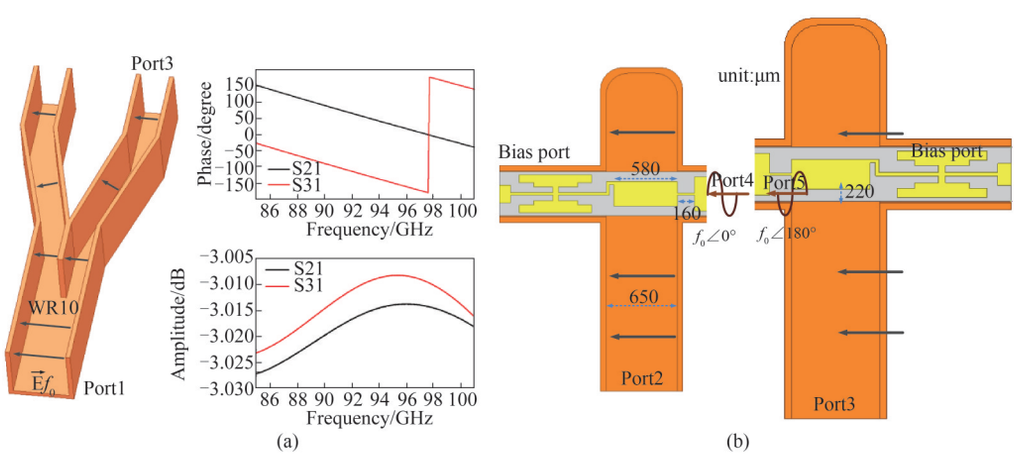


Fig. 3　(a) *E*-plane *Y*-junction waveguide power splitter and its amplitude and phase properties, (b) diagram of the *E*-plane waveguide-to-microstrip transition structure pair

图3　(a)E面波导Y型结功分器及其幅相特性,(b) E面波导-微带探针对结构图

related harmonics.

The 180-degree combining structure in Fig. 5 acts as the critical combination of I_1 and I_2 from Port6 and Port7 in red. The proposed *E*-plane probe-based differential combing structure features great amplitude balance between two suspended ports, which also exhibits flat input impedances (Z_{in}) to match the varactors. Thus, the even order components in I_1 and I_2 would be totally trapped between the low pass filters(LPF) and the virtual ground plane represented by red dotted line in Fig. 2 (b). On the contrary, odd-harmonics current components in I_1 and I_2 would be combined in-phase at the output probe, where the fundamental harmonic is cut off by the WR3. 4 waveguides.

The demonstrated tripler is a split-block waveguide module that features twelve Schottky varactors glued on a 30 μm-thick quartz-based substrate with a dimension of 4946 μm×400 μm, as shown in Fig. 6. The whole *E*-plane split-waveguide block is fabricated by computer numerical control milling technology with a volume of 20 mm*20 mm*20 mm. The whole planar chip is inserted in the suspended channel with a cross section of 420 μm×300 μm, which could cut off the waveguide field distribution of waves at frequencies higher than 320 GHz. It is worth to notice that the module only needs one external bias but is supplied with two glass insulators to ensure the perfect circuit symmetry. Two utilized discrete diodes in anti-series (totally six junctions) are carefully glued on the 30-μm-thick quartz substrate with one pad directly on the waveguide block, which provides better thermal conductance to prevent the junctions from thermal breakdown.

3 Results and discussion

The 265~294 GHz *E*-plane split-waveguide module is fabricated by computer numerical control milling technology with dimension variations of ±5 μm. As shown in Fig. 6, the whole module comprises a WR-12 *Y*-junction splitter, a pair of multiplying cells and a differential output *E*-probe. During the fabrication, each cell contains a pair of discrete GaAs diodes which are carefully selected to minimize the series resistance and junction capacitance differences.

The measurement platform to measure the frequency response of the 285 GHz tripler is illustrated in Fig. 7. During the test, a MMIC-based multiplier module has been fabricated to multiply the inputs (11~12. 5 GHz)

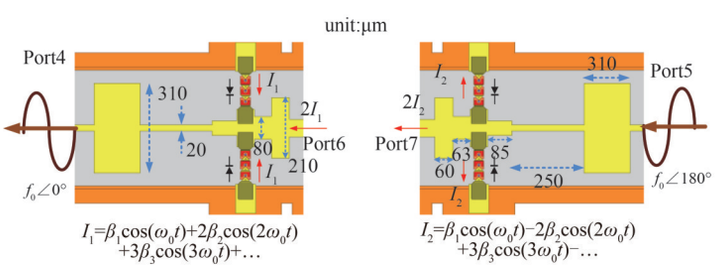


Fig. 4 Suspended matching and filtering networks including diode pairs in mirror symmetry
图4 包含二极管对的镜像对称悬置匹配滤波网络

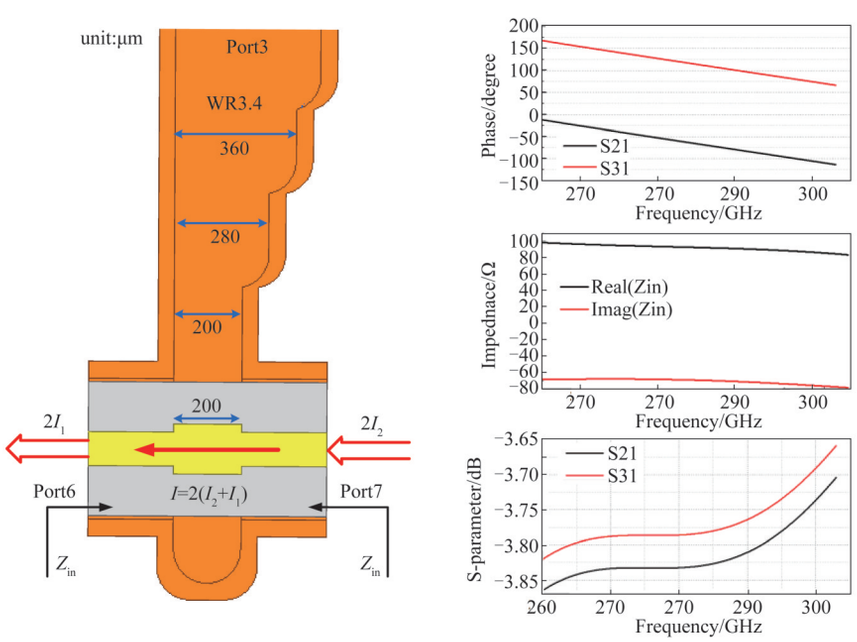
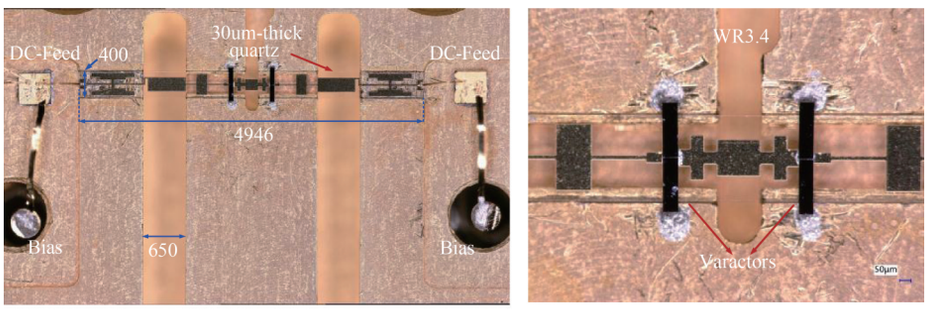


Fig. 5 *E*-plane probe-based differential combining structure with related performances
图5 基于E面探针的差分功率合成结构及其相应的仿真性能



(a)　　(b)

Fig. 6　Photograph of the fabricated balanced tripler module and its details
图6　实现的平衡式三倍频电路模块照片及其细节

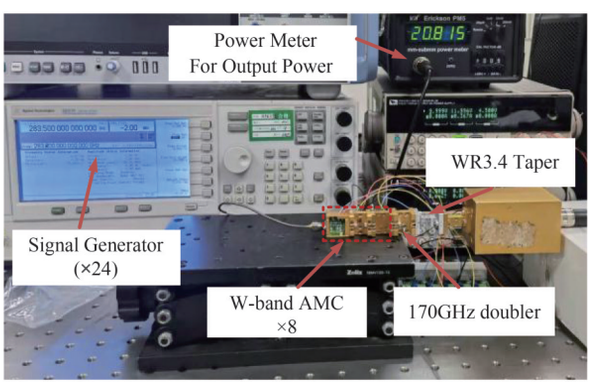


Fig. 7　Measurement platform of the balanced tripler module
图7　平衡三倍频电路测试平台

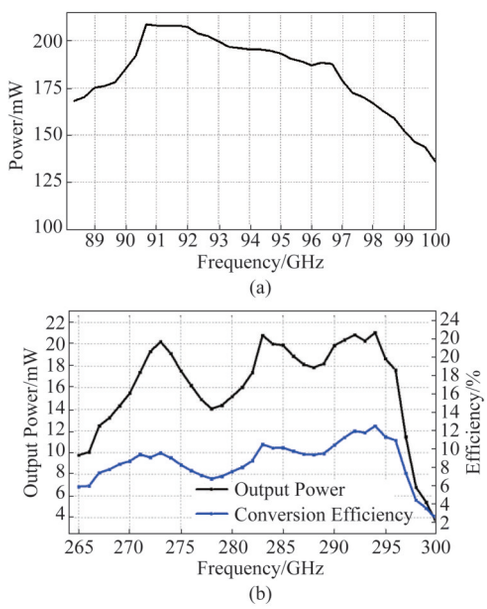


Fig. 8　(a) Driven power of the proposed tripler module, (b) measured performances of the fabricated balanced tripler module
图8　(a)三倍频模块测试时的驱动功率,(b)三倍频模块的测试性能曲线

from the Agilent E8257D synthesizer by eight times with an output power over 5 mW, which would be amplified to over 50 mW by the medium amplifier in cascade. Moreover, a self-developed amplifier module has been utilized to provide the required waves in the range from 88 to 100 GHz, with a saturation power of 25 dBm. And an Erickson PM5 power meter was used to calibrate the input power of tripler at each measured frequency point, cooperating with a 10-dB isolator. And the measured output power of the driven chain is illustrated in Fig. 8(a). To achieve the best performance, each anode of the diodes was biased between -3.3 V through those two bias glass insulators which were tied together and connected to the external voltage. A WR3.4 to WR10 taper has been used to measure the output power range from 265 to 300 GHz. To maximize the available input power, the diode tripler was connected directly to the W-band amplifier which leads to the lack of return loss measurement. With the calibration of WR3.4 to WR10 taper, the proposed 285 GHz tripler exhibits an output power morn than 10 mW in the range of 265~296 GHz. At room temperature, the achieved peak efficiency is proved to be 12.5% at 294 GHz with a related output power of 21 mW. The demonstrated tripler could handle more than 300 mW at the input, which holds the potential of providing higher output power in this range.

Comparisons between the simulated and measured results have also been carried out in this work, as shown in Fig. 9. Accordingly, the difference between the measured and simulated output power is less than 2 dB over the whole operation frequency range, which proves a great simulation accuracy. But there is a small discrepancy when it comes to the whole output power curve. The actual device seems to work better at both ends of the operating band than the predicted results, which is believed to be caused by variations in the fabrication and assembly process. Meanwhile, the measured output power exhibits larger ripples than the simulated one, especially in the range of 275~285 GHz. This phenomenon is probably caused by the standing wave between the tripler and its driven stage.

Table 1 compares this work with the recently reported sub-millimeter frequency triplers. On the one hand, the balanced topology in this work shows better conversion efficiency and bandwidth compared to the imbalanced ones in Ref. [3]. On the other hand, the face-to-face differential structure allows significant reduction in waveguide losses by drastically reducing the electrical length, which provides the same potential in efficiency and fractional bandwidth as traditional balanced power-

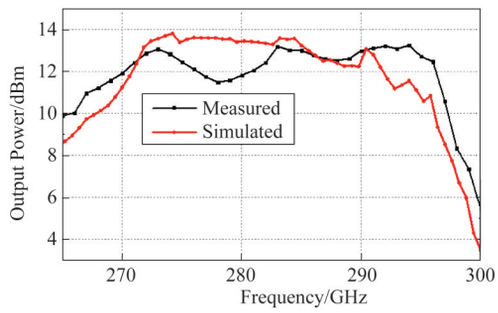


Fig. 9 Comparisons of the simulated and measured output power of the balanced tripler module
图9 平衡三倍频电路输出功率的仿真实测曲线对比

combined tripler circuits in Ref. [7] and [12]. Even without the use of on-chip capacitors, this architecture is believed to exhibit better performance when fabricated with the monolithic integrated techniques.

Table 1 Comparison of several tripler in adjacent frequency ranges
表1 相近频段的几种三倍频电路比较

Ref	Balanced or not	On-chip Capacitor	Diodes quantity	Freq/GHz FBW/(%)	Peak power /mW	Efficiency /(%)
[3]	not	no	2	208~220 ~5	38.2	5~17.8
[7]	yes	yes	4	265~300 12.5	26	5~15
[9]	yes	no	4	89~94 ~5	20	5~25
[12]	yes	yes	4	105~120 17	~200	20~30
This Work	yes	no	4	265~296 ~11	21	7~12.5

4 Conclusions

A 265~294 GHz triple frequency multiplier has been demonstrated in this work based on the novel balanced topology, which utilizes two symmetrical multiplying cells to suppress the even-order harmonics without any on-chip capacitor. Given the doubled number of Schottky junctions, the proposed circuit should produce approximately twice as many power as traditional designs without any compromise in efficiency or bandwidth. This configuration is expected to be able to accept over 400 mW at the input with improved thermal arrangements, which leads to over 30 mW at 290GHz in the future.

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