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Small signal model and low noise application of InAlAs/InGaAs/InP-based PHEMTs

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Abstract: This paper presents an improved small-signal model and a W-band monolithic low noise amplifier (LNA) using 100 nm InAlAs/InGaAs/InP-based high electron mobility transistors (HEMT) technology. For improving the fitting accuracy of S-parameters in low frequency, the small-signal model takes into account differential resistances of gate-to-source and gate-to-drain diodes, which modeled by resistances R_{fs} and R_{fd}. A W-band LNA monolithic millimeter-wave integrated circuit (MMIC) has been designed and fabricated based on this model to verify the feasibility of this model. The amplifier is measured on-wafer with a small-signal peak gain of 14.4 dB at 92.5 GHz and 3-dB bandwidth from 85 to 110 GHz. In addition, the MMIC also exhibits an excellent noise characteristic with the noise figure of 4.1 dB and the associate gain of 13.8 dB at 88 GHz. This MMIC amplifier shows wider 3-dB bandwidth and higher per-stage gain than others results at the similar band.

Key words: InAlAs/InGaAs/InP, pseudomorplic high electronic mobility transistor (PHEMTs), small-signal model, millimeter and submillimeter, monolithic millimeter-wave integrated circuit (MMIC), low noise amplifier (LNA)

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InAlAs/InGaAs/InP 基 PHEMTs 小信号建模及低噪声应用

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摘要:利用改进的小信号模型对采用 100 nm InAlAs/InGaAs/InP 工艺设计实现的 PHEMTs 器件进行建模,并设计实现了一款 W 波段单片低噪声放大器进行信号模型的验证。为了进一步改善信号模型低频 S 参数拟合差的精度,该小信号模型考虑了栅源和栅漏二极管微分电阻,在等效电路拓扑中分别用 R_{fs}和 R_{fd}表示. 为了验证模型的可行性,基于该信号模型研制了 W 波段低噪声放大器单片. 在片测试结果表明:最大小信号增益为 14.4 dB@92.5 GHz,3 dB 带宽为 25GHz@85-110 GHz. 而且,该放大器也表现出了良好的噪声特性,在 88 GHz 处噪声系数为 4.1 dB,相关增益为 13.8 dB. 与同频段其他芯片相比,该放大器单片具有宽3 dB 带宽和高的单级增益.

关 键 词:InAlAs/InGaAs/InP; 赝高电子迁移率晶体管(PHEMTs);小信号模型;毫米波和亚毫米波;单片微波集成电路(MMIC);低噪声放大器

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Introduction

In recent years, there has been an increasing demand for MMICs in the high millimeter/submillimeter-wave frequency regime[1-3]. The morphemic windows (94, 140, and 220 GHz) are of great interest for high-resolution imaging, remote atmospheric sensing, next

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generation automotive collision avoidance radars (140 GHz), environmental sensors (118/183 GHz), security detection of concealed weapons or explosives (220 GHz), broadband satellite communications and low noise detectors[4-9]. Due to the high sheet carrier density, high peak drift velocity, and high electron mobility, InP-based InAlAs/InGaAs HEMTs have demonstrated high operating frequency, low noise, as well as high gain performance[7, 10-11]. Therefore, the HEMTs are considered a unique candidate for those applications.

A physically meaningful small signal equivalent circuit is not only an important tool for circuit design, but also an important hint for device fabrication and improvement. To some extent, the model accuracy determines the success of the circuit design and shortens the circuit development cycle. Accurate device models become crucial to predict the circuit performance correctly.

In this paper, we present an improved small-signal equivalent circuit model, which consider differential resistances of gate-to-source and gate-to-drain diodes. The LNA, which is designed based on this small-signal model, is measured on-wafer with a small-signal peak gain of 14.4 dB at 92.5 GHz, 3-dB bandwidth is 25 GHz range from 85 to 110 GHz and the optimal noise figure is 4.1 dB at 88 GHz with a gain of 13.8 dB. The LNA has a great potential for receiver-front-end applications at W-band.

1 InP HEMT technology

A cross-sectional view of the InP PHEMT is shown in Fig. 1(a). The PHEMTs were grown by molecular beam epitaxy (MBE) on a 3-inch semi-insulating (100) InP wafers, Fig. 1 (b) shows the photo of the device. A typical room temperature Hall mobility of 11 000 $cm^2/(v\cdot s)$ and a Hall sheet carrier concentration charge of a 3.4E12 cm^{-2} were measured by Hall test. The process has demonstrated typical values for maximum oscillation frequency f_{max} = 384 GHz and current gain cutoff frequency f_T = 232 GHz, the maximum drain current is 863 mA/mm and peak gm is 1 182 mS/mm.

The backside of InP HEMT MMIC process provides a 50-μm-thick wafer for reduce the high frequency loss with through substrate vias, which connect the backside metal ground plane to the front side device and circuit elements. Additionally, 30 μm diameter through-substrate vias are used for minimizing source inductance and maintaining high device gain. The process further includes 50 Ω/sq NiCr thin film resistors (TFRs), 0.3 fF/μm^2 metal-insulator-metal (MIM) capacitors, and thru-substrate vias.

2 Equivalent circuits

Figure 2 shows the circuit topography of the small signal model. Normally, the small-signal equivalent circuit model of InP HEMTs include an intrinsic part (C_{gs}, C_{gd}, C_{ds}, R_{gd}, R_{ds}, R_i, R_{fs}, R_{fd}, tau, and g_m), whose elements are bias dependent, and an extrinsic part (R_g, R_s, R_d, L_s, L_g, L_d, C_{gsp}, C_{dgp}, and C_{dsp}), whose elements are independent of bias conditions[12-15]. The parasitic resistances (R_g, R_s, R_d) and inductances (L_s, L_g, L_d) associated with each contact and wire connection. The parasitic capacitances (C_{gsp}, C_{dgp}, C_{dsp}) are introduced by the pad connection or probe contacts[14-15].

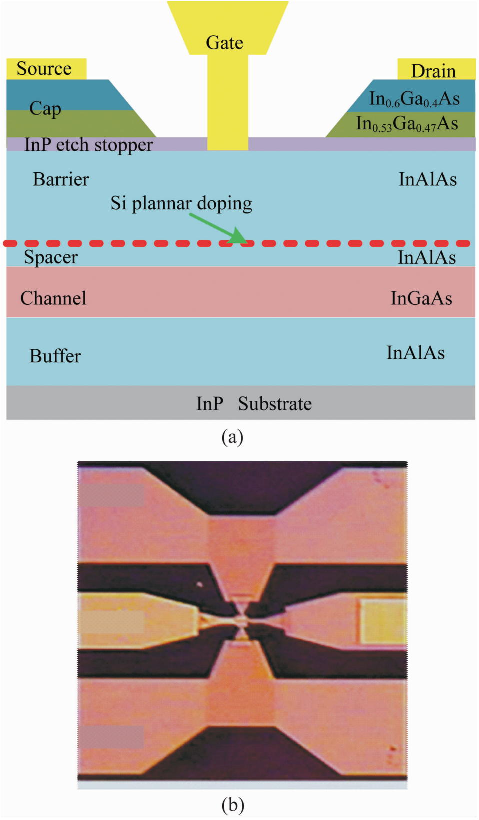

Fig. 1 (a) Schematic cross-sectional view of the InP-based PHEMT, (b) the photo of the device
图 1 (a) InP PHEMT 截面示意图, (b) 器件照片

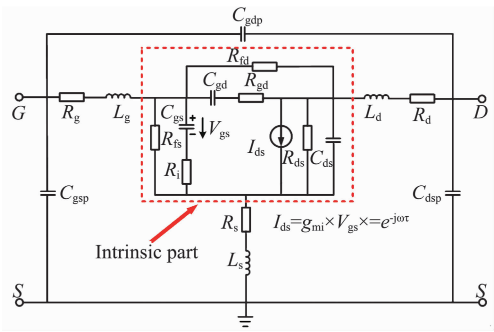

Fig. 2 Circuit topography for the small-signal model used for parameter extraction
图 2 器件小信号等效电路模型

The parasitic capacitances, resistances and inductances were extracted under a pinched-off "cold-FET" condition (V_{ds} = 0 V, V_{gs} = −1.2 V). As far as the extrinsic parasitic parameters are confirmed, the intrinsic circuit elements can be extracted from the S-parameters, which measured under the working bias conditions

(V_{gs} = −0.15 V, V_{ds} = 1.5 V).

After de-embedding the extrinsic components, the Y-parameters for the intrinsic part of the device can be express as following formula based on the topology:

$$Y_{int} = \begin{bmatrix} (j\omega c_{gd} \| R_{gd}^{-1}) + G_{fs} + G_{fd} + (j\omega c_{gs} \| R_i^{-1}) & G_{fd} - (j\omega c_{gd} \| R_{gd}^{-1}) \\ \dfrac{g_{mi} e^{-j\omega\tau}}{1 + j\omega c_{gs} R_i} - (j\omega c_{gd} \| R_{gd}^{-1}) - G_{fd} & G_{ds} + G_{fd} + j\omega c_{ds} + (j\omega c_{gd} \| R_{gd}^{-1}) \end{bmatrix}$$

A ∥ B = (A · B)/(A + B). The differential resistances of gate-to-source and gate-to-drain diodes are modeled by the resistances R_{fs} and R_{fd}, which can be determined at low frequencies. They are used for characterize the gate leakage current condition under the negative gate bias condition, which is significance for the device used in the high frequency. To ensure a smooth transition from symmetric "cold model" to operating points in the saturation region, the resistor R_{dg} is include.

The calculated S-parameters of the small signal model are compared with the measured values as shown in Fig. 3. The calculated S-parameters with R_{fs} and R_{fd} (red line) have better agreement with the measured S-parameters at low frequency.

Finally, the calculated extrinsic and intrinsic parameters for this device are listed in Table 1.

Table 1　The calculated small-signal equivalent circuit model parameters

表 1　小信号等效电路模型参数

Extrinsic parameters (Pads and cold-FET procedure)			Intrinsic parameters	
C_{pgd} = 2.55 fF	R_s = 1.2 Ω	L_s = 0.65 pH	g_{mi} = 134 mS	C_{gd} = 14.3 fF
C_{pgs} = 7.1 fF	R_d = 4.4 Ω	L_d = 28.6 pH	g_{ds} = 8.96 mS	C_{ds} = 18.2 fF
C_{pds} = 9.6 fF	R_g = 4.5 Ω	L_g = 34 pH	R_i = 2.1 Ω	C_{gs} = 72.1 fF
Parasitic capacitance	Parasitic resistance	Parasitic inductance	R_{gd} = 11.6 Ω R_{fs} = 20 kΩ	tau = 0.3 psec R_{fd} = 15 kΩ

The MMIC design will consider the influence of S_{21} more than S_{11}, S_{22}, and S_{12}, so we calculated the model S_{21} phase error and magnitude error, as shown in Fig. 4.

3　Model verification

A W-band LNA MMIC based on this model has been designed and fabricated. Figure 5 shows the circuit topology of the MMIC amplifier and Fig. 6 shows the photograph of the fabricated MMIC. Two stages were employed with dual source vias on each device in the MMIC, each stage uses a total gate-width of 2 × 40 μm InP PHEMT device. To prevent the excitation of parasitic modes in the substrate, the wafer was thinned down to 50 μm.

The MMIC was tested on-wafer using an Agilent N5245A PNA-X network analyzer with Farran Technology of series FEV-10 (75 ~ 110 GHz) frequency extenders. To measure noise figure, the W-band output signal was down-converted and measured by Agilent N8975A. Probe tip LRRM calibration was performed with Cascade Microtech calibration substrate. The reference plane was set at the probe pads of the MMIC. Figure 7 shows the building test system and on-wafer measurements are carried out at room temperature.

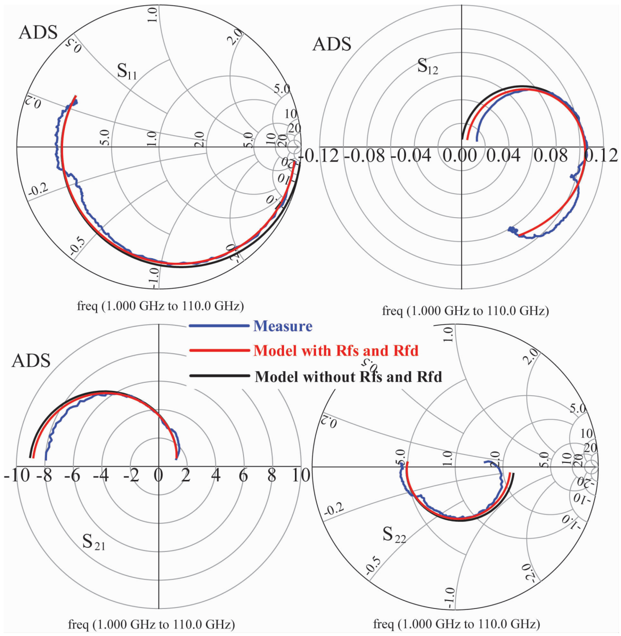

Fig. 3　Comparison of the S-parameters from measurement and simulation at bias of V_{gs} = −0.15 V and V_{ds} = 1.8 V

图 3　测试和建模 S 参数拟合曲线对比

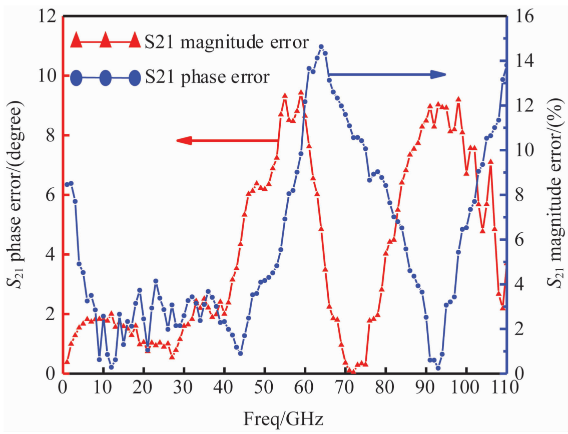

Fig. 4　The S_{21} errors of the model compared with the measured

图 4　模型与实测 S_{21} 幅度和相位误差对比

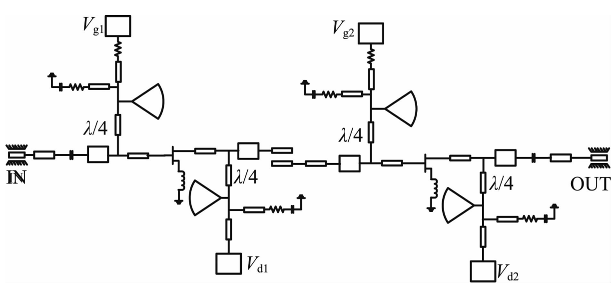

Fig. 5　The circuit topology of the MMIC amplifier

图 5　电路拓扑结构示意图

The on-wafer measured S-parameters are depicted in Fig. 8. A peak linear gain of approximately 14.4 dB was obtained at 92.5 GHz and greater than 11.4 dB from 85

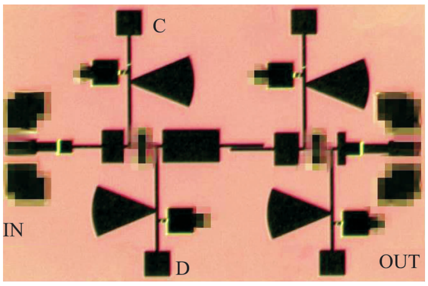

Fig. 6 Chip photograph of the two-stage MMIC amplifier
图 6 两级单片放大器实物照片

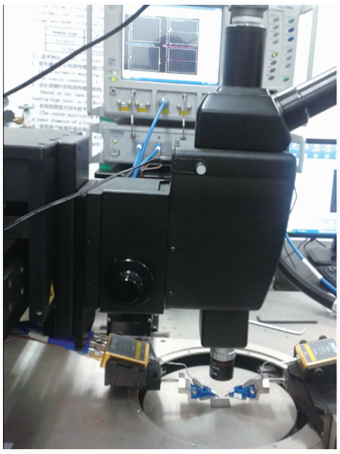

Fig. 7 Photograph of the test system
图 7 实际测试环境

to 110 GHz with input and output return loss greater than 5 dB over this band by applying a drain voltage of V_{ds} = 1.5 V. The total drain current at this bias point was I_d = 26.6 mA. Figure 9 shows the noise figure and associated gain of the LNA MMIC at room temperature. The optimal noise figure of 4.1 dB with associated gain of 13.8 dB at 88 GHz.

The excellent performance of the amplifier benefits from our improved common source InP PHEMT device with high maximum oscillation frequency and the optimized backside process. The input and output return loss is not ideal, because the MMIC amplifiers are measured on-wafer that may lead to self-excitation and mismatch. The reason for S_{21} discrepancy between the measured and simulated results can be attributed to the model errors, as shown in Fig. 4. Therefore, we should make a tradeoff

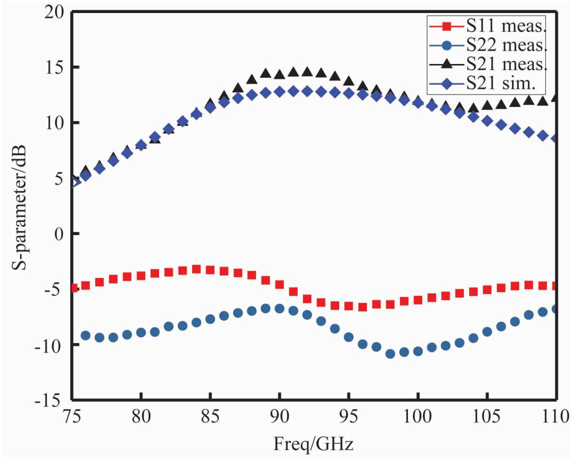

Fig. 8 On-wafer measured S-parameters
图 8 在片测试所得 S 参数

between the model precision and bandwidth.

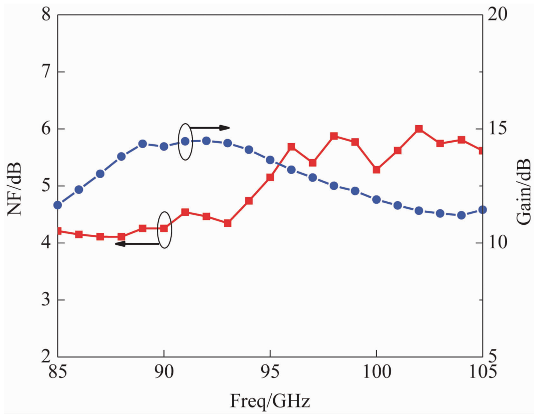

Fig. 9 Noise figure and associated gain of the LNA MMIC
图 9 LNA MMIC 的噪声系数及相关增益

The comparison of this work with previously published amplifiers at W-band are shown in Table 2. Our W-band MMIC amplifier exhibits wider 3-dB bandwidth, higher gain per stage and a better noise figure.

4 Conclusion

This paper presents an improved small signal model that considers the differential resistances of gate-to-source

Table 2 Performance summary of amplifiers at W-band
表 2 W 波段放大器性能对比

Ref.	Technology	Freq /GHz	Topology	Gain/stage/dB	3 dB BW/GHz	NF/dB	Associated gain/dB
[8]	100 nm HEMT	80 ~ 100	5-stg CS	6	20	1.9	30
[9]	70 nm MHEMT	80 ~ 100	3-stg CS	6.7	20	2.5	20
[10]	100 nm MHEMT	95 ~ 100	4-stg CS	5	5	–	–
[16]	100 nm PHEMT	85 ~ 99.6	3-stg CS	4.8	14.6	5.5	22
[17]	100 nm PHEMT	80 ~ 94	2-stg CS	> 5.5	14	5	11
[18]	150 nm HEMT	84 ~ 100	1-stg CC	> 10	16	4.3	12
This work	100 nm PHEMT	85 ~ 110	2-stg CS	7.2	25	4.1	13.8

and gate-to-drain diodes. The results of the model exhibit good agreement with the experimental data. In order to verify the accuracy of the model, we designed and fabricated a W band LNA MMIC based on this model. The two-stage amplifier is measured on-wafer with a small-signal peak gain of 14.4 dB at 92.5 GHz. In 85 ~ 110 GHz frequency range, the small signal gain is greater than 11.5 dB. The LNA also exhibits an excellent noise characteristics with an optimal noise figure of 4.1 dB and associated gain of 13.8 dB at 88 GHz. For future improve in LNA, methods such as increasing InAs content, shortening gate length and optimizing ohmic contact can be used.

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