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Pd/Ti/Pt/Au alloyed ohmic contact for InAs/AlSb heterostructures with the undoped InAs cap layer

ZHANG Jing[1,2], LYU Hong-Liang[1*], NI Hai-Qiao[2], NIU Zhi-Chuan[2], ZHANG Yi-Men[1], ZHANG Yu-Ming[1]

(1. School of Microelectronics, Xidian University and Key Laboratory of Wide Band-Gap Semiconductor Materials and Devices, Xi'an 710071, China;
2. State Key Laboratory for Superlattices and Microstructures, Institute of Semiconductors, Chinese Academy of Sciences, Beijing 100083, China)

Abstract: In order to achieve low contact resistances of InAs/AlSb heterostructures with the undoped InAs cap layer, Pd/Ti/Pt/Au alloyed ohmic contact has been investigated. The contact resistance R_c is evaluated by using transmission-line-model (TLM) measurements. A minimum of 0.128 Ω·mm has been obtained by using the optimal rapid thermal annealing (RTA) with the condition at temperature of 275 °C and annealing time of 20 s. The measurement from transmission electron microscopy (TEM) demonstrates that the Pd atoms diffuses into the semiconductor, which is beneficial to the formation of a high-quality ohmic contact during the rapid thermal annealing. This study shows that the contact resistance R_c is reduced significantly after Pd/Ti/Pt/Au alloyed ohmic contact, which is suitable for its application in InAs/AlSb heterostructures.

Key words: Ohmic contacts, rapid thermal annealing, InAs/AlSb heterostructures
PACS: 81.05.Bx, 81.05.Ea, 82.45.Vp

InAs/AlSb 异质结的 Pd/Ti/Pt/Au 合金化欧姆接触

张 静[1,2], 吕红亮[1*], 倪海桥[2], 牛智川[2], 张义门[1], 张玉明[1]
(1. 西安电子科技大学 宽带隙半导体技术国家重点学科实验室,陕西 西安 710071;
2. 中国科学院半导体研究所,超晶格国家重点实验室,北京 100083)

摘要:为了得到较低的接触电阻,研究了帽层未掺杂的 InAs/AlSb 异质结的 Pd/Ti/Pt/Au 合金化欧姆接触.利用传输线模型(TLM)测量了接触电阻 R_c.在最佳的快速热退火条件为 275 °C 和 20 s 时,InAs/AlSb 异质结的 Pd/Ti/Pt/Au 接触电阻值为 0.128 Ω·mm. TEM 观察发现经过快速热退火后 Pd 已经扩散到半导体中有利于高质量欧姆接触的形成.研究表明经过 Pd/Ti/Pt/Au 合金化欧姆接触后 R_c 有明显减小,适用于 InAs/AlSb 异质结的应用.

关 键 词:欧姆接触;快速热退火;InAs/AlSb 异质结
中图分类号:TN304.2,TN305 **文献标识码**:A

Introduction

The InAs/AlSb high electron mobility transistor (HEMT) is a promising candidate device for microwave/millimeter-wave circuits because of a large conduction band offset between InAs and AlSb, high peak electron velocity, and high sheet electron density in the InAs channel [1-2]. The fabrication process has been initially developed from a previous first generation of InAs/AlSb HEMT reported in Refs. 3-5, in which the process is based on five main processing steps, ohmic contact formation, electrical isolation, gate metal electrode deposition, probing pad metallization and passivation.

Ohmic contact formation is the first key step of the process[6-7], because the parasitic resistance plays an im-

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Biography: ZHANG Jing (1988-), female, Shaanxi, China, Ph. D. candidate. Research area involves Semiconductor materials and devices. E-mail: zhangjing6048@126.com
* **Corresponding author**: E-mail: hllv@mail.xidian.edu.cn

portant role in influencing the frequency characteristics of InAs/AlSb HEMT. The parasitic resistance is mainly composed of the contact resistance in the source/drain for the nanoscale device. Thus, the realization of low ohmic contact resistance is crucial to improving the performance of HEMT.

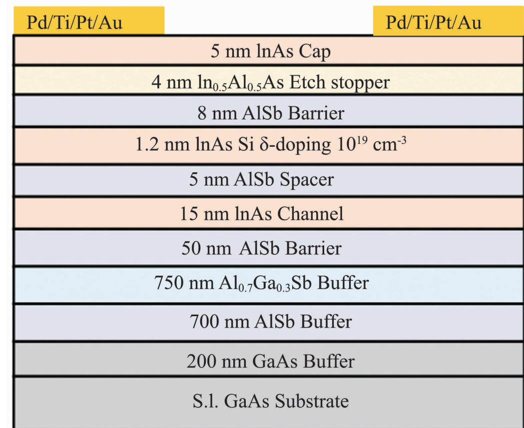
In the early fabrication process of the HEMT device, the gate-recess etch is the second key process step performed by dry etching or wet etching to avoid the gate-to-source and gate-to-drain leakage through the highly doped InAs cap layer[8]. However, the dry etching introduces damage and leads to increasing of the leakage current. Furthermore, the corrosion time of the wet etching needs to be controlled accurately to selectively stop the etching on the InAlAs protection layer. Although the highly doped InAs cap layer is a conventional structure to improve the ohmic contact quality, the subsequent etching process improves the difficulty and cost of the fabrication as well. As for the undoped InAs cap layer structure, the leakage and the gate-recess etching are not necessary any longer, but more effort is needed to achieve high ohmic contact quality, especially the low contact resistance R_c.

In this paper, the undoped InAs cap layer and Pd/Ti/Pt/Au alloyed ohmic contact are used for InAs/AlSb heterostructures. The contact resistance R_c is evaluated by using conventional two-point-probe transmission-line-model (TLM) measurements. Low ohmic contact resistance has been achieved by optimal rapid thermal annealing (RTA) for the Pd/Ti/Pt/Au contacts to InAs/AlSb heterostructures.

1 Experimental procedures

All contacts were prepared on an InAs/AlSb heterostructures depicted in Fig. 1 (a) and the energy band diagram is illustrated in Fig. 1 (b). The epitaxial materials were grown by molecular beam epitaxy (MBE) on 2-in semi-insulating GaAs substrates. A composite AlSb/$Al_{0.7}Ga_{0.3}Sb$ metamorphic buffer layer with a thickness of 1.45 μm was utilized to relax the 8% compressive lattice mismatch between the GaAs substrate and the device active layers. The AlSb metamorphic buffer layer ensures a high electrical resistivity but suffers from strong oxidation in air and moisture, however, the top $Al_{0.7}Ga_{0.3}Sb$ layer is far more stable in ambient[9-11]. The HEMT active layers above the metamorphic buffer layers consist of a 50 nm AlSb HEMT buffer layer, a 15 nm InAs channel, a 5 nm AlSb spacer, a Si δ-doping plane inserted in four monolayers of InAs (~1.2 nm), and an 8-nm AlSb Schottky layer. On the top, there are a 4 nm $In_{0.5}Al_{0.5}As$ protection layer and a 5 nm undoped InAs contact layer. Meanwhile, a compared sample in the InAs contact layer with heavily Si-doped also is prepared. A single-layer method was used to calibrate the carrier concentration of 3.5×10^{16} cm^{-3} for the undoped InAs layer and 5×10^{18} cm^{-3} for the Si-doped InAs cap layer.

Hall measurements were performed on 1 cm × 1 cm pieces at 300 K and the results show an electron mobility of 18 730 $cm^2/V\cdot s$ and a sheet electron density of 1.21×10^{12} cm^{-2}. Figure 2 shows the morphology of InAs cap surface after material growth is done. The root-mean-square roughness measured on the as-grown surface by AFM is 1.269 nm. The two different InAs/AlSb heterostructures have similar results.



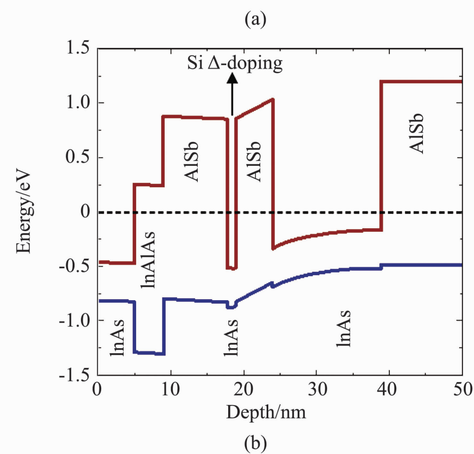


Fig. 1 (a) Schematic InAs/AlSb heterostructure, (b) the energy band diagram
图 1 (a) InAs/AlSb 异质结示意图,(b)能带图

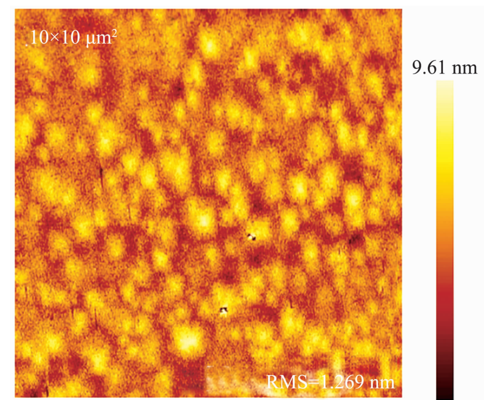


Fig. 2 AFM image of InAs cap surface
图 2 InAs 帽层表面 AFM 图

The standard photolithographic technique was used to define TLM patterns with nominal gap spacings of 4, 6, 8, 16 and 32 μm, as shown in Fig. 3. Prior to depo-

sition, the semiconductor surface was treated with a HCl-based solution for 15 s to minimize surface oxides, followed by a deionized water rinse and N_2 blow drying. The Pd/Ti/Pt/Au (20 nm /30 nm /30 nm /30 nm) deposition was then implemented by electron-beam evaporation. Samples were annealed by using RTA in a N_2 ambient at a temperature ranging from 275℃ to 325℃ for 10 to 30 s.

Following the heat treatment, the contacts were redefined by a mesa etching to completely remove the active layers down to the $Al_{0.7}Ga_{0.3}Sb$ metamorphic buffer layer and isolate the TLM pattern from the surrounding area. This process was performed by ICP dry etching with $Ar/Cl_2/CH_4$ (8.5/4.5/11.7 sccm). The RF power, ICP power and chamber pressure are 30 W, 400 W and 3.9 mToor, respectively. After etching for 1 min, the depth is 147 nm, measured by KLA Tencor Profiler. Then, a sidewall etching was carried out using citric acid/H_2O_2 solution to avoid gate-to-channel conduction at mesa edge.

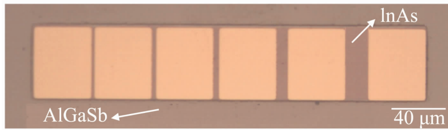


Fig. 3　Optical image of TLM pattern
图 3　TLM 图案的光学图片

A test pattern was designed to measure the currents for the comparison between two contacts before and after mesa isolation and the results were shown in Fig. 4. The distance between two contacts is 14 μm and the size of contact metal is 100 μm × 100 μm. According to Fig. 4, acceptable device isolation is achieved by adopting this shallow mesa isolation.

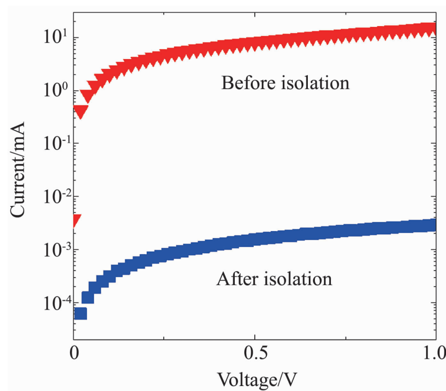


Fig. 4　*I-V* curves of two contacts before and after mesa isolation
图 4　台面隔离前后的 *I-V* 曲线

2　Results and discussion

TLM is often used to extract the contact resistance R_c and the specific ohmic contact resistance ρ_c to evaluate the quality of the ohmic contact[12-14]. The optical image of TLM pattern is shown in Fig. 3, which consists of several metal contacts of the same width W and length L, and the distance d_n between adjacent contact metals is increasing. In addition, the test structure also requires mesa isolation to ensure that the current flow through the area between the two ohmic contacts.

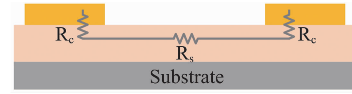


Fig. 5　The equivalent model of total resistance (R_{tot})
图 5　总电阻 R_{tot} 的等效模型

The equivalent model of the total resistance R_{tot} is shown in Fig. 5, where R_c is the ohmic contact resistance and R_s is the bulk resistance of the semiconductor between the two contact metals. R_{tot} is a function of d_n.

Here $$R_s = R_{sh}\frac{d_n}{W} \quad . \quad (1)$$

According to Fig. 5, R_{tot} between any two contacts is given by Eq. 2

$$R_{tot} = 2R_c + R_{sh}\frac{d_n}{W} \quad . \quad (2)$$

From Eq. 2, R_{tot} is a linear function of d_n. The slope of the fitting straight line is R_{sh}/W and the intersection of the vertical axis is $2R_c$.

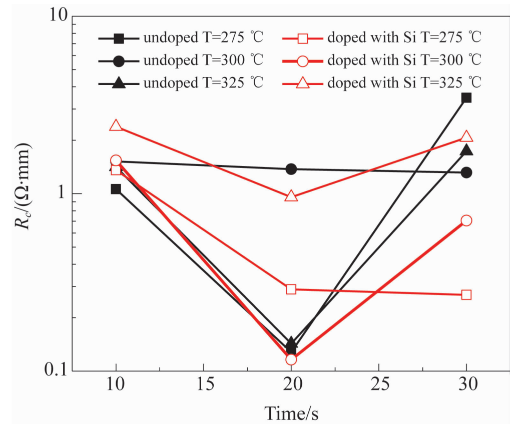


Fig. 6　The contact resistance R_c versus annealing time and temperature
图 6　接触电阻 R_c 与退火时间及温度的关系曲线

Figure 6 shows the contact resistance R_c for the Pd/Ti/Pt/Au contacts as a function of annealing time, in which contact resistance values decrease with the increasing annealing time up to 20 s and then increase. The contact resistance reaches a minimum of 0.116 Ω · mm at 300°C for the Si-doped InAs cap layer as the annealing time is 20 s. The ohmic contact can be formed due to the fact that the electrons are easier to penetrate the thinner barrier region which can be obtained by the heavily Si-doped InAs.

In this work, InAs/AlSb heterostructure with the undoped InAs cap layer is used to avoid the gate-recess

etching. Figure 6 shows the contact resistance reaches a minimum of 0.128 Ω · mm at 275°C for the undoped InAs cap layer as the annealing time is 20 s. Contact resistance value of 0.128 Ω · mm is close to the value of Si-doped InAs cap layer, which is acceptable for device operation.

Here, several methods used in this work to form ohmic contact:

(1) A narrow-band (E_g = 0.36 eV) InAs material is used to reduce the barrier height of the metal and contact layer.

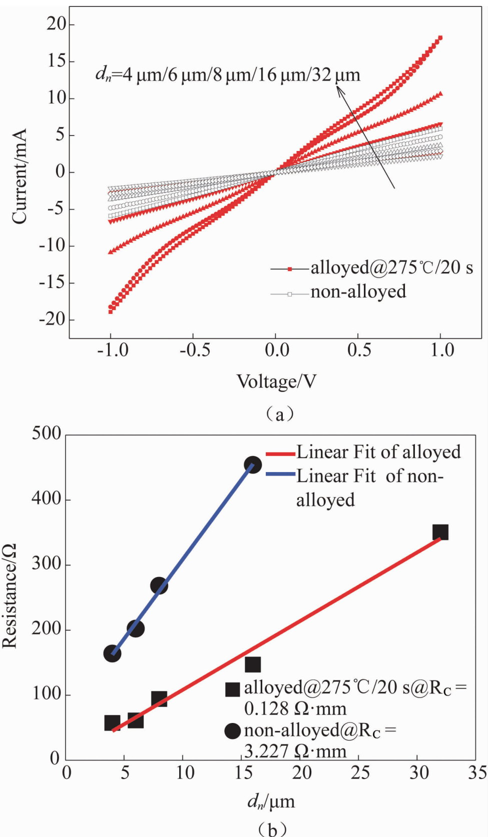


Fig. 7 (a) *I-V* curves of two contacts with different d_n, (b) R_{tot} versus d_n

图 7 (a)不同间距 d_n 的 *I-V* 曲线,(b)总电阻 R_{tot} 与不同间距 d_n 的关系曲线

(2) It is more suitable to choose alloying ohmic contact due to there is a barrier layer above the channel for InAs/AlSb heterostructure. The *I-V* curves versus different d_n for different samples and R_{tot} as a function of d_n are shown in Fig. 7 (a) and (b). It can be seen from Fig. 7 (a) that the electrical characteristics of the metal and semiconductor interface are changed significantly after RTA. As shown in Figure 7 (b), the contact resistance R_c for the non-alloyed sample is 3.277 Ω · mm, and it has significantly reduced to 0.128 Ω · mm after RTA.

(3) Compared with the common Ti/Pt/Au contacts to InAs/AlSb heterostructures, the Pd contacts to InAs/AlSb heterostructures using Ti as an adhesion layer, Pt as a diffusion barrier and Au as a capping layer shows that Pd/Ti/Pt/Au contacts exhibit low contact resistance and excellent morphology[15]. Figure 8 is a TEM image of a Pd/Ti/Pt/Au contact annealed at 275°C for 20 s. The TEM image shows that Pd has diffused into InAs channel layer due to Pd has a stronger penetration capacity to form a reacted region than Ti in III-V compound semiconductors which is beneficial to high-quality ohmic contact[7,15]. The stronger penetration capacity of Pd is attributed to the desirable features, such as easy penetration and displacement of the native oxide layer on the semiconductor and the formation of metastable ternary reaction products at the proper temperature for narrow-bandgap semiconductor processing.

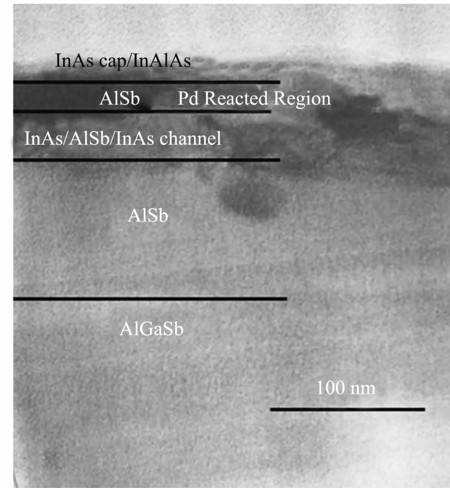


Fig. 8 TEM image of Pd/Ti/Pt/Au ohmic contact

图 8 Pd/Ti/Pt/Au 欧姆接触的 TEM 图

3 Conclusion

Pd/Ti/Pt/Au alloyed ohmic contact has been investigated for InAs/AlSb heterostructures with an undoped InAs cap layer. The gate-recess etching can be avoided and lower contact resistance of 0.128 Ω · mm has to be achieved with the optimal rapid thermal annealing condition at temperature of 275°C and annealing time of 20 s. The image from transmission electron microscopy demonstrates that the Pd has diffused into the semiconductor to form a reacted region to be beneficial to the formation of a high-quality ohmic contact, so it is suitable for the application in InAs/AlSb heterostructures.

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