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Minimization design of guard ring size of p- well/DNW single photon avalanche diode

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Abstract: In order to further diminish the size of SPAD detector, the guard ring size of p-well/DNW (deep n-well) SPAD was designed based on a 0.18 μm CMOS Image Sensor (CIS) technology and SPADs of varied guard ring sizes were fabricated. The measured results show that, the guard ring with its size decreased to 0.4 μm is still effective in preventing premature edge breakdown (PEB), and the guard ring size does not have a significant impact on the dark count rate (DCR) and the photon detection probability (PDP) of p-well/DNW SPADs. The SPADs achieve a low DCR and a broad spectral response, and the DCR is 638 Hz at 25℃ with a PDP peak of 16% at 530 nm for 20 μm diameter active area structure.

Key words: single photon avalanche diode (SPAD), guard ring, premature edge breakdown (PEB), dark count rate (DCR), photon detection probability (PDP)
PACS: 85.60.Bt, 85.60.Dw, 85.30.-z.

p- well/DNW 单光子雪崩二极管保护环的最小化设计

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摘要: 为了进一步缩小 SPAD 探测器的尺寸, 基于 0.18 μm CMOS 图像传感器(CIS)工艺对 p-well/DNW(deep n-well) SPAD 的保护环尺寸进行设计, 并制造了不同保护环尺寸的 SPAD 器件. 测试结果表明, 保护环尺寸减小到 0.4 μm 仍然能有效防止器件发生过早边缘击穿(PEB), 且保护环尺寸对 p-well/DNW SPAD 器件的暗计数率(DCR)和光子探测概率(PDP)影响较小. 直径为 20 μm 的 SPAD 器件, 温度为 25℃ 时暗计数率为 638 Hz, 且波长为 530 nm 时峰值光子探测概率为 16%, 具有低的暗计数率特性和宽的光谱响应特性.

关 键 词: 单光子雪崩二极管(*SPAD*); 保护环; 边缘击穿(*PEB*); 暗计数率(*DCR*); 光子探测概率(*PDP*)

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Introduction

Single photon avalanche diodes (SPADs) are reversely biased PN junctions, whose bias voltage is larger than their breakdown voltage. Because of the large bias voltage, the electric field of the depletion region is high enough for making a single carrier trigger a self-maintained avalanche through impact ionization, thus generating a high current pulse. If the carrier is generated by photon absorption, the current pulse detected by the associated electronic circuitry will signify the detection of the photon. Due to their single-photon sensitivity and high timing resolution, SPADs are widely used for low flux and high speed photon detection such as positron emission tomography (PET), fluorescent lifetime imaging (FLIM), fluorescence correlation spectroscopy (FCS), as well as 3D optical ranging [1].

SPADs implemented in standard CMOS technology can be integrated together with on-chip readout and sig-

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nal processing circuits, resulting in a monolithic large array with thousands of pixels. This opens the way to realize a fully integrated, low-cost and high-performance system for high-sensitivity imaging [2]. Therefore, CMOS SPADs are arousing great interest in many single photon detection applications, in which accurate measurement of photon arrival times is required [2-3]. In particular, SPAD arrays with integrated readout circuits aimed at 3D imaging application were reported [4-5].

The earliest design of CMOS SPADs appeared in 2003 [6], and then many groups worldwide developed various SPAD structures at different CMOS technology nodes for coping with premature edge breakdown (PEB), electric field uniformity, tunneling effects, wide depleted region thickness and so on [7-11]. Imaging application requires high-density SPAD arrays integrated with in-pixel electronics, hence pixel pitch does play an important role in the design of CMOS SPAD arrays.

In order to decrease the pixel pitch, there are two ways to be used. One is to reduce the area occupied by the integrated electronics using simple quenching and readout circuits instead of complex ones [12], the other is to decrease the size of the SPAD by improving its structure. As CMOS technology scales down, the area occupied by the integrated electronics is promptly reduced, resulting in the reduction of CMOS SPAD arrays [13]. Nevertheless, the size of the SPAD itself impedes the further scaling down of CMOS SPAD arrays. Therefore, the integration of small size pixels and low dark count rate (DCR), high photon detection efficiency (PDE) SPADs arouses widespread concern [10].

The smallest SPAD device with a 2-μm active diameter was reported using shallow trench isolation (STI) guard ring, but the DCR was extremely high (about 100 kHz) [14]. The p+/n-well SPAD with a traditional p-well guard ring cannot be scaled down much below 5 μm because of the expansion of the depletion regions around the p-well implants [8]. Especially in deep sub-micrometer CMOS technology, the depletion region of SPAD designed using p+/n-well junction becomes narrow due to high n-well doping concentration, resulting in a high dark noise by tunneling with reduced PDE [14-15]. Richardson et al. presented a novel design in 2009 [16] and later extensively discussed it in 2010 [17]. This new design, which was implemented in a 130-nm CMOS technology, is formed by lightly doped p-well and deep n-well (DNW) layers, with a virtual guard ring formed by a retrograde profile. Because of the lower doping concentrations, the depletion region of this device is wider than that of the traditional p+/n-well SPAD, so as to reduce the tunneling noise and broad the spectral response toward the longer wavelength region with high PDE [16]. In particular, this SPAD device can be scaled down to a 2-μm active diameter with a low DCR of about 9 Hz, which is a strong candidate for single photon detection applications requiring high spatial and temporal resolution [17].

In order to further scale down the SPAD device reported in Ref. [17], SPADs with different guard ring sizes are achieved in a 0.18 μm CMOS image sensor (CIS) technology. The rest part of this thesis is organized as follows: the device structure and simulation results are presented in Sect. 1, the experimental results and discussion are shown in Sect. 2, and the conclusion is given in Sect. 3.

1 SPAD structure and simulation results

The circular device cross section of p-well/DNW SPAD is shown in Fig. 1. The structure of this device was detailed in Refs. [16-17]. The active area is formed by a lightly doped p-well in conjunction with a retrograde DNW, which makes doping concentration increase from a low level at the surface to a high level deeper into the wafer. The DNW is connected to the n+ cathode through n-well. The p-well and n-well are designed with a gap in between by blocking peripheral p-well formation, and the gap length is marked with D. Therefore, the p-well is surrounded by the DNW, which causes the region around the periphery of p-well to be effective n-, thus forming a virtual 3D guard ring to avoid PEB. In addition, in order to minimize the DCR of this device, STI is avoided near the multiplication region to prevent the electron generation from interface traps.

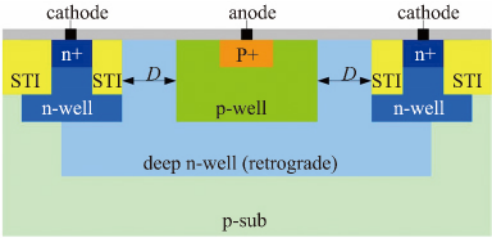

Fig. 1 Schematic cross section of the p-well/DNW SPAD
图1 p-well/DNW SPAD **结构图**

As is shown in Fig. 1, the decrease of the gap length D will reduce the size of the detector, accordingly scaling down the SPAD array and improving the fill factor of imaging system [17]. But excessive shrinking of the gap can lead to PEB, and the retrograde DNW cannot work as a guard ring, because the n- density around p-well edge becomes large enough due to the lateral diffusion of n-well. Therefore, this structure has to be optimized to obtain the minimum guard ring size. For this purpose, SPADs with different gap lengths are being studied.

To evaluate the smallest value of the gap length D, 2D process and device simulations were performed using Silvaco TCAD. Device structures were defined by Athena, and device simulations were done using Silvaco's Atlas device simulator based on the structure implemented above. When the device was being simulated, the output current was measured at the cathode, while the anode and the substrate were connected to the ground.

Several devices with different diameters and varied gap lengths were simulated. The simulation results show that the devices with different diameters and the same gap lengths have the same reverse I-V characteristics because of the same impurity concentration distribution in the devices. Therefore, only the simulated reverse I-V characteristics of SPADs with varied gap lengths are shown in Fig. 2. It indicates that the breakdown voltage of devices with gap lengths $D \leqslant 0.2$ μm is smaller than

that of devices with gap lengths larger than 0.2 μm (whose breakdown voltage is about 16 V). This implies that PEB occurs when the gap length D decreases to 0.2 μm.

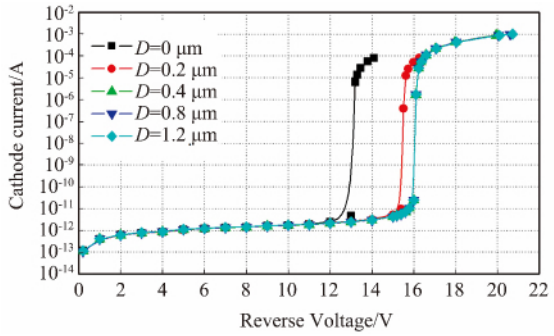

Fig. 2　Simulated reverse *I-V* characteristics of SPADs with different gap lengths

图 2　不同间隙长度 SPAD 的反向 *I-V* 特性仿真结果

The electric field distributions at breakdown of SPADs with diameters of 20 μm, 10 μm, and 2 μm for D = 0.4 μm and D = 0.2 μm are plotted in Figs. 3(a-f), respectively. Figures 3(a-c) display that the high field region (orange) is localized uniformly at the center region where p-well overlaps DNW, and there is a natural reduction from medium (green) to low (blue) at the edge of the active region. This indicates that the guard ring is efficient for preventing the SPAD from PEB when D = 0.4 μm. Figures 3 (d-f) show that the high field region (orange) is localized at the side junction of the device, indicating the ineffectiveness of the guard ring when D = 0.2 μm.

In order to better characterize the SPADs and determine the exact breakdown location, the current density in the SPADs were simulated under 16-V reverse bias voltage. This bias is just to let SPAD break down, so the breakdown spot can be determined from the breakdown current flow. Figures 4 (a-c) show the current density simulation results when the gap length D is 0.4 μm. It can be observed that the current flows through the center of the junction, which clearly manifests that the spontaneous avalanche breakdown occurs at the center of the active area, where the electric field strength is highest. From Figures 4 (d-f), one can see that when D = 0.2 μm, the breakdown happens at the side junction of the SPAD.

The above experimental results show that, because the distribution of impurity concentration of the guard ring is the same, the minimum guard ring size of SPAD devices with different diameters is also the same, and its value is 0.4 μm.

2　Experimental results and discussion

In order to find the minimum gap length in a 0.18 μm CIS technology, four SPADs with different gap lengths were designed. Figure 5 shows the micrograph of the fabricated SPADs, whose active diameters are all 20 μm, while the gap length D has four different values: 1.2 μm, 0.8 μm, 0.4 μm and 0.2 μm.

The reverse *I-V* characteristics of the SPAD designs were measured using Keithley source meter (Keithley 6517), and are plotted in logarithmic scale in Fig. 6. One can see that, the breakdown voltage of the 0.2 μm gap SPAD is smaller than that of the remaining three devices, which show an avalanche around a measured reverse bias voltage of 16 V with a dark current less than 1 nA. It implies that, the 0.2 μm gap SPAD is not func-

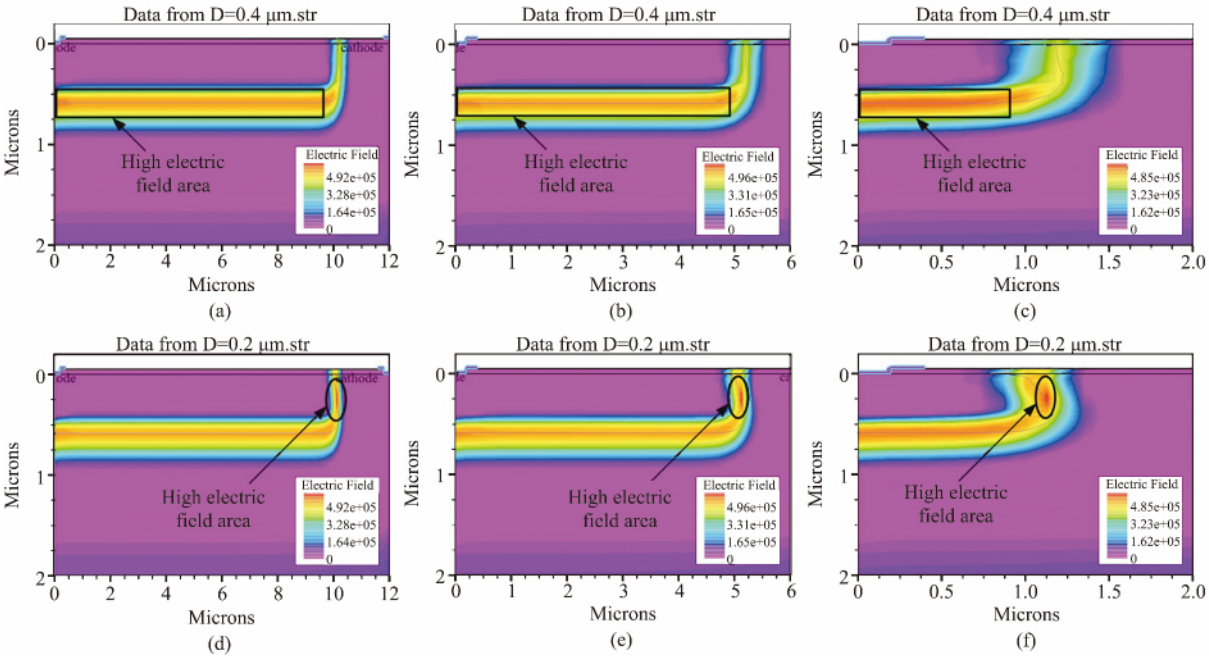

Fig. 3　Simulation results of electric field for devices with diameters of 20 μm, 10 μm, 2 μm, respectively (a-c) when D = 0.4 μm, (d-f) when D = 0.2 μm

图 3　直径分别为 20 μm, 10 μm, 2 μm 器件的电场强度仿真结果 (a-c) D = 0.4 μm, (d-f) D = 0.2 μm

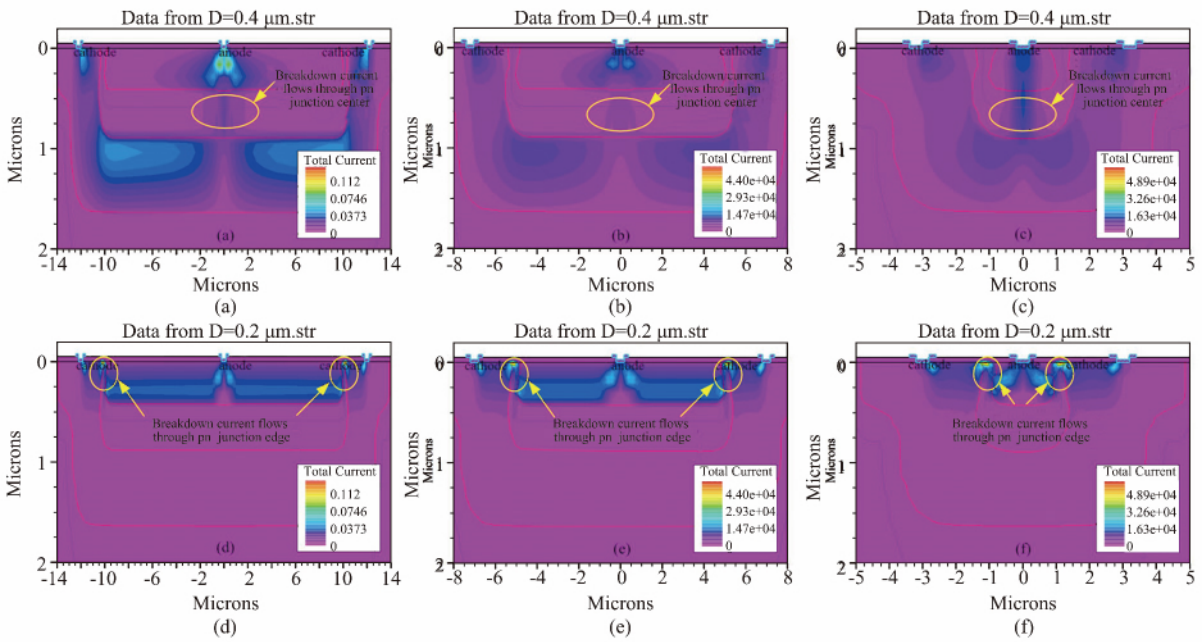

Fig. 4 Simulation results of total current density for devices with diameters of 20 μm, 10 μm, 2 μm, respectively (a-c) when D = 0.4 μm, (d-f) when D = 0.2 μm

图4 直径分别为20 μm, 10 μm, 2 μm器件的总电流密度仿真结果 (a-c) D = 0.4 μm, (d-f) D = 0.2 μm

Fig. 5 Micrograph of SPADs fabricated in a 0.18 μm CIS technology

图5 基于0.18 μm图像传感器工艺的SPAD显微照片

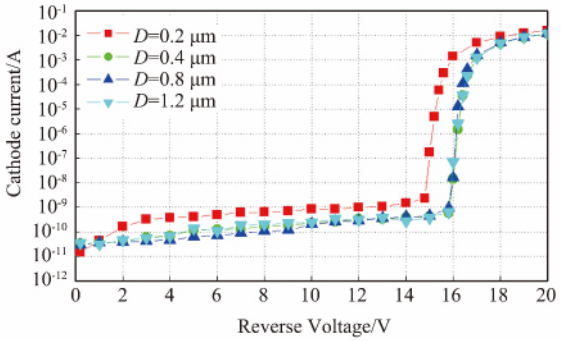

Fig. 6 Measured reverse I-V characteristics of SPADs with varied gap lengths

图6 不同间隙长度SPAD的反向I-V特性曲线测试结果

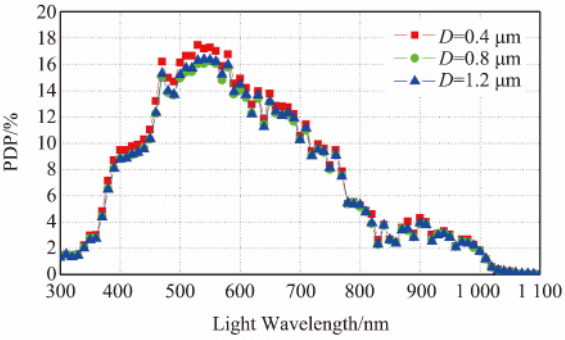

Fig. 7 Measured PDP of SPADs with varied gap lengths

图7 不同间隙长度SPAD的光子探测概率测试结果

tional, but the gap with its size decreased to 0.4 μm can still effectively work as a guard ring. That's to say, the gap length of this SPAD in the 0.18 μm CIS technology can be scaled down to 0.4 μm.

The photon detection probability (PDP), which represents the ratio of the number of detected photons over the number of incident photons, was measured over a wavelength range from 300 nm to 1 100 nm at room temperature with an excess bias voltage of 500 mV, and it is shown in Fig. 7. It is found that, the size of the guard ring has no great influence on the PDP. The typical PDP of 16% is less than that reported in Ref. [9], but it presents a broader spectral response shifted toward the longer wavelength region with a peak value wavelength around 530 nm, larger than that of p+/n-well junction, which peaks at 430 nm [9].

DCR measurement was achieved by counting the number of avalanche pulses when the SPAD was biased above its breakdown voltage in complete darkness. A passive quenching was chosen to measure the DCR of SPADs in this paper. The schematic of the test circuit is shown in Fig. 8. The cathode of SPAD is connected to a

voltage source V_A through a high-value quenching resistance R_Q, thus the excess bias voltage $V_{ex} = V_A - V_{BD}$, where V_{BD} is the breakdown voltage. The high-value quenching resistance R_Q is usually tens of kΩ (20 kΩ in this paper), the little sensing resistance R_S connected with the anode is set to be 50 Ω, and the substrate of SPAD is connected to the ground. The signal sensed by R_S is amplified by the amplifier first, and then compared with a reference voltage, and finally connected to a high performance oscilloscope (OSC) to count DCR.

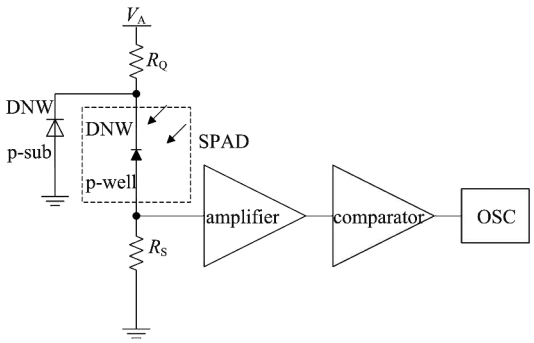

Fig. 8　Schematic of the measurement circuit of SPAD devices

图 8　SPAD 器件的测试电路图

Figure 9 shows the measured DCR as a function of the excess bias voltage V_{ex} (ranging from 0.5 V to 5 V with a 0.5 V step) at room temperature. We can see that, the DCR seems to increase linearly with the increase of V_{ex} because of the increasing avalanche breakdown probability and tunneling carrier generation. On the other hand, the DCR does not show a significant difference with different gap lengths at the same excess bias voltage, because the dark carriers generated in the side junction cannot trigger avalanche due to the low electric field caused by the guard ring. When V_{ex} increases from 0.5 V to 5 V, the typical DCR varies from 0.52 kHz to 3.02 kHz, showing a lower DCR/area value than that reported in Ref. [17].

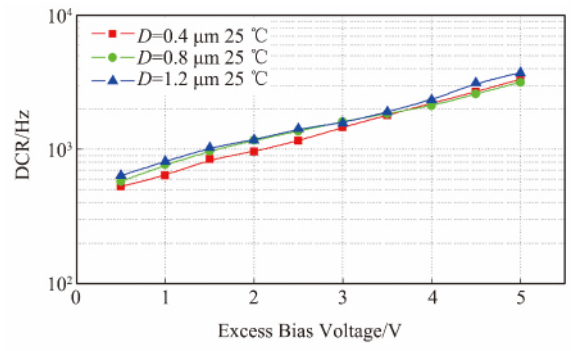

Fig. 9　DCR of SPADs at different excess bias voltages

图 9　不同过偏置电压时 SPAD 的 DCR 特性

The DCR of SPAD at different temperatures when V_{ex} remains at 1.0 V is shown in Fig. 10. The typical DCR increases from 0.14 kHz to 3.01 kHz with the temperature varying from 0℃ to 60℃, and it is lower than that reported in Ref. [9]. This is mainly due to Shockley Read Hall (SRH) thermal generation. At the same time, the band-to-band tunneling effect also contributes to this phenomenon [10, 17]. Therefore, it is quite indispensable to make SPAD present acceptable levels of DCR in practical applications [10].

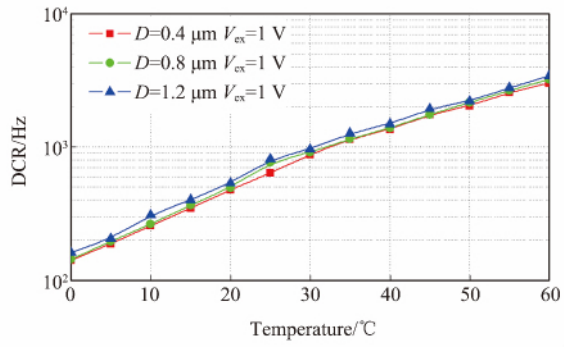

Fig. 10　DCR of SPADs at different temperatures

图 10　不同温度时 SPAD 的 DCR 特性

3　Conclusion

In this paper, the p-well/DNW single photon avalanche diode (SPAD) implemented in a 0.18 μm CMOS Image Sensor (CIS) technology has been designed, fabricated and tested. Four SPADs with different gap lengths were designed to demonstrate the successful scaling down of the guard ring. The guard ring can be decreased to 0.4 μm to make SPAD operate in Geiger mode to implement photon detection, and there is no significant impact on the dark count rate (DCR) and the photon detection probability (PDP) of p-well/DNW SPADs. Moreover, the SPADs for 20 μm diameter active area achieve a low DCR and a broad spectral response. Therefore, the p-well/DNW SPAD can be used for high spatial resolution array in 3D imaging applications.

Acknowledgements

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