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An improved 16-element small-signal model for InP-based HEMTs

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Abstract: In this paper, an improved 16-element small-signal topology for InAlAs/InGaAs InP-based HEMTs has been proposed. The gate-source resistance (R_{gs}) is introduced into the topological structure to characterize the gate leakage current caused by the short gate channel spacing. The output conductance (g_{ds}) and drain delay factor (τ_{ds}) are proposed to characterize the impact of drain voltage on channel current and also the phase change by drain-source capacitor (C_{ds}), which can improve the fitting accuracy of S_{22}. The parasitic elements are calculated through open and short dummy structures, and the intrinsic parameters are extracted by Y-parameters after de-embedding the external parasitic parameters. The ultimate values of parameters are determined by optimization procedure to gain the best fitting precision. The results show that the simulation values of S-parameters and frequency characteristics fit well with the measured values, and the introduction of R_{gs} and τ_{ds} reduces the model error. The accurate and appropriate small signal model for InP-based HEMTs would be of great importance in the design of high-frequency circuits.

Key words: InP-based HEMTs, small-signal model, gate-leakage current, drain delay
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InP 基 HEMTs 器件 16 参数小信号模型

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摘要:针对 InAlAs/InGaAs InP 基 HEMTs 提出了一种 16 参数小信号拓扑结构.拓扑结构中引入栅源电阻(R_{gs})表征短栅沟间距引起的栅泄漏电流效应.另外还引入输出跨导(g_{ds})和漏延迟(τ_{ds})描述漏端电压对沟道电流的影响以及漏源电容(C_{ds})引起的相位变化,从而提高了 S_{22} 参数拟合精度.外围寄生参数通过 open 和 short 拓扑结构计算得出,本征部分利用去除外围寄生参数后的 Y 参数计算得出,最终模型参数值经过优化以达到最佳拟合状态而确定.结果表明,s 参数和频率特性的仿真值与测试数据拟合程度很好,R_{gs} 和 τ_{ds} 的引入降低了模型误差.准确合适的 InP 基 HEMTs 小信号模型对于高频电路设计非常重要.

关 键 词:InP 基高电子迁移率晶体管;小信号模型;栅泄漏电流;漏端延时

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Introduction

InP-based high electron mobility transistors (HEMTs) have demonstrated low noise, high frequency and superior gain characteristics. Therefore, they are significantly competitive candidates for various high speed circuits[1-2], millimeter-wave systems[3-4] and even THz applications[5-7]. Accurate small-signal model under certain bias is the foundation of constructing large-signal model and noise model, which would directly impact the performances and relate to circuit's qualities. Various e-

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quivalent topologies and methods to construct small-signal model of HEMTs have been developed according to the device structures, manufacture technology and applications[8-10]. However, the existing small-signal models of HEMTs mostly utilize the traditional single delay topology, which just describe the delay effect of gate voltage on channel current. Besides, the coupling effect between gate and channel is almost depicted by a capacitor with a series resistor.

Well-known, InAlAs/InGaAs structure without InP etching-stopping layer is a very attractive option for InP-based HEMTs to obtain high gain and frequency performances[11]. Two-step gate-recess process coupling high-selective wet-etching and non-selective digital wet-etching techniques may be intensely proposed to improve the performances and fabrication flexibility. However, the gate-leakage current would become non-negligible factor with very small distance between gate and channel. The fitting accuracy of input terminal would greatly influence the gain and noise performance of the amplifiers. Meanwhile, the output impedance of InP-based HEMTs is usually situated around the edge in Smith chart. Slightly inaccurate design would result in the mismatching of output terminal. Therefore, the fitting precision of device output terminal would seriously impact the gain, output power and stability characteristics of circuits.

In this paper, an improved 16-element small-signal topology has been proposed for InAlAs/InGaAs InP-based HEMTs. The resistance of gate-leakage current (R_{gs}) is adopted to characterize the non-negligible gate-leakage current caused by short gate-channel distance. Meanwhile, the output conductance (g_{ds}) with drain delay factor (τ_{ds}) is introduced to improve the fitting accuracy of output terminal. Finally, the introduction of R_{gs} and τ_{ds} makes the small-signal model much more suitable for InP-based HEMTs.

1 Device structure and fabrication

Figure 1 shows the schematic cross-section of an InAlAs/InGaAs InP-based HEMT. The epitaxial layer structure was grown on 3-inch semi-insulating (100) InP substrates by molecular beam epitaxy (MBE). It consists of an InAlAs buffer, an InGaAs channel, an unstrained 3 nm-thick InAlAs spacer layer, a Si-doped plane, an unstrained 12 nm-thick lnAlAs Schottky barrier layer, and a composite InGaAs cap layer consisting of a highly Si-doped $In_{0.6}Ga_{0.4}As$ cap layer and a Si-doped $In_{0.53}Ga_{0.47}As$ transition layer. All InAlAs layers were lattice matched with the InP substrate.

InP-based HEMTs' fabrication processes were similar with the previous works[12-14]. The mesa isolation was achieved by phosphorus acid-based wet chemical etching till $In_{0.52}Al_{0.48}As$ buffer layer. Source and drain Ohmic contacts were spaced 2 μm apart by lift-off process and Ti/Pt/Au metals were evaporated by electron beam evaporator without annealing. Subsequently, Ti/Au connection wires were evaporated to form the coplanar waveguide bond pads. The final and most important process was gate process, which included gate lithography, recess, and metallization. T-gate patterns were defined by electron beam lithography (EBL) with resist layers of PMMA/Al/UVIII. Ti/Pt/Au gate metals were evaporated and followed by the gate-recess etching through combining selective etching and digital etching. Additionally, the dummy open and short devices were also fabricated on the wafer to extract the parasitic parameters related to the bond pads.

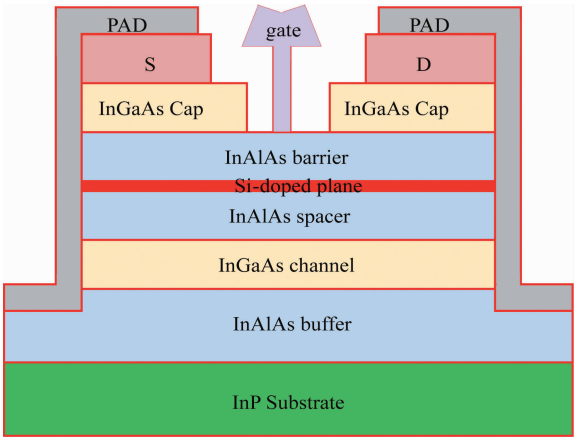

Fig. 1 Schematic cross-section of the InAlAs/InGaAs InP-based HEMT

图1 InAlAs/InGaAs InP基HEMT器件截面示意图

2 Extraction procedures

InP-based HEMTs with gate-width of 2×50 μm and gate-length of 0.15 μm were employed to construct the small-signal model, which biased at V_{gs} = 0.0 V, V_{ds} = 1.5 V to gain the maximum transconductance and frequency performances. The on-wafer S-parameters were characterized at frequencies ranging from 0.1 to 40 GHz with steps of 0.1 GHz at room temperature, including InP-based HEMTs, open and short dummy devices. The maximum measured frequency of 40 GHz is limited by the vector network analyzer of Agilent E8363B.

Based on the manufacturing process and operating principle of InP-based HEMTs, an improved 16-element small-signal topology is proposed as shown in Fig. 2. The parameters of topology include two parts: the parasitic elements induced by the pad metals and the intrinsic elements representing actual device characteristics. R_g, R_d and R_s are access resistors including Ohmic contact. L_g, L_d and L_s are parasitic inductors in series with access resistors. C_{pgd}, C_{pg} and C_{pd} are parasitic capacitors of pads. C_{gs} and R_i depict the coupling effect between gate and channel on source side, while C_{gd} describes the change of depletion region on drain side with bias voltage. Specially, C_{gs} and C_{gd} are a little different for the unequal electrostatic potential between gate and drain terminals. C_{ds} reflects the geometric capacitance between drain and source electrodes. g_m is the transconductance with delay factor of τ_{gs}. Specially, R_{gs} is introduced to characterize the gate-leakage current, and g_{ds} is the output conductance with drain delay factor of τ_{ds}. All elements are initially computed through the measured S-pa-

rameters and finally determined by optimization procedure to gain the best fitting precision.

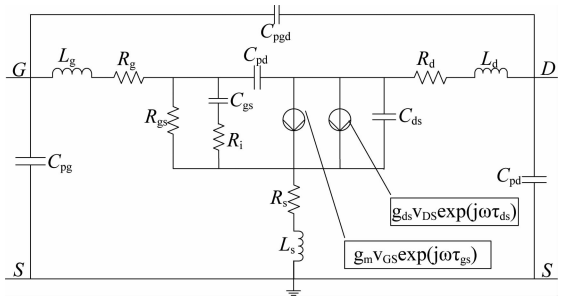

Fig. 2　Equivalent topology of InP-based HEMTs
图 2　InP 基 HEMT 器件等效拓扑

2.1　Parasitic parameters extraction

The equivalent topology of dummy open device is shown in Fig. 3, which contains the parasitic capacitors of C_{pgd}, C_{pg} and C_{pd}. Therefore, the parasitic capacitors can be solved by Eqs. (1-3) from the imaginary part of Y parameters, which are obtained by transferring from the measured S-parameters of open dummy device. The parasitic capacitance values by this method are shown in Table 1.

$$\mathrm{Im}Y_{11} = j\omega(C_{pgd} + C_{pg}) \quad , \quad (1)$$

$$\mathrm{Im}Y_{22} = j\omega(C_{pd} + C_{pgd}) \quad , \quad (2)$$

$$\mathrm{Im}Y_{12} = \mathrm{Im}Y_{21} = -j\omega C_{pgd} \quad . \quad (3)$$

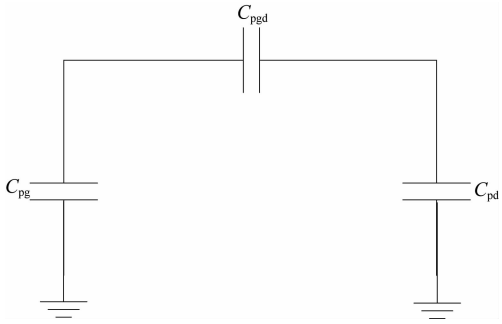

Fig. 3　Equivalent circuit of the open dummy structure
图 3　开路结构等效拓扑

Table 1　The parasitic capacitors by the open dummy structure

表 1　通过开路结构得到的寄生电容

Parameter	Value
C_{pg}	20 fF
C_{pd}	21 fF
C_{pgd}	4 fF

The equivalent topology of dummy short structure is shown in Fig. 4. The parasitic resistors and inductors in series can be extracted by the Z-parameters after de-embedding the parasitic capacitors from dummy short structure, as depicted by Eqs. (4-6). The computed parasitic resistors and inductors are shown in Table 2.

$$Z_{11} = R_s + R_g + j\omega(L_s + L_g) \quad , \quad (4)$$

$$Z_{22} = R_d + R_s + j\omega(L_d + L_s) \quad , \quad (5)$$

$$Z_{12} = Z_{21} = R_s + j\omega L_s \quad . \quad (6)$$

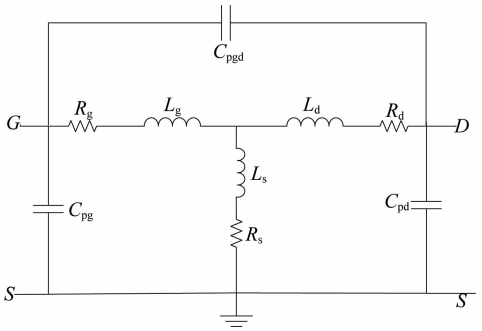

Fig. 4　Equivalent circuit of the short dummy structure
图 4　短路结构等效拓扑

Table 2　The parasitic resistors and inductors by the short dummy structure

表 2　通过短路结构得到的外围寄生电感和寄生电阻

Parameter	Value
L_g	53 pH
L_d	61 pH
L_s	5.7 pH
R_g	0.1 Ω
R_d	0.201 Ω
R_s	0.091 Ω

2.2　Intrinsic elements extraction

Intrinsic parameters of InP-based HEMTs can be determined from the measured intrinsic Y parameters after de-embedding external parasitic parameters, as Eqs. (7-10). The electron mobility of InP-based HEMTs is very high so that the drain delay of τ_{ds} is approximately equal to 0. Therefore, τ_{ds} and g_{ds} can be obtained by transforming Y_{22} to real and imaginary parts with trigonometric formula. The intrinsic elements of InP-based HEMTs are shown in Table 3.

$$Y_{11} = j\omega C_{gd} + \frac{j\omega C_{gs}}{1 + j\omega C_{gs} R_i} + \frac{1}{R_{gs}} \quad , \quad (7)$$

$$Y_{12} = -j\omega C_{gd} \quad , \quad (8)$$

$$Y_{21} = -j\omega C_{gd} + \frac{g_m e^{-j\omega\tau_{gs}}}{1 + j\omega C_{gs} R_i} \quad , \quad (9)$$

$$Y_{22} = j\omega(C_{gd} + C_{gs}) + g_{ds}\exp(-j\omega\tau_{ds}) \quad . \quad (10)$$

Table 3　The extracted intrinsic parameters of 2 × 50 μm InP-based HEMTs

表 3　2 × 50 μm InP 基 HEMT 的本征参数

Parameter	Value
τ_{gs}	12.4 ps
g_m	0.09 S
C_{gs}	68.8 fF
C_{ds}	24.2 fF
C_{gd}	7.8 fF
R_i	6.205 Ω
τ_{ds}	50 fs
g_{ds}	0.05 mS

3 Results and discussion

Well-known, InP-based HEMTs are widely used in high gain amplifiers, especially Cascode topology. Based on practical experience of circuit design, the output impedance of Cascode pair is usually situated around the edge in Smith chart. As a result, slightly inaccurate process would result in the mismatching of output terminal, and finally seriously impact the S-parameters of amplifier and even lead to circuit oscillation. Therefore, the improvement of output terminal fitting precision determines the characteristics of the amplifiers. As shown in Fig. 5 (a) and (b), the fitting precision of S_{22} has been obviously improved by adding τ_{ds}. Potential barrier lowering at source terminal would be induced by large drain voltage, and thus increase the channel carrier concentration, which is so-called drain induced barrier lowering (DIBL) effect. As the gate-length is decreased to several hundreds of nano-meters to gain high frequency performances, the DIBL effect cannot be ignored which would become very important for short-channel device. Therefore, the output conductance g_{ds} with drain delay factor τ_{ds} is proposed to characterize the impact of drain voltage on channel current. τ_{ds} represents a delay of the channel current response to drain voltage, which arises from the delay associated with the potential barrier change in source region. Besides, the introduction of τ_{ds} also takes the phase change by C_{ds} into consideration, which could improve the fitting accuracy of S_{22}.

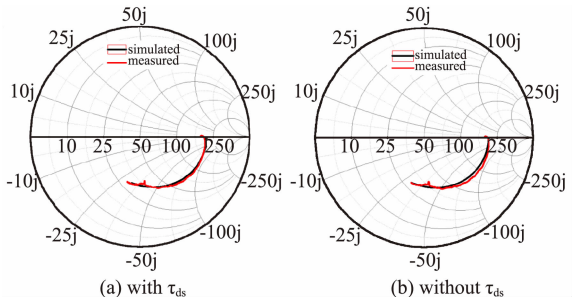

Fig. 5 The fitting of S_{22} for models (a) with τ_{ds}, (b) without τ_{ds}

图5 S_{22}拟合结果 (a) 添加 τ_{ds}的模型,(b)没有添加 τ_{ds} 的模型

Additionally, it is InAlAs semiconductor material that situates between gate and channel layer for InP-based HEMTs, and the distance is necessarily smaller than 15 nm to improve gain and frequency performances of InP-based HEMTs by two-step gate-recess etching process. R_{gs} is introduced to depict the inevitably severe gate-leakage current. Finally, the fitting of S-parameters has been done for model with τ_{ds} and R_{gs}, as shown in Fig. 6. It shows that the measured S-parameters demonstrate a good match with the simulated data.

In addition to S-parameters, the maximum oscillation frequency (f_{max}) and current cut-off frequency (f_T) are also important parameters for high frequency devices. Among them, f_{max} affects the device power gain, which is more important to the analog circuit. f_T determines the switching speed, which serves as a greater impact on the digital circuit. The value of f_T and f_{max} are determined by extrapolating the current gain (H_{21}) and maximum available/stable power gain (MAG/MSG) using a least squares fitting with a -20 dB/decade slope after subtracting the parasitic parameters due to the probing pads. As shown in Fig. 7, it can be seen that the simulated H parameters and gain performance show a good match with the measured values where f_T and f_{max} are 146 GHz and 220 GHz respectively.

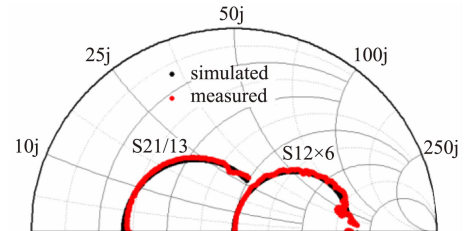

Fig. 6 Comparison of S parameters between measured and simulated

图6 测试和仿真的S参数拟合结果

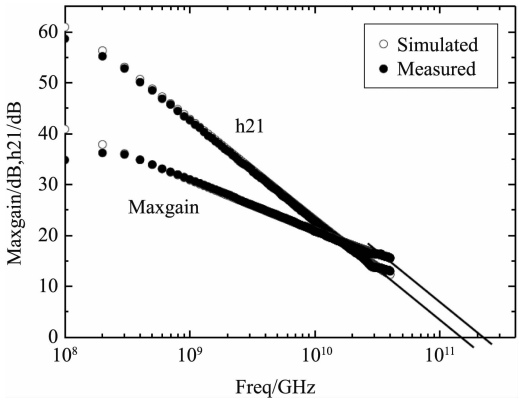

Fig. 7 Comparison of f_T and f_{max} between measured and simulated

图7 测试和仿真f_T和f_{max}拟合结果

The error factor (perror) has been widely used to represent the fitting accuracy of models. Especially, the error factor of perror involves S-parameters error (error S), stability factor error (error K) and gain error (error G). The function is as follows:

$$\text{perror} = \sqrt{\frac{(\text{error}S)^2 + (\text{error}K)^2 + (\text{error}G)^2}{3}} \quad . \quad (11)$$

The error factors have been computed for different

models by introducing R_{gs} and τ_{ds} gradually, and the values are shown in Table 4. It is obvious that the small-signal model with R_{gs} and τ_{ds} has much superior fitting accuracy compared to other models, which means the model is more suitable for InP-based HEMTs.

Table 4 The error factors for different models
表 4 不同模型的误差因子

Models	without R_{gs} and τ_{ds}	with R_{gs}	with τ_{ds}	with R_{gs} and τ_{ds}
Perror	0.294	0.269	0.291	0.266

4 Conclusions

In this paper, an improved 16-element small-signal topology has been proposed for InAlAs/InGaAs InP-based HEMTs on the basis of manufacturing process and operating principle. R_{gs} is adopted to describe the non-negligible gate-leakage current caused by short gate-channel distance. The output conductance g_{ds} with drain delay factor τ_{ds} is introduced to characterize the impact of drain voltage on channel current and also depicts the phase change by C_{ds}, which improves the fitting accuracy of S_{22}. The extraction process of all elements in small-signal topology is given in detail, and the values are ultimately determined by optimization procedure to gain the best fitting precision. The simulated S-parameters and frequency characteristics of f_T and f_{max} have shown good match with the measured values. Exactly the introduction of R_{gs} and τ_{ds} makes the small-signal model much more suitable for InP-based HEMTs. The more accurate small-signal model is of great significance on high-frequency circuits design.

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