第37卷第3期
2018年6月

红外与毫米波学报
J. Infrared Millim. Waves

Vol. 37, No. 3
June, 2018

文章编号: 1001-9014(2018)03-0261-08

DOI: 10.11972/j.issn.1001-9014.2018.03.002

# A low noise and high uniformity readout integrated circuit for IFPA applications

ZHOU Tong[1], HE Yong[1*], ZHAO Jian[2], JIANG Bo[1], SU Yan[1*]

(1. School of Mechanical Engineering, Nanjing University of Science and Technology, Nanjing 210094, China;
2. Department of Electronic Engineering, Tsinghua University, Beijing 100084, China)

**Abstract:** This paper proposed a readout integrated circuit (ROIC) with high uniformity and low-noise, by mitigating the fixed patter noise (FPN) of Infrared focal plane arrays (IFPA) to acquire high-quality infrared images. The row shared gain-controlling NMOS transistors are adopted in front-end circuit to reduce the pixel FPN. Furthermore, a novel correlated double sampling (CDS) structure is proposed to reduce the column FPN. Based on the simulation results, a 16 × 16 experimental chip has been manufactured adopting AMS 0.35 μm CMOS process. Extensive experiments have been implemented to verify the function and performance of the proposed readout circuit. The test results demonstrate the ROIC with the inherent advantages of low FPN and high uniformity, which makes it suitable for the application of high performance IFPA.

**Key words:** readout circuit, fixed patter noise suppression, correlated double sampling, high uniformity
**PACS:** 07.57.Kp, 42.30.-d.

# 一种用于非制冷红外焦平面阵列的低噪声高均匀性读出电路

周 同[1], 何 勇[1*], 赵 健[2], 姜 波[1], 苏 岩[1*]

(1. 南京理工大学 机械工程学院,江苏 南京 210094;
2. 清华大学 电子工程系,北京 100084)

**摘要:** 提出了一种高均匀性低噪声的读出电路,该电路通过抑制非制冷红外焦平面阵列固定模式噪声,从而可实现高质量的红外图像. 该电路前端采用了行共享的增益可控NMOS管抑制像元固定模式噪声,同时采用了新型的相关双采样电路抑制列固定模式噪声. 在仿真基础上,采用了AMS 0.35 μm CMOS工艺完成了16 × 16像元芯片的制备. 对芯片的大量测试结果表明提出的读出电路可以有效地降低非制冷红外焦平面阵列的固定模式噪声,同时具有高均匀性的特点,适用于高性能非制冷红外探测器.

**关 键 词:** 读出电路; 固定模式噪声抑制; 相关双采样; 高均匀性

**中图分类号:** TN432 **文献标识码:** *A*

## Introduction

A readout integrated circuit calculates the infrared radiation on the focal plane and transmits the signal to image manipulation circuit [1-4]. Reducing or restraining the readout noise can increase the signal-noise-ratio, leading to improve the quality infrared image [5-6]. There are mainly two kinds of noise in the readout circuit: the devices intrinsic noise (MOSFET device, etc.) and the additionally noise introduced by the operational mode the circuit structure. The former is mainly contributed by the $1/f$ noise, and the latter basically behaves the fixed patter noise (FPN) [7-9]. FPN consists of pixel FPN and column FPN, which is classified according to genesis. Pixel FPN is caused by the mismatch in the semiconductor manufac-

**Received date:** 2017-08-07, **revised date:** 2018-02-09 **收稿日期:** 2017-08-07, **修回日期:** 2018-02-09
**基金项目:** 国家自然科学基金(A2620110012),江苏省自然科学基金(BK20170853,BK20170850)
**Foundation items:** Supported by The General Program of National Natural Science Foundation of China (A2620110012) and National Natural Science Foundation of Jiangsu Province (BK20170853, BK20170850)
**Biography:** ZHOU Tong(1985-), male, Xuzhou, lecturer of Nanjing University of Science and Technology, Ph. D. Research area involves infrared readout integrated circuits and mixed-signal integrated circuits. E-mail: zhoutong@njust.edu.cn
* **Corresponding author:** E-mail: yhe1964@njust.edu.cn; suyan@njust.edu.cn

turing process of the transistor parameters (such as threshold voltage of transistors, gain, W, L, etc.), while the column FPN is brought about by column readout circuits. FPN can deteriorate images quality by causing vertical and spots stripes, which is irrespective to the light intensity. Therefore, it is important to suppress FPN to improve the ROIC performance [10-14].

A widely accepted technique reducing the FPN is CDS [15-17], which works by two steps, firstly, storing the noise on one clock phase, and then subtracting it at the following clock phase. This operation virtually eliminates FPN noise at the outputs of the circuit [18-20]. However, the conventional CDS circuits suffer from two main defects. One is that the pixel FPN caused by mismatch in the pixel circuit cannot be reduced, and the other is that both amplifier and the capacitors are widely adopted to fulfill the amplified FPN suppression functions, which will inject the additional noise and increase the chip size in conventional CDS technique.

Another method to reduce the FPN is pixel calibration technique [21-22]. In this approach, FPN calibration is implemented by gain control transistors controlled by on-chip DAC, which consumes large chip size and increase the complexity. In addition, the temperature response and uniformity are inevitably serious degenerated by the gain control transistors variation threshold voltage.

This paper presents a readout circuit structure to solve the above mentioned problems. FPN is reduced by two ways in this novel readout circuit. First, the row shared gain-controlling NMOS transistors and stable dark current suppression circuits adopted in front-end circuit can reduce the pixel FPN. Second, a novel CDS structure with signal capacitor is also proposed, which can reduce the column FPN introduced by amplifier offset noise. The proposed ROIC is featured with low FPN, high signal-noise ratio (SNR), high uniformity and small chip area of the CDS structure.

## 1 Circuit structure descriptions

### 1.1 Circuit architecture

The proposed ROIC consists of an M × N pixel bias array, dark current suppression unit, current-voltage conversion unit, signal capacitor CDS unit, and output unit (Fig. 1). An active pixel array connected to the M × N bias array responds to infrared radiation. The current directly proportional to the changed resistance is then generated as an infrared radiation signal, including the radiation-generated current and the dark current. These current signals are read out by the readout interface and transferred to the dark current suppression unit subsequently. Dark current is then suppressed by the dark current suppression unit. The current-voltage conversion is located at the end of each column, which is implemented by a column shared capacitor trans-impedance amplifier (CTIA). The CTIA performs the current-voltage conversion by integrating. The column shared CDS stage is proposed to reduce the FPN, which saves the active pixel and reference signals, and effectively decreases the noise through differential output existing in both the active and reference signals in sequence. Finally, the output circuit transfers the output signals to the following part of the IFPA signals processing system.

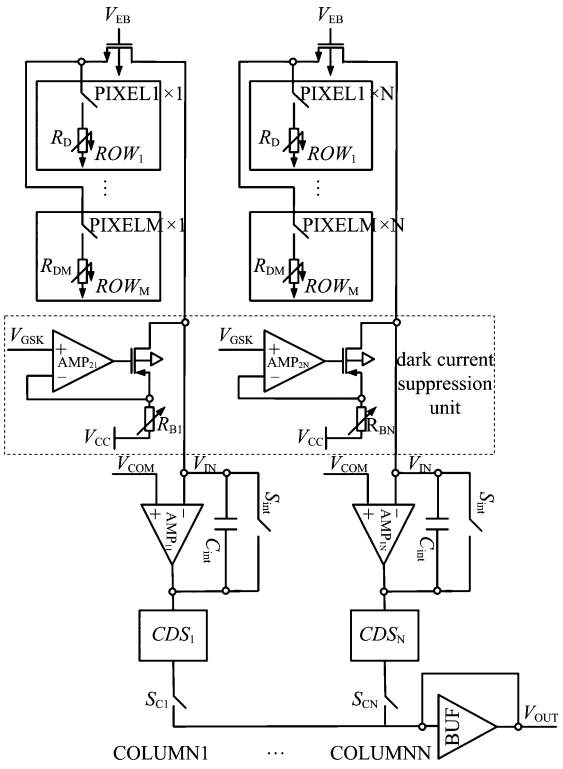


Fig. 1 Readout circuit architecture

**图1 读出电路结构**

### 1.2 Novel FPN suppression method

#### 1.2.1 Front-end circuit

The front-end circuit generates the bias voltage applied to the bolometer pixel and converts the pixel resistance changes to the current changes. The output current non-uniformity is one of the most concerned parameters, which directly influences the IFPA image quality. Taking into account of improving the non-uniformity of the circuit, the front-end circuit is proposed in Fig. 2.

It is composed by pixel bias array, dark current suppression unit, and current-voltage conversion circuit. The main property of the pixel bias array circuit is to bias the bolometer, and respond to the infrared radiation by resistance change. The pixel array is biased by a voltage through a MOS transistor $M_N1$. The detection current can be obtained:

$$I_D = \frac{1}{2}\mu_n C_{OX}\frac{W_{MN1}}{L_{MN1}}(V_{EB} - I_D R_D - V_{TH})^2 \quad (1)$$

where $W_{MN1}$ is the width of the $M_{N1}$, $L_{MN1}$ is the length of the $M_{N1}$, $V_TH$ is the threshold voltage of the NMOS transistor, $C_{OX}$ is the capacitance per unit of the transistor, is the mobility of the electron, $R_D$ is the resistance of the micro-bolometer. Figure 2 also shows the pixels in the same column have the same variations of $V_{TH}$, not affected by the row-to-row $V_{TH}$ variations [19], which will improve the output non-linearity.

However, the dynamic range and the charge storage

capacity are limited by the dark current, which should be skimmed before the integration stage for applications in high background radiation condition.

The dark current suppression circuit is composed of a PMOS device $M_{P1}$, a dark resistor $R_B$ and a high-gain differential amplifier ($AMP_2$). $M_{P1}$ is used to bias and sense the bias resistor $R_B$. $AMP_2$ is connected between the $M_{P1}$ gate node and the bias resistor node. The bias voltage can be stabilized to $V_{GSK}$ due to the deep negative feedback of the amplifier. The compensation current $I_B$ can be expressed as:

$$I_B = \frac{V_{CC} - V_{GSK}}{R_B} \quad , \quad (2)$$

where $R_B$ is the bias resistance to match the active pixel, which is shielded by a blind mask, not influenced by infrared ray. Adjustable bias voltage $V_{GSK}$ is generated by programmable digital to analog converter (DAC) outside the chip. So the detector current can be obtained:

$$I_I = I_D - I_B \quad . \quad (3)$$

The differential current $I_I$ is then integrated in CTIA located at the end of each column.

Due to row shared gain-controlling NMOS transistors $M_{N1}$ and stable compensation current generated by the bias voltage $V_{GSK}$, this circuit has a good high-uniformity and low FPN.

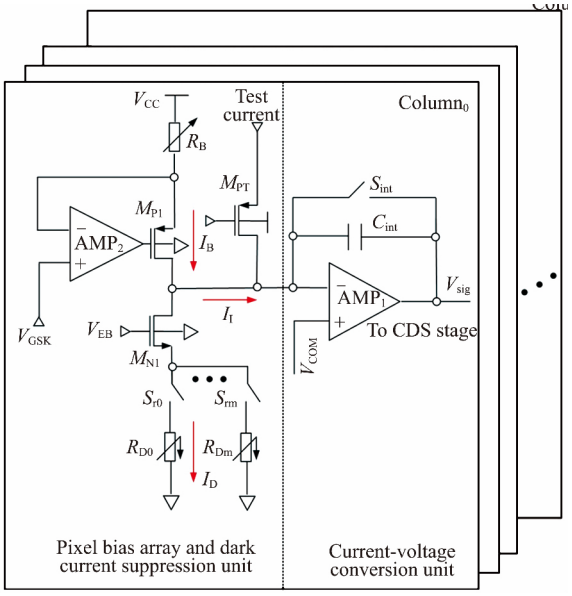


Fig. 2 Proposed FPN suppression circuit

**图 2 固定模式噪声抑制电路原理图**

### 1.2.2 Improved single capacitor CDS circuit

In order to reduce the FPN noise caused by column readout circuits, a novel CDS structure with signal capacitor is proposed. Single capacitor CDS circuit consists of source follower ($M_{P10}$, $M_{P11}$, $M_{P12}$), CDS capacitor ($C_{CDS}$), sampling switch (TG1), reset switch ($M_{P13}$), output voltage follower ($M_{P14}$, $M_{P15}$, $M_{n8}$, $M_{n9}$, $M_{n10}$), and column select phase switch (TG2) (Fig. 3).

Figure 4 shows the timing waveforms for the proposed readout structure of the CDS circuit. The sequencer on chip generates all digital signals necessary for a synchronous ROIC operation. CDS circuit realizes its capabilities through two periods: (I) one clock before integration completion, CRES goes at low level, $M_{P13}$ turns on, The B point of $C_{CDS}$ is charged by reference voltage $V_{COM}$. SAMP turns from high level to low level, TG1 turns on, source follower ($M_{P10}$, $M_{P11}$, $M_{P12}$) start to take effect. (II) After the integration completes, INT (control signal for $S_{int}$, Fig. 2) turns to high, the integrator output voltage is set to $V_{COM}$, before that, CRES turns from low to high, the B point of $C_{CDS}$ is suspended. At stage (I), the voltage of A and B point can be obtained as follows:

$$V_A(\mathrm{I}) = V_{sig} + V_{SG,Mp12} + V_{offset} + V_{noise1} \quad , \quad (4)$$

$$V_B(\mathrm{I}) = V_{COM} \quad . \quad (5)$$

In Eq. (4), $V_{sig} = V_{COM} - \frac{I_I T}{C_{int}}$ is integrator output signal, $V_{SG,Mp12}$ is $M_{P12}$ source-gate voltage, $V_{offset}$ is AMP1 offset voltage, $V_{noise1}$ is noise introduced by FPN noise of integration circuit.

At stage (II), CRES turns from low to high, which lead to the B point of $C_{CDS}$ be suspended. INT turns to low after that, the integrator circuit is reset, as the charges across the capacitor $C_{CDS}$ cannot be mutated:

$$C_{CDS}\{V_A(I) - V_B(I)\} = C_{CDS}\{V_A(\mathrm{II}) - V_B(\mathrm{II})\} \quad . \quad (6)$$

At stage (II), the voltage of A and B point can be obtained as follows:

$$V_A(\mathrm{II}) = V_{COM} + V_{SG,Mp12} + V_{offset} + V_{noise2} \quad . \quad (7)$$

It should be noted that, due to the dominant noise is low-frequency noise induced by the focal plane array, there is significant correlation between the two samplings, so $V_{noise1} \approx V_{noise2}$ can be formulated, we can thus obtain:

$$V_B(\mathrm{II}) = 2V_{COM} - V_{sig} \quad . \quad (8)$$

Using $V_{sig} = V_{COM} - \frac{I_I T}{C_{int}}$ in Eq. (8) we obtain:

$$V_B(\mathrm{II}) = V_{COM} + \frac{I_I T}{C_{int}} \quad . \quad (9)$$

As seen from Eq. (9), the FPN noise has been eliminated by charge transfer when sampling completed. The voltage response to radiation is stored in capacitor $C_{CDS}$, which is irrelevant to the offset voltage $V_{offset}$.

The FSYNC and DATAVALID are output pins indicating the output data status which are also controlled by the internal sequencer. The frame synchronization FSYNC denotes a new frame, while DATAVALID indicates a new row. When DATAVALID goes high, the column select phase (COL1-COLN) is enabled serially to sample the voltage signals one column after another, and transfer them to the output stage.

## 2 Experiment results

The HSPICE simulations are performed for AMS 0.35 μm 2P4M process. Figure 5 shows the simulation of integrator output voltage with different input current, sweeps from −70 nA to 70 nA. The simulation is imple-

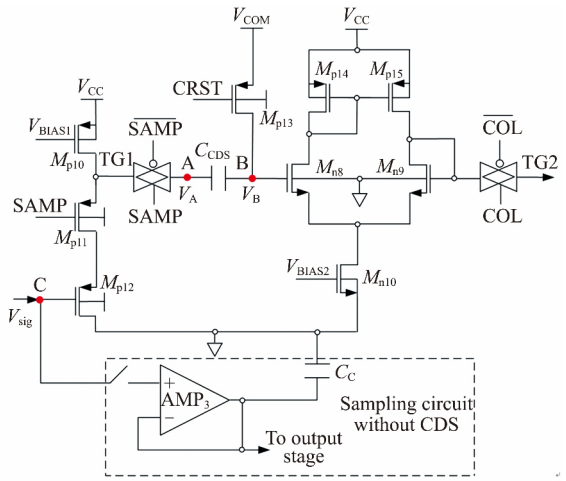


Fig. 3 Proposed single capacitor CDS circuit

**图3 单电容相关双采样电路原理图**

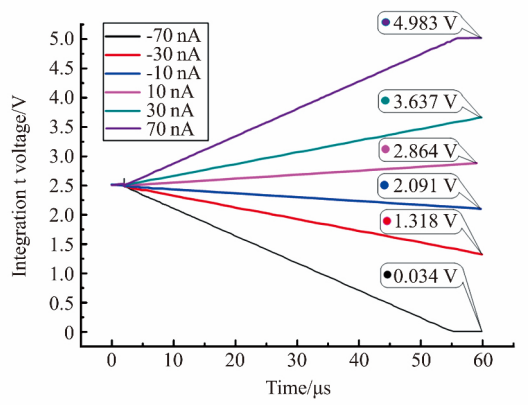


Fig. 5 Parametric sweep and its performance analysis waveforms on the integration node of one unit cell

**图5 对一个单元的积分器进行参数扫描和性能分析的仿真波形**

mented at 5 V power supply, 58 μs integration time and 3.75 pF integration capacitor. Figure 5 shows the integration circuit with performance of the high linearity and nearly rail to rail output swing.

Figure 6 shows simulation waveforms of point A, B and C in Fig. 3 with 15 nA input current. It also indicates how CDS circuit works. During stage (I), the output signal of the integration node (C) is sampled on the point A ($V_A$) at the end of integration phase which is held until the stage (II). The voltage of point B ($V_B$) is equal to the $V_COM$ because CRES is set at low level, $M_{P13}$ is on, which makes point B connected to the reference voltage ($V_{COM}$). In stage (I), $V_A$ is 2.299 V and $V_B$ is 2.50 V. In stage (II), $M_{P13}$ is set off firstly which causes the point B suspended. In stage (Ⅱ), point A is connected to the negative of the AMP1, so $V_A$ is changed to 2.963 V. Since the capacitor $C_{CDS}$ charge cannot be mutated, $V_B$ is changed to 3.162 V. During the CDS stage, FPN of integration unit and the source-gate voltage of $M_{P12}$ (see Fig. 3) are eliminated effectively.

Figure 7 shows the noise spectral density of the front-end circuit, the noise is simulated under the conditions of zero input to remove the effect of the input current. As shown in Fig. 7, the low frequency noise is in leading side, and the RMS noise of the front-end circuit can be calculated through integration in effective bandwidth range, which is 7.196E-11 A. To estimate the output noise of the proposed circuit, sampling is performed at the output note, and then the noise spectral density can be calculated as shown in Fig. 8, in which 0 dB is defined to be 1 $V^2/Hz$, and the RMS noise is 0.024 mV. The corner simulation is also performed to estimate the FPN suppression effect, the conditions of

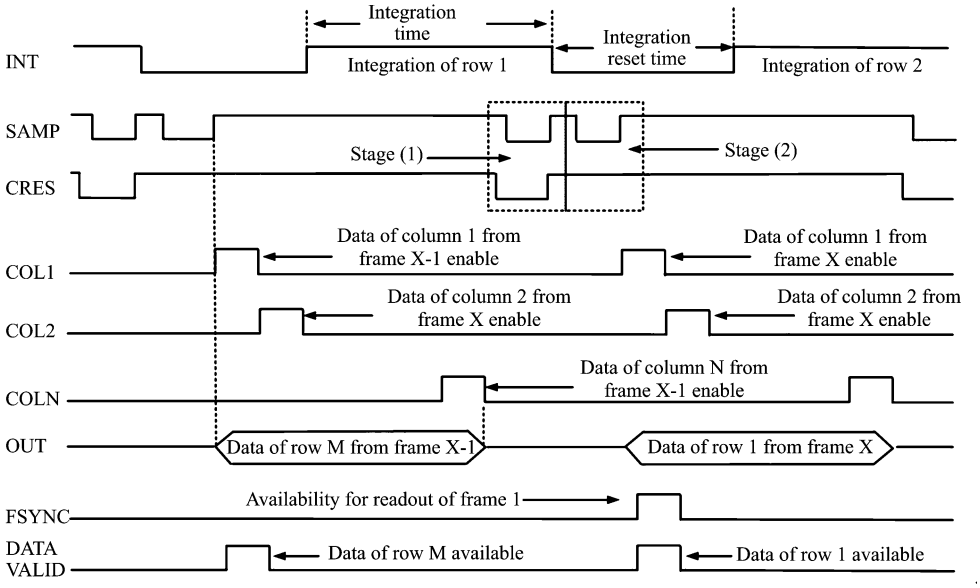


Fig. 4 Timing waveforms for the proposed circuit

**图4 读出电路时序逻辑图**

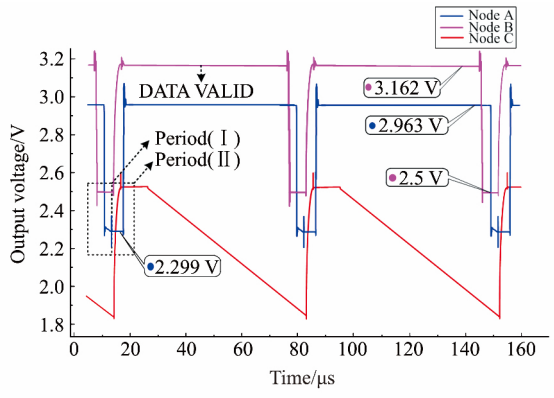


Fig. 6　Simulation waveform with 15 nA input current
**图 6　15 nA 电流输入条件下的仿真波形**

corner simulation is shown in Table 1. We choose five different threshold voltages of NMOS and PMOS as the corner simulation conditions. Figure 9 shows the simulation results. The FPN introduced by the threshold voltages can be well suppressed with proposed CDS circuit.

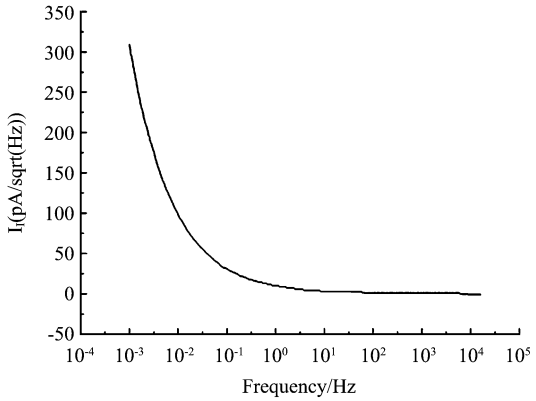


Fig. 7　Noise spectral density of front-end circuit
**图 7　前端电路噪声谱密度曲线**

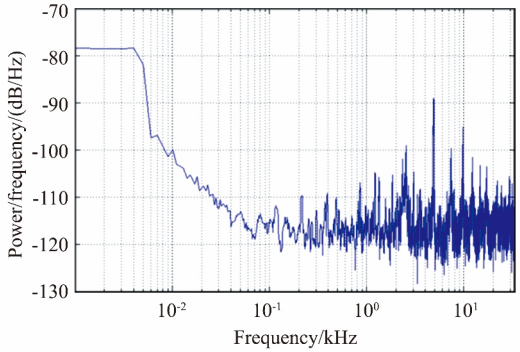


Fig. 8　Noise spectral density of outputs
**图 8　输出端噪声谱密度曲线**

Figure 10 shows the die photo of the 16 × 16 ROIC chip which is fabricated under AMS 0.35 μm CMOS process and the evaluation board of the chip. A unit cell

**Table 1　Conditions of corner simulation**
**表 1　工艺角仿真条件**

| Conditions | $V_{TH}$(NMOS) | $V_{TH}$(PMOS) |
|---|---|---|
| TT | 552 mV | −649 mV |
| FF | 503 mV | −598 mV |
| SS | 605 mV | −694 mV |
| FS | 503 mV | −694 mV |
| SF | 605 mV | −598 mV |

consumes a 30 μm × 25 μm area and less than 0.05 mW power. The power supply for the chip is 5 V. The compensation current and bias current are globally calibrated by the adjusting control voltages, $V_{GSK}$ and $V_{EB}$, using the discrete 16 bit DAC (AD5541). The reference voltage of integration and CDS circuits is supplied by the 2.5 V reference source ADR421. In order to obtain the chip parameters such as injection efficiency, output linearity and FPN suppression performance, high precision current source is used to generate the DC current simulated as the infrared current. 24 bit ADC (ADS1258) is implemented to convert the output voltage to the digital signal, and the output signal can also be observed by the oscilloscope. The overall timing and control sequences are generated using FPGA connected with the evaluation board by the pin connector.

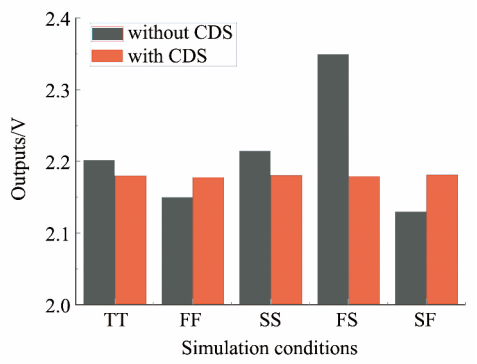


Fig. 9　Corner simulation results
**图 9　工艺角仿真结果**

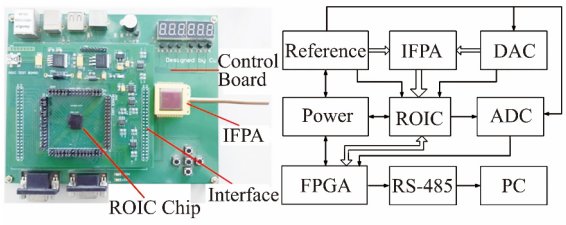


Fig. 10　The evaluation board of the chip
**图 10　芯片评估电路板**

Figure 11 shows the measurement waveform of the readout chip. The red waveforms is the output of the NODE A, and the blue waveforms is the output of the NODE B. The test curves coincide well with the simulation curves, which also validate the soundness of the proposed ROIC.

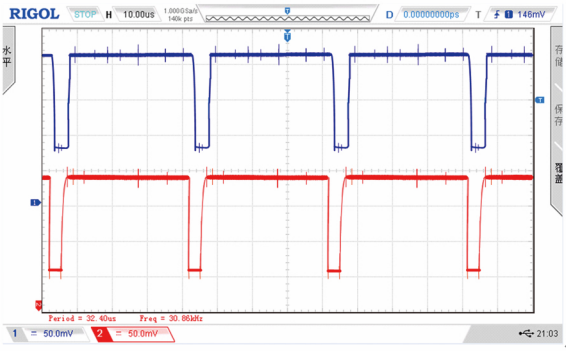


Fig. 11 Measurement waveform for the voltage signals with 15 nA input current

**图 11 15 nA 输入电流条件下电压信号测试波形图**

The output noise measurement was performed by reading a 16 × 16 array 1 500 times and performing noise power density. Data acquisition is delayed by 10 s to stabilize the array after one frame data acquisition completion. Pixels in four rows are simultaneously measured in order to accurately evaluate the ROIC noise (Fig. 12). Low frequency noise is in leading side in output noise, as the CTIA is a low pass filter with the band-width half of the reciprocal of the integration time. The integration time is set to 30 μs in the experiment, so the band-width is 16.7 kHz. Additionally, the maximum measured root mean square noise (0.01 ~ 1 Hz) is 0.178 mV (Row Two).

Figure 13 shows the measured output linearity. Extend blackbody is used to simulate different temperature target, with temperature range from −10℃ to 80℃. The integration time is set to 58 μs with 3.75 pF integration capacitance. Figure 10 indicates that the proposed structure possesses better than 99% linearity with output voltage swing from 0.53 V to 4.38 V, under temperature range from 5℃ to 70℃. We can also calculate that the voltage responsivity is 59 mV/K.

Figure 14 shows the 16 × 16 ROIC FPN test results by blackbody calibration. The 16 × 16 pixel micro-bolometer was placed at 30 degrees blackbody environment without infrared radiation. Required timing waveforms were generated by FPGA, and high-precision data acquisition system was used to measure the output voltage. Figure 14 (a) is the test results of the proposed ROIC without CDS circuit, it can be seen from the figure the circuit has a large FPN noise because the offset voltage have a great influence on the results. Figure 14 (b) is the test results of the ROIC with proposed CDS circuit. The max-min output non-uniformities caused by FPN, with the conventional and proposed readout integrated circuit are 16 mV and 3.5 mV, respectively. The proposed scheme output non-uniformity is reduced to 22 % compared to the conventional scheme. It can be seen from the figure that the FPN noise can be significantly suppressed with proposed row shared gain-controlling NMOS transistors and single capacitor CDS circuit, the focal plane could exhibit a better uniformity.

Some key parameters of the chip are measured, and the comparison between this work and other ones of the

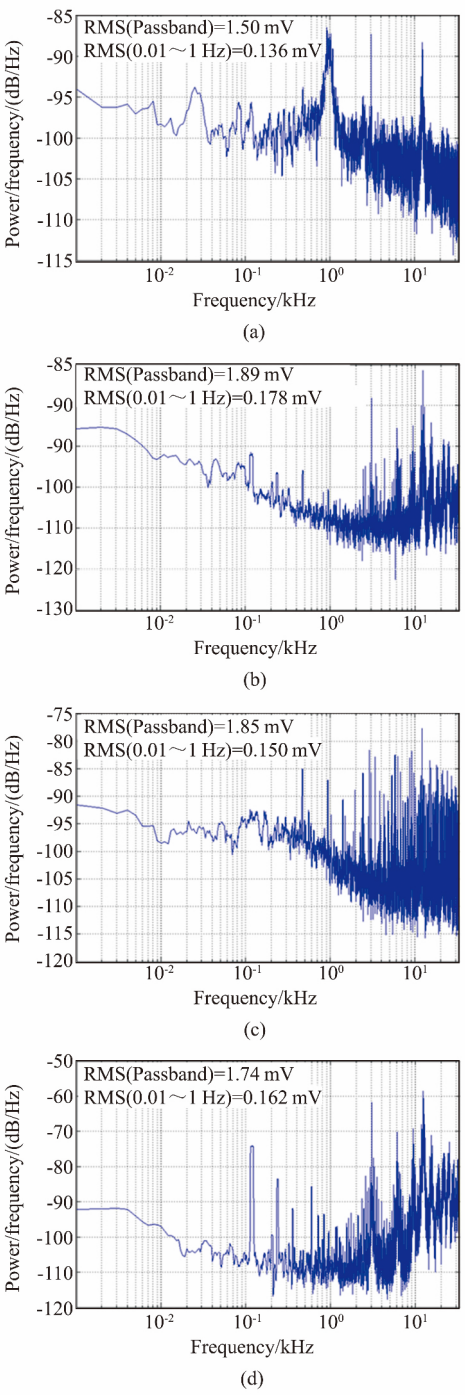


Fig. 12 Measurement of the output noise spectrum, (a) output noise spectrum of row one, (b) output noise spectrum of row two, (c) output noise spectrum of row three, (d) output noise spectrum of row four

**图 12 电路输出信号噪声功率谱,(a) 第一行像元输出噪声功率谱,(b) 第二行像元输出噪声功率谱,(c) 第三行像元输出噪声功率谱,(d) 第四行像元输出噪声功率谱**

literature is listed in Table 2. As shown in Table 2, the test results demonstrate the ROIC with the inherent ad-

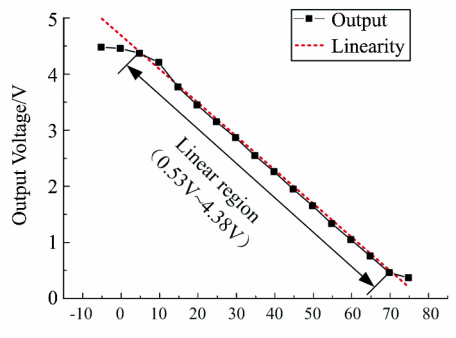


Fig. 13　The linearity measurement results of the designed circuit

**图 13　读出电路线性度测试结果**

vantages of low noise and high dynamic range. Furthermore, benefit from the proposed two-step FPN suppression method, the fixed patter noise is also significantly reduced.

## 3　Conclusions

This paper proposes a ROIC which could dramatically decrease the FPN caused by pixel noise and column mismatch. The ROIC consists of an M × N pixel bias array, dark current suppression unit, current-voltage conversion unit, signal capacitor CDS unit, and output unit. The inherent advantages of low noise and high uniformity make the proposed readout circuit fit for the application of the high uniformity and high performance IFPA.

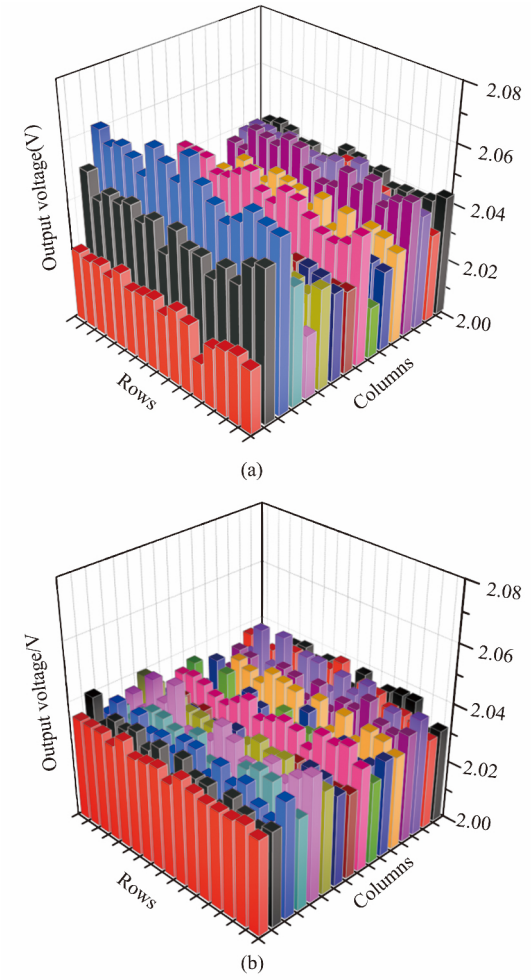


Fig. 14　The FPN of 16 × 16 ROIC measured by two methods, (a) FPN measured without CDS circuit, (b) FPN measured with proposed CDS circuit

**图 14　采用两种方法对 16 × 16 像元读出电路 FPN 的测试结果,(a) 无 CDS 电路的 FPN 测试结果,(b) 带 CDS 电路的 FPN 测试结果**

## References

[1] Hsieh C C, Wu C Y, Jih F W, *et al*. Focal-plane-arrays and CMOS readout techniques of infrared imaging systems [J]. *IEEE Transactions on Circuits & Systems for Video Technology*, 1997, **7**(4): 594-605.

[2] Jo Y M, Woo D H, Kang S G, *et al*. Very Wide Dynamic Range ROIC With Pixel-Level ADC for SWIR FPAs [J]. *IEEE Sensors Journal*, 2016, **16**(19): 7227-7233.

[3] Chen X, Lv Q. A versatile CMOS readout integrated circuit for microbolometric infrared focal plane arrays [J]. *Optik - International Journal for Light and Electron Optics*, 2013, **124**(20): 4639-4641.

[4] Zhao H, Liu X, Xu C. A low power cryogenic 512 × 512-pixel infrared readout integrated circuit with modified MOS device model [J]. *Infrared Physics & Technology*, 2013, **61**: 111-119.

[5] Blanksby A J, Loinaz M J. Performance analysis of a color CMOS photogate image sensor [J]. *IEEE Transactions on Electron Devices*, 2000, **47**(1): 55-64.

**Table 2　Comparison between this work and existing ROICs**

**表 2　测试性能对比表**

| Performance | Capability | Ref. [14] | Ref. [17] | Ref. [22] |
|---|---|---|---|---|
| Technology | SMIC 0.18 μm 1P6M CMOS | 0.35 μm 2P4M CMOS | CMOS | 0.35 μm 2P4M CMOS |
| Pixel size | 30 μm × 25 μm | 50 μm × 50 μm | 15 μm × 15 μm | 35 μm × 35 μm |
| Format | 16 × 16 | 128 × 128 | 640 × 512 | 64 × 64 |
| Power supply | 5 V | 3.3 V | 3.3 V | 3.3 V |
| Power dissipation | 13.2 mW | 16.5 mW | 120 mW | |
| Linearity | > 99% | | 99% | |
| Output voltage swing | 3.85 V | 1.4 V | ≤ 2.0 V | |
| Responsivity | 59 mV/K | | 6.4 mV/K | |
| Output noise | 0.178 mV rms | 0.205 mV rms | 0.631 mV rms | |
| Dynamic range | 84.6 dB | 80.9 dB/95.4dB | 74.3 dB | |
| FPN | Reduced to 22 % | | | Reduced to 26 % |

[6] Degerli Y, Lavernhe F, Magnan P, *et al*. Non-stationary noise responses of some fully differential on-chip readout circuits suitable for CMOS image sensors [J]. *IEEE Transactions on Circuits & Systems II Analog & Digital Signal Processing*, 1999, **46**(12): 1461-1474.
[7] Dupont B, Dupret A, Belhaire E, *et al*. FPN Sources in Bolometric Infrared Detectors [J]. *IEEE Sensors Journal*, 2009, **9**(8): 944-952.
[8] Vatteroni M, Covi D, Sartori A. A linear-logarithmic CMOS pixel for high dynamic range behavior with fixed-pattern-noise correction and tunable responsivity [C]. *IEEE SENSORS* 2008 *Conference*, 2008, 930-933.
[9] Kim Y S, Woo D H, Jo Y M, *et al*. Low-Noise and Wide-Dynamic-Range ROIC With a Self-Selected Capacitor for SWIR Focal Plane Arrays [J]. *IEEE Sensors Journal*, 2017, **17**(1), 179-184.
[10] Yonemoto K, Sumi H, Suzuki R, *et al*. A CMOS image sensor with a simple FPN-reduction technology and a hole accumulated diode [C]. *Solid-State Circuits Conference*, 2000, 102-103.
[11] Wolf A, Pezoa J E, Figueroa M. Modeling and Compensating Temperature-Dependent Non-Uniformity Noise in IR Microbolometer Cameras [J]. *Sensors*, 2016, **16**(7): 1121.
[12] Cruz C A D M, Monteiro D W D L, Souza A K P, *et al*. Voltage Mode FPN Calibration in the Logarithmic CMOS Imager [J]. *IEEE Transactions on Electron Devices*, 2015, **62**(8): 2528-2534.
[13] Dem'yanenko M A, Kozlov A I, Marchishin I V *et al*. Development of analog-digital readout integrated circuits for infrared focal plane arrays [J]. *Optoelectron. Instrument. Proc*, 2016, **52**(6): 630-636.
[14] Woo D H, Nam I K, Lee H C. Smart Reset Control for Wide-Dynamic-Range LWIR FPAs [J]. *IEEE Sensors Journal*, 2011, **11**(1): 131-136.
[15] Im S, Park S G. Thermal noise analysis of switched-capacitor integrators with correlated double sampling [J]. *International Journal of Circuit Theory & Applications*, 2016, **44**(12): 2101-2113.
[16] Popowicz A. Analysis of correlated double sampling circuit with integration [J]. *Przeglad Elektrotechniczny*, 2012, **88**(2): 200-203.
[17] Altun O, Tasdemir F. Low-noise readout circuit for SWIR focal plane arrays [C]. *SPIE Defense + Security*, 2017: 1017707.
[18] Enz C C and Temes G C. Circuit techniques for reducing the effects of op-amp imperfections: autozeroing, correlated double sampling, and chopper stabilization [J]. *Proceedings of the IEEE*, 1996, **84**(11): 1584-1614.
[19] Wey H, Guggenbuhl W. Noise transfer characteristics of a correlated double sampling circuit [J]. *IEEE Transactions on Circuits & Systems*, 1986, **33**(10): 1028-1030.
[20] Kim D, Bae J, Song M. A high speed CMOS image sensor with a novel digital correlated double sampling and a differential difference amplifier [J]. *Sensors*, 2015, **15**(3): 5081-5095.
[21] Fieque B, Tissot J L, Trouilleau C. Uncooled microbolometer detector: Recent developments at Ulis [J]. *INFRARED PHYSICS & TECHNOLOGY*, 2007, **49**(3): 187-191.
[22] Kim G, Lim S, Kim Y, *et al*. High-uniformity post-CMOS uncooled microbolometer focal plane array integrated with active matrix circuit [C]. *Transducers & Eurosensors Xxvii: the, International Conference on Solid-State Sensors, Actuators and Microsystems. IEEE*, 2013: 2361-2364.

(上接第260页)

And the project is supported by National Key R&D Program of China (2016YFB0402401) and the National Science Foundation of China (No. 61376052, 61475179 and 61604159).

## References

[1] SHAO Xiu-mei, GONG Hai-mei, LI Xue, *et al*. Developments of High Performance Short-wave Infrared InGaAs Focal Plane Detectors [J]. *Infrared Technology*, 2016, **38**: 629-635.
[2] Omer Ceylan, Atia Shafique , Abdurrahman Burak, *et al*. Digital readout integrated circuit (DROIC) implementing time delay and integration (TDI) for scanning type infrared focal plane arrays (IRFPAs) [J]. *Infrared Physics & Technology*, 2016, **79**: 101-112.
[3] HUANG Zhang-cheng, CHEN Yu, HUANG Song-lei, *et al*. Analysis and simulation of a new kind of noise at the input stage of infrared focal plane array [C]. *Proc. SPIE*, 2014. **9100**(3).
[4] ZHU Hui, LI Yao-qiao, CHEN Xin-yu, *et al*. A design scheme of digital output for IRFPA [J]. *Laser & Infrared*, 2007, **37**: 997-1000.
[5] GAO Lei, ZHAI Yong-cheng, LIANG Qing-hua, *et al*. RFPA ROIC integrated digital output [J]. *InInfrared and Laser Engineering*, 2015, **44**(6): 1686-1691.
[6] HUANG Song-lei, HUANG Zhang-cheng, CHEN Yu, *et al*. A low noise high readout speed 512 × 128 ROIC for shortwave InGaAs FPA [C]. *Proc. SPIE*, 2015, 9521.
[7] Gisela de La Fuente-Cortes, Guillermo Espinosa Flores-Verdad, Victor R. Gonzalez-Diaz, *et al*. A new CMOS comparator robust to process and temperature variations for SAR ADC converters [J]. *Analog Integrated Circuits and Signal Processing*, 2017, **90**: 301-308.
[8] HUA Fan. Effective method to improve linearity of high-resolution SAR ADC [J]. *Microelectronics Journal*, 2017, **61**: 35-42.
[9] ZHANG Dai, Ameya Bhide and Atila Alvandpour. A 53-nW 9.1-ENOB 1-kS/s SAR ADC in 0.13-m CMOS for Medical Implant Devices [J]. *IEEE J. Solid-State Circuits*, 2012, **47**(7): 1585-1593.
[10] LIU C-C, CHANG S-J, HUANG G-Y, *et al*. A 10-bit 50-MS/s SAR ADC with a monotonic capacitor switching procedure [J]. *IEEE J. Solid-State Circuits*, 2010, **45**(4): 731-740.
[11] Phillip E. Allen, Douglas R. Holberg. CMOS Analog Circuit Design [M], Beijing: Publishing House of Electronics Industry (Phillip E. Allen, Douglas R. Holberg. CMOS 模拟集成电路设计, 北京: 电子工业出版社), 2007: 483-485.