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# Design and implementation of high performance single-photon avalanche diode in 180 nm CMOS technology

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**Abstract**: A wide spectral range and fast Single-photon avalanche diode (SPAD) chip which can be integrated with actively quenching circuit for large array realization is designed and implemented. The precise circuit model of SPAD for simulating the static and dynamic behaviors in Geiger-mode is used. The device with an 8 μm diameter active area is fabricated in GSMC 180 nm CMOS image sensor (CIS) technology. With the efficient device's structure, the low breakdown voltage is 15.2 V and quenching time is 7.9 ns. Additionally, the device achieves wide spectral sensitivity and enables maximum photon detection probability (PDP) of 15.7% from 470 to 680 nm of wavelength at low excess voltage. Moreover, it exhibits a relatively low dark count rate (DCR) at room temperature.

**Key words**: single-photon avalance diode (SPAD), photon detection probability (PDP), model, Geiger mode, CMOS CIS technology

**PACS**: 85.60. Bt, 85.60. Dw, 85.30. -z.

# 高性能单光子雪崩二极管在180 nm CMOS工艺中的设计与实现

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**摘要**：为了实现大阵列电路集成，文中设计和实现了一种能与主动淬火电路集成的宽光谱范围和快速的单光子雪崩二极管(SPAD)芯片.一个精确的单光子雪崩二极管电路模型模拟了其在盖革模式下的静态和动态行为.该有源区直径为8 μm的单光子雪崩二极管器件是基于上海宏利GSMC 180 nm CMOS图像传感器(CIS)技术实现的.由于采用有效的器件结构，其击穿电压是15.2 V，淬灭时间是7.9 ns.此外，该器件实现了宽的光谱灵敏度，其在低过电压下的光子探测概率(PDP)从470 nm到680 nm光波长段最高可达15.7%.并且它在室温下的暗计数率相当低.

**关　键　词**：单光子雪崩二极管；光子探测概率；模型；盖革模式；CMOS图像传感器技术

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## Introduction

Among the advanced CMOS image sensors reported before, the most appealing options in terms of high sensitivity and fast timing are those based on Single-photon avalanche diodes (SPADs)[1]. SPADs are conventional devices, which are able to detect single photons thus allowing the measurement of weak optical signals. These devices are used in diverse time-correlated applications, such as biomedical diagnostics[2], fast optical imaging, space telescopes[3] and 3D cameras.

Essentially, a SPAD device is a common P-N junction, operating in Geiger-mode, reverse biased at a voltage '$V_b$' well above its breakdown threshold '$V_{BR}$'. As the electric field is so high that a single charge carrier in-

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**Biography**: Jin Xiang-liang (1974-), male, Professor, China. Research interests include MEMS and readout circuit design, CMOS image sensor design, ESD, and mixed-mode application-specific integrated circuits

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jected in the depletion layer may trigger a self-sustaining avalanche, the current rises promptly to a macroscopic steady level. Current keeps flowing until the charge multiplication process is interrupted by lowering the reverse bias of the junction below the $V_{BR}$ for avoiding permanent damage in SPAD and detecting subsequent photons[4]. Therefore, appropriate quenching electronic circuit is needed for every SPAD pixel.

In consideration of well designing an integrated SPAD array detector, it is necessary to set up a precise circuit model for SPAD and to improve SPAD performance. Therefore, an accurate SPAD model consisting of generic analog components and a behavioral description by Verilog-A language is used in this work to model the static and dynamic behaviors. Moreover, the main photon-sensitive junction with a wide depletion region is designed to enhance spectral response.

Based on the adopted model, a set of STI-Bound SPAD devices fabricated in GSMC 180 nm CIS technology has been designed and tested. The superior performance of SPADs in standard CIS process has also inspired the integration of linear arrays of SPAD with dedicated processing circuitries for three-dimension imaging purposes.

## 1 Precise circuit model of SPAD

A piecewise linear model through a behavioral description by Verilog-A codes is used[5], which can overcome some typical disadvantages of inadequate accuracy and convergence problems reported in tradition models[6-8]. The schematic diagram of the used precise model is shown in Fig. 1, which is mainly composed of the central processing module CP, a voltage comparator COMP and an ideal set-reset latch SR_LATCH. CP implements the piecewise linear characteristic as sketched in Fig. 2(a), and both CP and COMP are implemented by Verilog-A languages. Switch T controls the avalanche triggering. $C_d$ is stray capacitance of the depletion layer, and $C_p$ is the parasitic capacitance, which mainly depends on the practical SPAD structure and the associated quenching circuit.

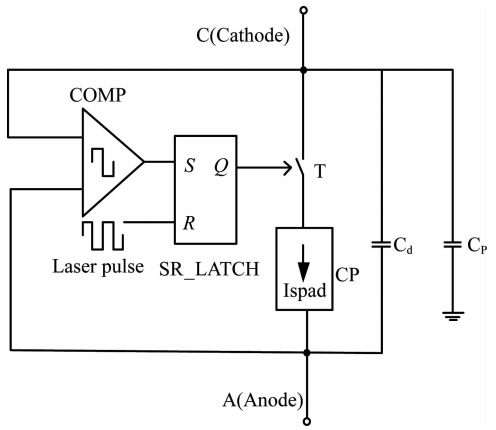


Fig. 1　schematic diagram of the precise model
图 1　精确电学模型的电路原理图

The model provides a more exact static description of SPAD and can quench the avalanche current automatically when the bias voltage '$V_b$' is below the breakdown voltage '$V_{BR}$'. As a result, the model permits free-running simulations in Cadence or other circuit simulation tools. To resolve the convergence problems during simulation, the practical voltage-current characteristic can be approximated as follows:

$$F_1(V_b) = I_{sat} \quad , \quad (1)$$

$$F_2(V_b) = I_{sat} \times e^{eV_b - V_{BR}} \quad , \quad (2)$$

$$I_{SPAD}(V_b) \approx -n \times \ln\left[e^{-\frac{F_1(V_b)}{n}} + e^{-\frac{F_2(V_b)}{n}}\right] \quad , \quad (3)$$

'$I_{rev}$' is the reverse current of the SPAD in linear-mode. Equation (3) is a continuous and differentiable function for the voltage-current characteristic. The representative value of '$n$' ranges from $10^{-4}$ to $10^{-6}$, which is a scaling factor introduced to prevent overflow or underflow during the computation.

The static behaviors of CP and COMP are described by Verilog-A codes. The module CP implements Eqs. (1)-(3) after defining the main electrical and simulation parameters. In the block COMP, the input cathode and anode voltages are used to evaluate the voltage across the diode and next compared with $V_{BR}$. Module set-reset latch is composed of two ideal NOR gate, whose set terminal is controlled by the output of the comparator while reset terminal is controlled by the laser pulse. The avalanche current flows through the SPAD when a photon reaches and $V_b$ is higher than $V_{BR}$. The theoretic piecewise linear *I-V* characteristic of accurate circuit model as depicted in Fig. 2(a) includes three SPAD characteristic parameters: the breakdown voltage '$V_{BR}$', the reverse saturation voltage '$V_{sat}$' and the reverse saturation current '$I_{sat}$'. However, the avalanche current of the traditional model reported in Refs. [6-7] is not saturated, which violates the apparent fact.

The main parameters of the used precise circuit model of SPAD are summarized in the Table 1.

**Table 1　Model parameters for the simulated SPAD Devices**
**表 1　仿真 SPAD 器件的模型参数**

| parameters | |
|---|---|
| $V_{BR}$ | 15.2 V |
| $C_P$ | 500 fF |
| $C_d$ | 322 fF |
| $I_{sat}$ | 10 mA |
| $I_{rev}$ | 1 nA |

Preparatory SPECTRE simulations of the used model is executed and the simulation results of *I-V* characteristic of the used piecewise linear model is shown in Fig. 2(b), incorporated with the theoretic piecewise linear *I-V* response.

## 2 Structure of SPAD

Based on the accurate circuit model, a set of low breakdown voltage SPADs with p-well guard ring demonstrating photon counting abilities have been designed. A GSMC 180 nm CIS technology has been selected for manufacturing the SPAD devices due to extremely high requirement of assembling compact integrated photoelectric

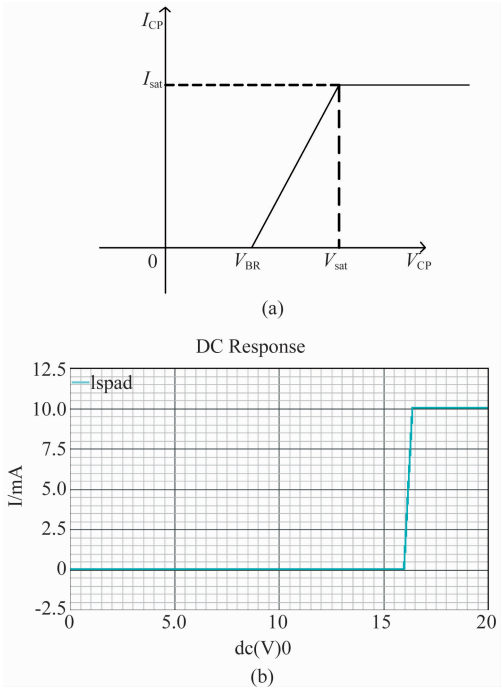


Fig. 2 (a) Theoretic piecewise linear *I-V* characteristic, (b) *I-V* characteristic of the model obtained through SPECTRE

图 2 (a)理论分段线性电压—电流特性曲线,(b)电学模型基于 SPECTRE 仿真的电压—电流特性曲线

detection circuit in SPAD fabrication .

As can be seen in Fig. 3, the SPAD consists of a P+/N-well junction and a circular virtual guard-ring which is made out of lightly doped P-well. A planar and shallow P+/N-well junction is used to define the active region for photon detection where charge multiplication occurs. The space charge region is achieved by diffusing the curved edge of the P+ implant into a surrounding P-well ring, so as to reduce electrical filed non-uniformities which can cause premature edge breakdown. Another N-type well is implanted with a deep N-well retrograde doping profile. The upward diffuse of doped atoms in the deep wafer improves the active region's ability of collecting charges. Note that the STI delimits the SPAD, while the P-well guard ring ensures that the electric field is maximized in the center of the device[9]. Moreover, all the non-active areas of SPAD are covered with the metal layers to avoid lighting, which can cause higher noise and higher after-pulsing probability.

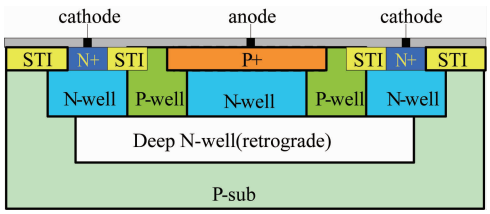


Fig. 3 The cross section of the designed SPAD

图 3 设计的 SPAD 横截面图

## 3 Passive quenching and actively quenching circuit

It is necessary to stop avalanche current to avoid destroying the SPAD device. Two kinds of quenching circuits are adopted to perform this quenching operation by promptly lowering the reverse bias voltage down to or below $V_{BR}$. Finally, the bias of the SPAD requires to be restored to its initial value to detect new incoming photon.

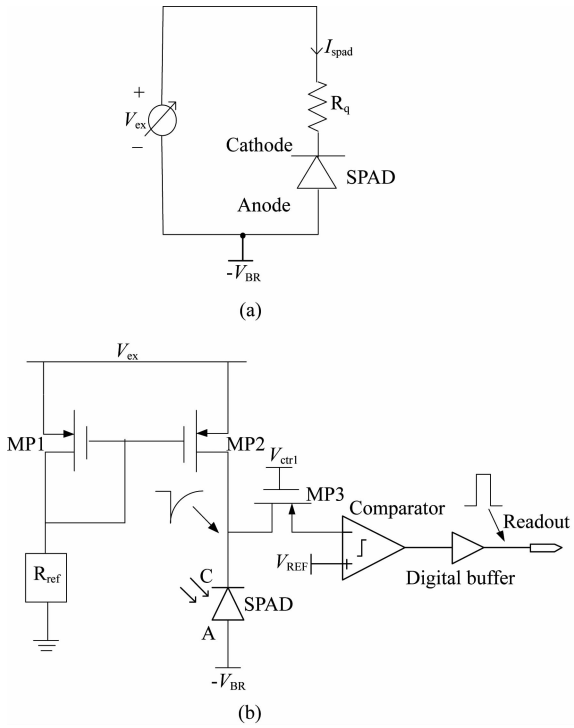


Fig. 4 (a) Passive quenching Circuit and (b) actively quenching circuit of the designed SPAD device

图 4 (a)设计的 SPAD 被动淬火电路,(b)设计的 SPAD 主动淬火电路

Particularly, a resistance in series with the SPAD makes up the simplest quenching circuit shown in Fig. 4 (a), implementing the so-called passive quenching electronics[10]. Due to the parasitic capacitances of the SPAD, by using a high value ballast resistance $R_q$, passive quenching leads to a small quenching time at the expense of a high resetting time and vice versa that a low value of the resistance improves the performance during the resetting phase at expense of the quenching time. In this case, optimum value of the ballast resistance about 100 kΩ is chosen to minimize the dead time.

Figure 4 (b) shows the schematic for the actively quenched SPAD[11], composed of a current mirror, an external resistor $R_{ref}$, a fast voltage comparator and a digital buffer followed by readout circuit. A simple PMOS current mirror is composed of transistor MP1 and MP2 with the current value set by $R_{ref}$, whose value is 100 kΩ. When no photon arrives, no current flows through the SPAD at this time, and the MP2 operates in the deep triode region. At this point, the source and drain voltage

of MP2 are both excess voltage '$V_{ex}$', and the voltage across the SPAD is $V_{ex}$ + $V_{BR}$. When an avalanche process occurs within the SPAD triggered by an incoming photon, the voltage across the SPAD immediately drops. In this case, MP2 now operates in the saturation zone and acts like a constant current source. If the internal resistance of the current source is so high that the voltage across the SPAD drops down to $V_{BR}$, then the avalanche will be stopped. The current for MP2 now recharges the internal depletion and parasitic capacitances and the circuit resets ready for detecting next photon. In addition, the output signal of SPAD's cathode passes through MP3 (when $V_{ctrl}$ is low) to fast comparator and compares with $V_{REF}$ ($V_{REF} < V_{ex}$). Finally, the output pulse of comparator buffered by digital buffers and can be read out .

## 4　Experimental results and analysis

Figure 5 shows the microphotograph of the circular SPAD fabricated in commercial GSMC 180 nm CIS technology with an 8 μm diameter active area[12].

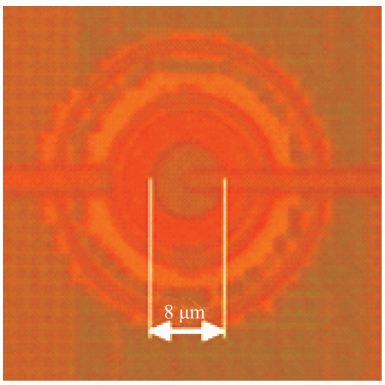


Fig. 5　Micro-photograph of the SPAD fabricated in GSMC 180 nm CIS technology
图 5　基于上海宏利 180 nm 图像传感器工艺的 SPAD 的显微镜照片

Figure 6 shows a test platform, which consists of three modules, A, B and C, representing DC power supply, digital oscilloscope and the designed SPAD with its quenching circuits respectively.

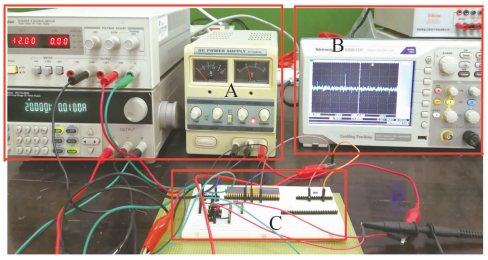


Fig. 6　Test platform of the SPAD with its quenching circuits
图 6　SPAD 及其淬火电路的测试平台图

### A. *I-V* characteristic

*I-V* characteristic simulation and measurement on the reverse biasing condition for the SPAD are performed at room temperature represented on Fig. 7.

It is easy to observe that the experimental data of the practical device is basically consistent with the simulation result of the used model in logarithmic coordinates. To be more specific, '$I_{spad}$' increases slowly until bias voltage reaches at 15.2 V in both of *I-V* curves, and then grows exponentially due to avalanche multiplication, and eventually trends to steady level. Therefore, it verifies the effectiveness of the accurate circuit model. Besides, this model can efficiently guide the design and manufacture of the actual device, which improves the rate of success of the design, and the actual device has been applied in the 3D image sensor.

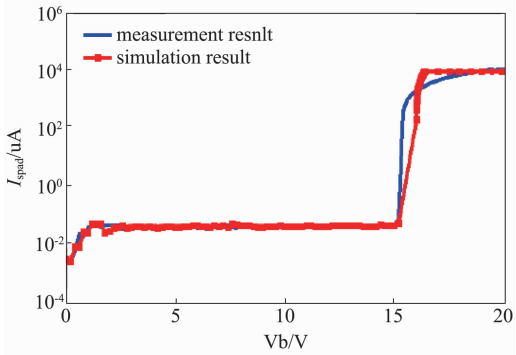


Fig. 7　Simulation result of the model and experimental data of SPAD developed by GSMC
图 7　SPAD 电学模型仿真结果与上海宏利制造的 SPAD 器件测试结果

### B. Quenching time

Figure 8 reports the sensor's cathode voltages after quenching using the two quenching circuits depicted in Figs. 4(a) and (b) respectively.

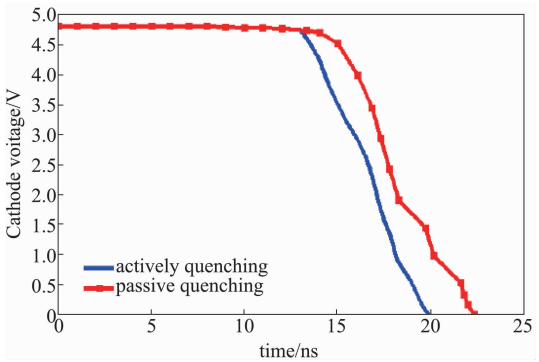


Fig. 8　SPAD's cathode voltages by using the actively quenching circuit and passive quenching circuit
图 8　使用主动和被动淬火电路的 SPAD 阴极电压值

As can be easily seen, setting $V_{ex}$ equal to 4.8 V, the SPAD device gives an actively quenching time of 7.9 ns against the result of 10.35 ns by using the passive quenching circuit. The actively quenched SPAD offers lower quenching time than passive quenching which is explained by the excess voltage producing a relative high

avalanche current, hence improving the speed performances.

**C. Dark count rate (DCR)**

The DCR measurement is conducted in the dark condition to count the number of avalanches pulse when the SPAD is reversely biased by a voltage larger than $V_{BR}$. The cathode of SPAD is connected to a high resolution oscilloscope as shown in Fig. 6 to count DCR with the excess bias voltage ranging from 0.5 V to 3.5 V at room temperature. The relationship of DCR and $V_{ex}$ is illustrated in Fig. 9. We can see that DCR increases linearly with the increase of excess bias voltage $V_{ex}$ which is mainly due to the band-to-band tunneling and trap-assisted tunneling carrier generation. When $V_{ex}$ increases from 0.5 to 3.5V, the DCR of our designed SPAD varies from 0.085 kHz/μm$^2$ to 2.5 kHz/μm$^2$ much lower than the DCR of 100 kHz in Ref. [13], which means our design benefits from rare trap center.

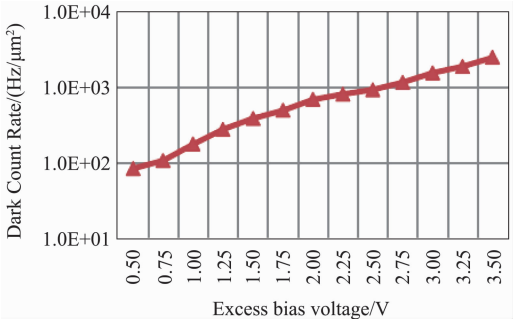


Fig. 9 DCR of the SPAD at different excess bias voltage

图 9 在不同的过偏置电压下的 SPAD 的暗计数率

**D. Photon Detection Probability (PDP)**

As illustrated in Fig. 5, the breakdown voltage (15.2 V) indicates that the depletion region is relatively thick, and it is also helpful to enhance the spectral response in some degree.

A SPAD's sensitivity to incident photons is characterized by the PDP that quantifies the probabilities that a photon impinging on the detection triggers avalanche. The PDP measurements conduct at 0.5 V, 2.5 V and 5 V of excess bias voltage ($V_{ex}$) to check that the p+/n-well SPAD works without edge breakdown. It achieves PDP of 15.7 % from 470 nm to 680 nm at $V_{ex}$ of 5 V as shown in Fig. 10 (a), which is wider than previous work[14] in standard CMOS technology. Additionally, it shows that the larger the $V_{ex}$ is, the higher PDP of the device at room temperature for blue led, green led and red led is, as depicted in Fig. 10(b). Especially, the most sensitive band for detection is 540 nm with the designed SPAD.

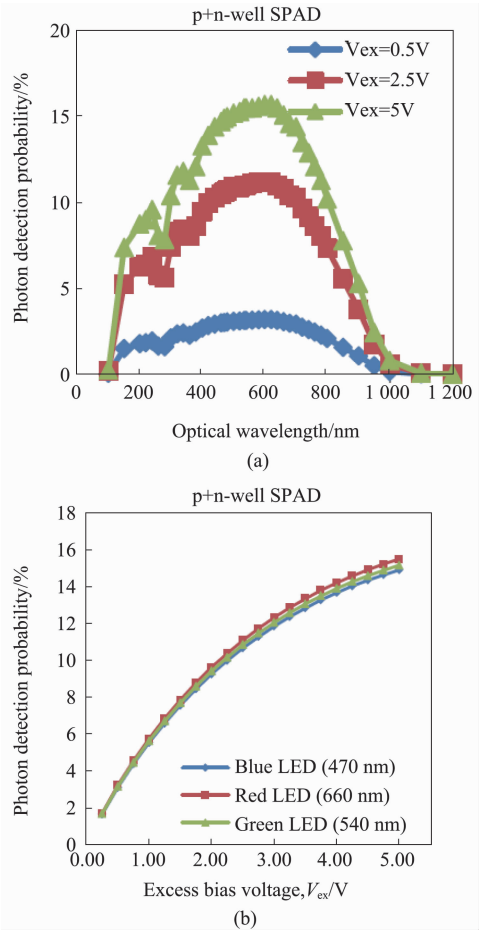


Fig. 10 (a) PDP of the designed SPAD versus wavelength; (b) PDP of the designed SPAD versus excess bias voltage

图 10 (a)设计的 SPAD 在不同波段下的光子探测概率 (b)设计的 SPAD 在不同的过偏置电压下的光子探测概率

## 5 Conclusion

A SPAD chip can in companion with actively quenching circuit implemented in GSMC 180 nm CIS technology is presented. The accurate model is implemented through a mixed circuital/behaviors description which includes generic analog circuit elements and Verilog-A codes. The experimental data extracted from practical devices developed by GSMC Microelectronics exhibited superb fitting with the SPECTRE simulation results of the model. A piecewise linear approximation is used to emulate the realistic *I-V* curve, which greatly improves the simulation accuracy. Moreover, the high performance SPADs with an 8 μm diameter active area are able to achieve low breakdown voltage of 15.2 V and quenching time of 7.9 ns. It realizes the goals that DCR can range from 0.085 to 2.5 kHz/μm$^2$ within 3.5 V excess voltage and that the PDP is 15.7 % from 470 nm to 680 nm at 5 V excess voltage. Thus, the performance improvements in the fabrication of CMOS avalanche photon diodes create the opportunity to integrate these low voltage and ultra-fast SPAD arrays with readout circuits in the 3D image sensor.

## References

[1] Betta G F D, Pancheri L, Stoppa D, *et al*. Avalanche Photodiodes in Submicron CMOS Technologies for High-Sensitivity Imaging[M], Advances in Photodiodes. InTech, 2011: 1253 - 1272.

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方法选择的波段子集相比,本文方法得到的波段子集具有更优越的异常检测性能.

## References


[1] Wang S, Chang C I. Variable-number variable-band selection for feature characterization in hyperspectral signatures [J]. *IEEE Transactions on Geoscience and Remote Sensing*, 2007, **45**(9):2979 - 2992.

[2] Jia S, Ji Z, Qian Y. Unsupervised band selection for hyperspectral imagery classification without manual band removal [J]. *IEEE Journal of Selected Topics in Applied Earth Observations and Remote Sensing*, 2012, **5**(2): 531 - 543.

[3] LIU Xue-Song, GE Liang, WANG Bin, *et al*. An unsupervised band selection algorithm for hyperspectral imagery based on maximal information [J]. *J. Infrared Millim. Waves*(刘雪松, 葛亮, 王斌, 等. 基于最大信息量的高光谱遥感图像无监督波段选择方法. **红外与毫米波学报**), 2012, **31**(2):166 - 170.

[4] Pal M, Foody G M. Feature selection for classification of hyperspectral data by SVM [J]. *IEEE Transactions on Geoscience and Remote Sensing*, 2010, **48**(5):2297 - 2307.

[5] LIU Chun-Hong, ZHAO Chun-Hui, ZHANG Ling-Yan. A new method of hyperspectral remote sensing image dimensional reduction [J]. *Journal of Image and Graphics*(刘春红, 赵春晖, 张凌雁. 一种新的高光谱遥感图像降维方法. **中国图象图形学报**), 2005, **10**(2):218 - 222.

[6] Yang H, Du Q, Chen G. Unsupervised hyperspectral band selection using graphics processing units [J]. *IEEE Journal of Selected Topics in Applied Earth Observations and Remote Sensing*, 2011, **4**(3):660 - 668.

[7] Chang C I, Du Q, Sun T L, *et al*. A joint band prioritization and band-decorrelation approach to band selection for hyperspectral image classification [J]. *IEEE Transactions on Geoscience and Remote Sensing*, 1999, **37**(6):2631 - 2641.

[8] Sun K, Geng X, Ji L. An efficient unsupervised band selection method based on an autocorrelation matrix for a hyperspectral image [J]. *International Journal of Remote Sensing*, 2014, **35**(21):7458 - 7476.

[9] FANG Shuai, QU Chneg-Jia, YANG Xue-Zhi, *et al*. Linear prediction band selection based on optimal combination factors[J]. *Journal of Image and Graphics*(方帅, 瞿成佳, 杨学志, 等. 组合因子最优的线性预测波段选择. **中国图象图形学报**), 2016, **21**(2):255 - 262.

[10] Dai W, Milenkovic O. Subspace pursuit for compressive sensing signal reconstruction [J]. I*EEE Transactions on Information Theory*, 2009, **55**(5):2230 - 2249.

[11] Von L U. A tutorial on spectral clustering[J]. *Statistics and Computing*, 2007, **17**(4):395 - 416.

[12] QIN Fang-Pu, ZHANG Ai-Wu, WANG Shu-Min, *et al*. Hyperspectral band selection based on spectral clustering and inter-class separability factor [J]. *Spectroscopy and Spectral Analysis*(秦方普, 张爱武, 王书民, 等. 基于谱聚类与类间可分性因子的高光谱波段选择. **光谱学与光谱分析**), 2015, **35**(5):1357 - 1364.

[13] TIAN Yei, ZHAO Chun-Hui, JI Ya-Xin. The principal component analysis applied to hyperspectral remote sensing image dimensional reduction[J]. *Natural Sciences Journal of Harbin Normal University*(田野, 赵春晖, 季亚新. 主成分分析在高光谱遥感图像降维中的应用. **哈尔滨师范大学自然科学学报**), 2007, **23**(5): 58 - 60.

[14] CHEN Hong-Da, PU Han-Ye, WANG Bin, *et al*. Image Euclidean distance-based manifold dimensionality reduction algorithm for hyperspectral imagery [J]. *J. Infrared Millim. Waves*(陈宏达,普晗晔,王斌, 等. 基于图像欧氏距离的高光谱图像流形降维算法. **红外与毫米波学报**), 2013, **32**(5):450 - 455.

[15] ZHAO Chun-Hui, YAO Zhe-Feng. Local kernel RX algorithm-based hyperspectral real-time detection [J]. *J. Infrared Millim. Waves*(赵春晖,姚浙峰. 基于局部核 RX 算法的高光谱实时检测. **红外与毫米波学报**), 2016, **35**(6): 708 - 714.


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[2] Braga L H C. An8 × 16-pixel 92 k SPAD time-resolved sensor with on-pixel 64ps 12b TDC and 100 MS/s real-time energy histogramming in 0.13 μm CIS technology for PET/MRI applications [C]. IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers (ISSCC), 2013: 486 - 487.

[3] Maruyama Y, Blacksberg J, Charbon E. A 1024 × 8700ps time-gated SPAD line sensor for laser Raman spectroscopy and LIBS in space and rover-based planetary exploration[J]. in IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers (ISSCC), 2013,2:110 - 111.

[4] Zappa F, Lotito A, Giudice A C, *et al*. Monotithic active-quenching and active-reset circuit for single-photon avalanche detectors [J]. IEEE J. Solid-State Circuits, 2003, **38**(7), pp. 1298 - 1301.

[5] Mita R, Oliveri A, Palumbo G, *et al*. A novel model for single photon detectors[C]// IEEE International Conference on Electronics, Circuits and Systems. IEEE, 2008:1 - 4.

[6] Zappa F, Ghioni M, Cova S, *et al*. An integrated active-quenching circuit for single-photon avalanches diodes [J]. IEEE Trans. Instrum. Meas., 2000, **49**(6), 1167 - 1175.

[7] Zappa F, Tisa S, Gulinatti A, *et al*. Monolithic CMOS detector module for photon counting and picosecond timing[J]. Solid-State Device Research Conf., September 2004, 341 - 344.

[8] Haitz R H. Model for Electrical Behavior of a Microplasma[J]. J. Appl. Phys., 1964, **35**(5), pp. 1370 - 1376.

[9] Karami M A, Yoon H J, Charbon E. Single-photon Avalanche Diodes in sub-100 nm Standard CMOS Technologies[J]. *Proc. intl. image Sensor Workshop*, 2011, **28**(11):1738 - 1752.

[10] Chick S, Coath R, Sellahewa R, *et al*. Dead time compensation in CMOS single photon avalanche diodes with active quenching and external reset[J]. *IEEE Trans. Electron Devices*, 2014, **61**(8):2725 - 2731.

[11] Niclass C, Rochas A, Besse P A, *et al*. Design and characterization of a CMOS 3D image sensor based on single photon avalanche diodes [J]. IEEE J. Solid-State Circuits, 205,**40**(11): 1847 - 1854.

[12] Mandai S. A wide spectral range single-photon avalanche diode fabricated in an advanced 180 nm CMOS technology [J]. Opt. Express, 2012,**20**(6): 5849 - 5857.

[13] Niclass C, Gersbach M, Henderson R, *et al*. A Single Photon Avalanche Diode Implemented in 130-nm CMOS Technology[J]. IEEE Journal of Selected Topics in Quantum Electronics, 2007, 13(4): 863 - 869.

[14] Sun, Pengfei, Charbon E, Ishihara R. A Flexible Ultrathin-Body Single-Photon Avalanche Diode With Dual-Side Illumination [J]. Selected Topics in Quantum Electronics IEEE Journal of 2014, **20**(6):276 - 283.