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A 220 GHz high integration and high resolution detector

CUI Da-Sheng, DING Zheng-Zhi, HAO Hai-Dong, LV Xin

(Beijing Key Laboratory of Millimeter Wave and Terahertz Technology,
School of Information and Electrics, Beijing Institute of Technology, Beijing 100081, China)

Abstract: A high-integration detector which consists of a patch antenna, a matching circuit, schottky diodes (SBD) and lenses has been developed. The integration of detectors is increased obviously comparing with that of separated detectors by integrating antennas, matching circuits and SBD on a chip in SMIC 130 mm. To improve the directivity of the antenna on chip, the nylon lens with air cave was designed and optimized. The air cave in lens not only provides space for assembling but also reduces the size of lens. It was calculated through testing that the antenna gain at 220 GHz is 22 dB, in which the contribution of lens is about 20 dB. The tested responsivity of the detector can achieve 130-150 V/W and the noise equivalent power (NEP) is estimated to be 400～460 pW/$\sqrt{\text{Hz}}$.

Key words: terahertz detector, CMOS, Schottky diode, lens antenna
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一种高集成高空间分辨率220 GHz检波器

崔大圣, 丁正之, 郝海东, 吕 昕
(北京理工大学 信息与电子学院 毫米波与太赫兹技术北京市重点实验室,北京 100081)

摘要:设计了一种高集成检波器,其包含贴片天线、匹配电路、肖特基二极管和透镜.在中芯国际130 nm工艺下将天线、匹配电路、肖特基二极管集成到一个芯片上,检波器的集成度相比于分离式有了明显的提高.为增强片上天线的方向性,进行了带有空气腔的尼龙透镜的设计和优化.透镜上的空气腔不但提供了组装空间而且减小了透镜体积.通过测试,天线在220 GHz辐射增益为22 dB,其中透镜贡献约为20 dB.检波器测试得到的响应率可达到130～150 V/W,等效噪声功率计算为400～460 pW/$\sqrt{\text{Hz}}$.

关 键 词:太赫兹(THz)检波器;互补金属氧化物半导体工艺;肖特基二极管;透镜天线

中图分类号:TN454 **文献标识码**:A

Introduction

Terahertz technologies for potential applications such as concealed weapon detection, aviation assistance and high-speed wireless data communication attract more and more attentions[1-4]. In order to achieve these applications, a detector with excellent performance is required. As it is known for its low cost, high yield and high integration, the technology of CMOS is suitable for high-integration detectors. In 2004, the first THz detector was invented based on the plasma wave detection theory by Knap[5-6]. With the development of CMOS technology, the cutoff frequency of CMOS devices becomes higher and higher. With its excellent performance in terahertz detector, high-frequency SBD have attracted much attention. SBD with cutoff frequencies up to 1THz had been demonstrated on high-resistivity silicon substrates by growing a thin molecular beam epitaxial layer on top of n^+ layer[7]. Silicide was used to improve the conductivity of poly and n^+ regions in modern CMOS processes. Inspired by this technology, integrated detector chips containing antenna, matching circuit and SBD were designed and fabricated with 130 nm CMOS technology.

To improve the spatial resolution and sensitivity of detectors, lens antennas have been analyzed and designed. Traditional extended hemispherical lenses are usually mounted on back of the chip, which brings great difficulty to assembly due to the existence of silicon substrates[8]. A new type of air-cave lenses which not only provides space for front mounting but also reduces the size of the lens was designed and fabricated.

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Biography:CUI Da-Sheng, male, Shandong, China. Ph. D. Research area involves terahertz device and quasi-optical component. E-mail: dscui@bit.edu.cn

In this paper, integrated detector chips are designed with 130 nm CMOS technology. The lens antenna with air cave was simulated, optimized and machined by 3D printing. The measurement results including radiation patters, responsivity and noise equivalent power are presented.

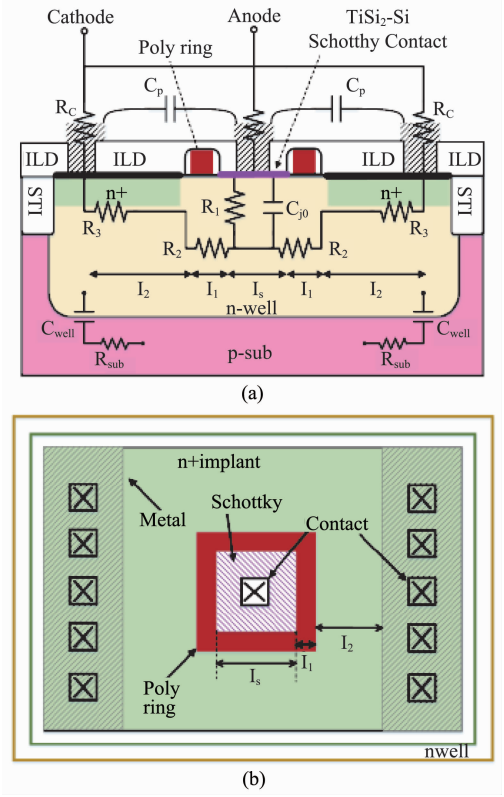

Fig. 1　(a) Cross-section of proposed SBD, and (b) equivalent cell layout
图 1　(a)肖特基二极管剖面图,(b)肖特基二极管版图示意

1　Design of the SBD

Figure 1 shows the cross-section and the equivalent cell layout of the proposed SBD. In order to realize shottky contact, poly-gate separation technology is used to separate anode and cathode, forming a shorter current path comparing with STI schottky diodes.

Zero-bias cut-off frequency of SBD is:

$$f_{co} = \frac{1}{2\pi R_s C_0} \quad , \quad (1)$$

where R_s is series resistance and C_0 is diode capacitance at zero bias. The expressions of R_s and C_0 are derived as below. Individual components contributing to R_s and C_0 are shown in Fig. 1.

$$R_s \approx R_1 + R_2 + R_3 + R_c \quad , \quad (2)$$

$$R_s \approx R_v + \frac{R_{nwell}}{28.6} + R_{poly}\left(\frac{l_1}{4l_s}\right) + R_{n^+}\left(\frac{l_2}{4(l_s + 2l_1)}\right) + R_c \quad , \quad (3)$$

$$C_0 = l_s^2 \sqrt{\frac{qN_D\varepsilon_{Si}}{2\phi_B}} + C_p \quad , \quad (4)$$

where, R_v is the vertical component of R_1, R_{nwell} is n-well sheet resistance, R_{poly} is the n-well sheet resistance under the poly separation ring, R_{n^+} is silicide n^+ sheet resistance, R_c is the overall of resistance of vias and contacts, N_D is n-well doping density, ε_{Si} is the permittivity of silicon, Φ_B is the built-in potential, and C_p is the parasitic capacitance of metal terminals. The factor of 1/28.6 is derived from the base-spreading resistance model in Ref. [9].

To increase f_{co}, the product of R_s and C_0 must be small. Equations 3 and 4 show that R_s is approximately proportional to $1/l_s$, while C_0 is proportional to l_s^2. This leads to a conclusion that maximum f_{co} is acquired when the minimum allowable length of l_s is chosen. Other design parameters include l_1 and l_2, which determine the value of R_s. Since the sheet resistance R_{poly} is higher than R_{n^+}, l_1 is set to a minimum length allowed by the design rule. R_s can be further lowered by decreasing l_2, however, since anode metal is getting closer to cathode metal, this will increase the side-wall capacitance C_p. The design parameters of SBD are: $l_s = 0.38$ μm, $l_1 = 0.13$ um, $l_2 = 1$ μm.

The designed schottky diodes were fabricated in SMIC 130 nm RF process and the DC characteristics were measured by using Agilent B1500 A semiconductor parameter analyzer. The ideality factor and barrier heights of these devices can be computed based on the thermionic emission model[10]. The designed devices have an ideality factor of 1.34, a barrier height of 0.42 eV and a turn on voltage of 0.4 V. The reverse leakage current is about 1 μA at 0.6V reverse bias, which can be tolerated if the diode is used in the forward bias region. The S-parameters were measured by using Agilent E8363B vector network analyzer. The series resistance (R_s) and diode capacitance (C_0) of the 8 cells SBD are 25 Ω and 4fF respectively. The cut-off frequency of the designed SBD is about 1.5 THz, which meets the requirements for THz detectors.

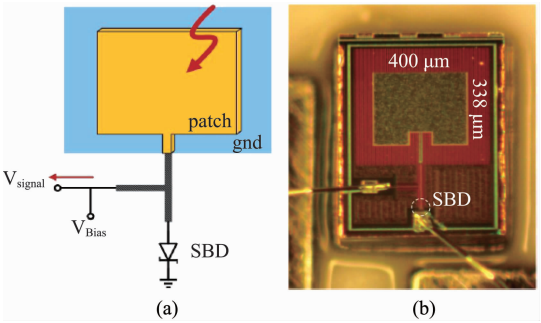

Fig. 2　(a) Schematic of the integrated detector chip, (b) photo of the integrated detector chip
图 2　(a)集成检波芯片结构示意图,(b)集成检波芯片照片

2 Integrated detector chips

Figure 2 shows the structure and photo of integrated detector chips. An antenna, a matching circuit and SBD are integrated into a chip. The patch antenna receives electromagnetic wave, the matching circuit achieves impedance matching and provides signal and offset channels, and the SBD works in forward bias state as a mixer device. As direct-current bias, V_{Bias} has direct impact on responsivity. Considering that the junction resistance (R_j) of the diode is too large (about 700 kΩ) in the zero bias state, it is difficult to perform effective power matching with such a large junction resistance. In addition, the oversized R_j also forms a low-frequency pole along with the parasitic capacitance, which affects the bandwidth of the detector. Based on these two points, a positive bias is applied to the diode in practical applications. In the experiment, the bias voltage is selected as the turn-on voltage of the diode. Comparing with traditionally separated detectors, the integration of designed detectors improve observably with the existence of integrated chips, which reduces the transmission loss and is conducive to the realization of array.

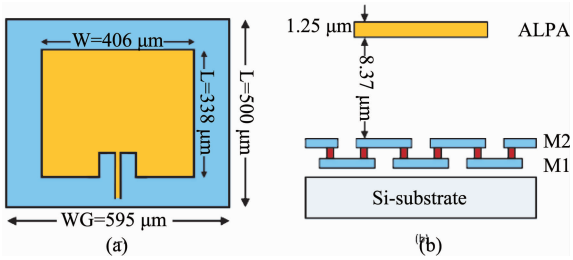

Fig. 3 (a) Planform of the patch antenna, and (b) cross-section of the patch antenna
图 3 (a)贴片天线俯视图,(b)贴片天线剖面图

Figure 3 shows the structure and size of the patch antenna. The patch antenna has good radiation directivity, and its structure is suitable for CMOS process. A large area of metal is no allowed by design rules. Therefore, the first and second layers of metal are assembled to form ground. And the ALPA is designed to be a patch to ensure the maximum dielectric thickness, which can improve the gain of patch antennas. Hollow in ALPA is designed to regulate the impedance of patch antenna. In order to reduce the transmission loss, a matching circuit is necessary, which is shown in Fig. 4.

Grounded coplanar waveguide (GCPW) was chosen as transmission line, and its impedance is set to 74 Ω after simulation and optimization. In this situation, the width of signal line is 3um and the distance of metal wall is 44 μm. The detailed values of the matching circuit are L1 = 85 μm, L2 = 100 μm, L_3 = 85 μm respectively.

3 Lens with air cave

Integrated lens antennas are wildly used in terahertz imaging field so as to improve the gain and resolution. Figure5 shows two types of integrated lens antennas.

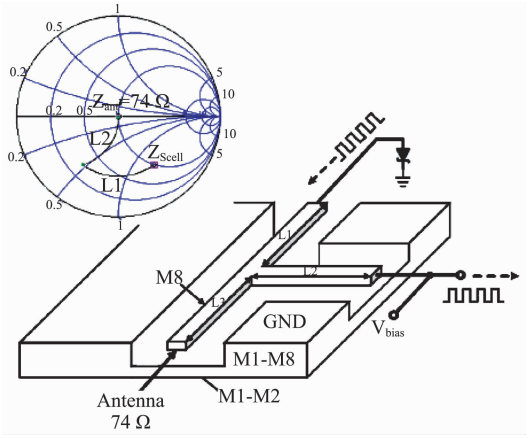

Fig. 4 Structure of matching circuit
图 4 匹配电路结构示意图

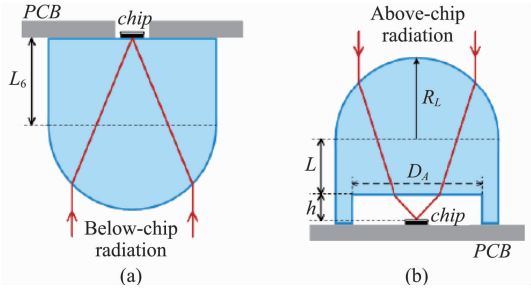

Fig. 5 (a) Below-chip configuration, and (b) above-chip configuration
图 5 (a)芯片背部组装,(b)芯片正面组装

Comparing with the below-chip configured lenses, above-chip configured lenses can be assembled easily with the existence of air caves. Moreover, the size of lenses in above-chip configuration can be shortened, which is helpful to the integration of detectors. Therefore, lenses with air caves are optimized with ray tracing technique, and the results are shown in Fig. 6.

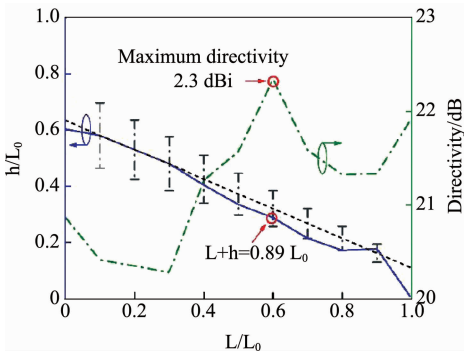

Fig. 6 Optimization design of height of lens air cave
图 6 透镜空气腔高度优化

where h, L, L_0 are defined as the same as in Fig. 5. Material of lens is nylon (ε_r = 2.68). The dotted line

means a theoretical value of h from 2-D ray tracing technique. To find optimal parameters of lenses, the studied range of h variation is around the initial value when L is defined. The solid line shows the optimal value of h and the dash dot line is the directivity of every optimal h. For the purpose of generalization, all geometrical parameters are normalized by the extension length of conventional lens, L_0.

The final parameters of lens are listed as below:

Table 1　Design parameter of lens with air cave
表 1　空气腔透镜设计参数

Parameters	R_L	L	D_A	h
Unit /mm	6.5	4	6	2

4　Test and analysis of the detector

Figure 7 shows the measurement setup of the proposed detector. A multiplier chain driven by signal source (Agilent E8257D) is used to generate a 12 dBm output at 220 GHz. A receiver is placed 30mm away from a transmitting horn. And a lock-in amplifier measures the rms value of output voltage for the detector and generates 1M signals for amplitude-modulation (AM) at 220 GHz. The DC drifts and low frequency noise 1/f are eliminated.

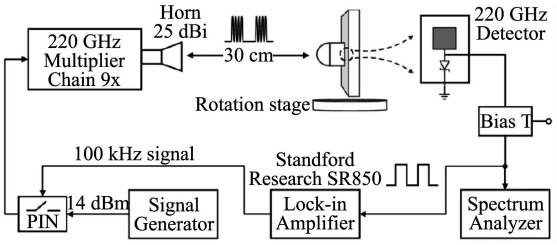

Fig. 7　The 220 GHz integrated detector measurement set-up
图 7　220 GHz 集成检波单元测试结构图

Responsivity reflects the input-output gain of a detector system. Based on Friis Transmission Equation, the voltage responsivity is[11]:

$$R_v = \frac{v_{\text{out}}}{P_{\text{in}}} = \frac{\frac{\pi}{\sqrt{2}}V_{\text{rms}}}{A_R \frac{P_{\text{cw}} G_{\text{T}}}{4\pi d^2}} \quad , \quad (5)$$

where, V_{rms} is the detector output recorded by lock-in amplifier, P_{cw} is the output power of multiplier chain, d is distance between the source and the detector, G_{T} is the gain of transmitting antennas and A_{R} is the effective aperture of detector antennas, which is calculated from the simulated directivity.

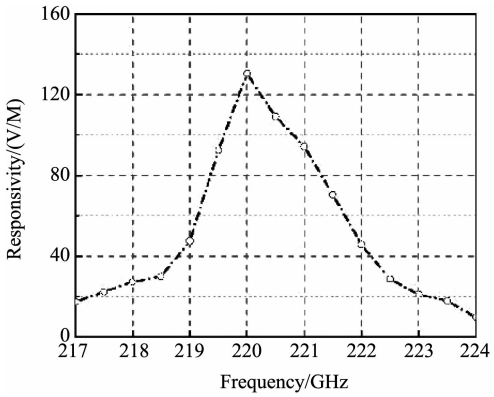

Fig. 8　Responsivity of only-patch detector
图 8　仅有贴片天线的检波单元响应率测试结果

For only-patch configuration, the AR is 0.5 mm^2, G_{T} is 20 dBi, and P_{cw} can be obtained by calibration. The measured peak responsivity is 130 V/W while the distance (d) is 20 cm, shown in Fig. 8. The output voltage of the with-lens detector increase by 20 dB, but the improvement of the responsivity is not improved although the effective aperture of the lens structure is greatly improved compared with the pure antenna structure, which responsivity is 150 V/W.

The NEP of detectors can be calculated by the following formula:

$$\text{NEP} \approx \frac{\sqrt{4kTB(R_{\text{s}} + R_{\text{d}})}}{R_{\text{v}}} \quad . \quad (6)$$

The NEP of only-patch and with-lens detector are 400 and 460 pW/$\sqrt{\text{Hz}}$, respectively.

The radiation pattern of patch antennas and integrated lens antennas are measured as shown in Fig. 9. Both antennas demonstrate very close performance, in spite of a slight difference in the sidelobe of the integrated lens antenna. It can be easily proved that the difference is caused by potting.

Based on the above results, Fig. 10 shows the prin-

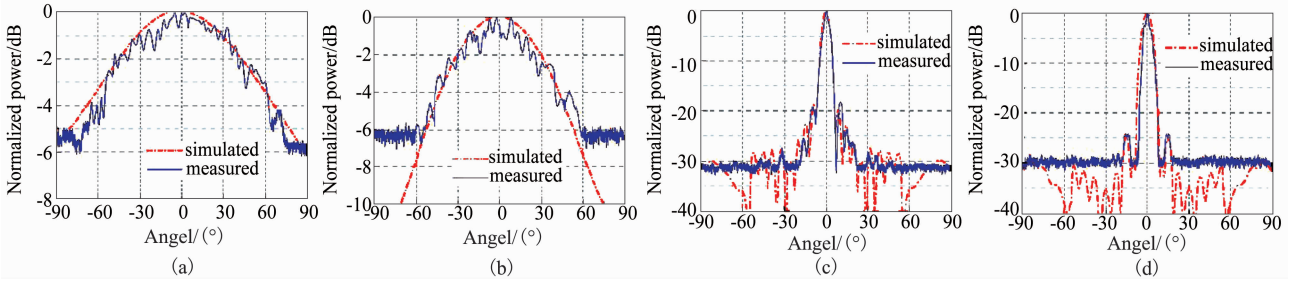

Fig. 9　Simulated and measured radiation pattern of detector (a) E-plane of the patch antenna, (b) H-plane of the patch antenna, (c) E-plane of the lens antenna, (d) H-plane of the lens antenna
图 9　检波单元仿测方向图(a)贴片天线 E 面,(b)贴片天线 H 面,(c)透镜天线 E 面,(d)透镜天线 H 面

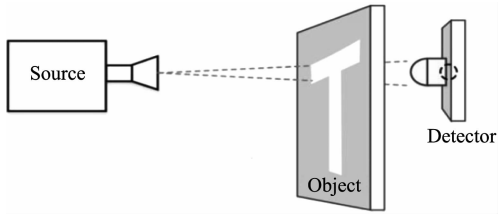

Fig. 10 Principle of imaging experimental
图 10 成像实验原理

ciple of imaging experimental. The imaging object is a 15 cm × 15 cm metal square with T shape hole, which moves with the 2D guide screw to achieve scanning. The detector is separated from the object by 5 cm, which means the resolution is 0.5 cm × 0.5 cm. The imaging result is shown as below:

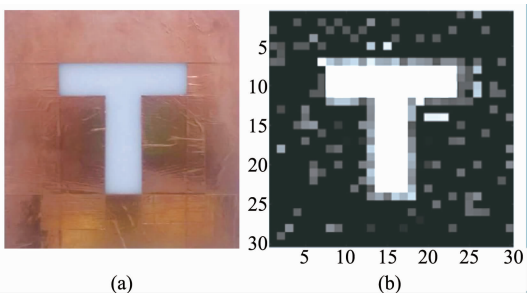

Fig. 11 (a) 15 cm × 15 cm metal square with T shape hole, and (b) imaging result
图 11 (a)15 cm × 15 cm 带 T 型孔的金属矩形,(b)成像结果

5 Conclusion

A high-integration detector has been designed and fabricated based on a patch antenna chip integrated Schottky diode in CMOS. The antenna radiation pattern and responsivity of the detector were measured at 220 GHz. The lens antenna is simulated and designed to improve the resolution of detectors. An ideal result was obtained in imaging experiments.

References

[1] Huang J, Zhao Q. A W - band monolithic broadwidth frequency multiplier on millimeter Schottky diode and metamaterial[J]. *Microwave & Optical Technology Letters*, 2015, **57**(3):525 - 530.

[2] Zhu M, Li X, Chung S, *et al*. Photo-induced selective gas detection based on reduced graphene oxide/Si Schottky diode[J]. *Carbon*, 2015, **84**(1):138 - 145.

[3] Viegas C, Alderman B, Powell J, *et al*. Characterization of 94 GHz and 183 GHz planar schottky diode based radiometer modules[C]// IEEE Mtt-S International Microwave and Rf Conference. IEEE, 2015: 296 - 299.

[4] Mou J, Guo D, Xue Q, *et al*. THz mixtenna chips and quasi-optical mixers for focal plane imaging applications[C]// International Conference on Infrared, Millimeter, and Terahertz Waves. IEEE, 2015: 1 - 1.

[5] Knap W, Teppe F, Meziani Y, *et al*. Plasma wave detection of subterahertz and terahertz radiation by silicon field-effect transistors[J]. *Applied Physics Letters*, 2004, **85**(85):675 - 677.

[6] Tauk R, Teppe F, Boubanga S, *et al*. Plasma wave detection of terahertz radiation by silicon field effects transistors: Responsivity and noise equivalent power[J]. *Applied Physics Letters*, 2006, **89**(25): 253511 - 253511 - 3.

[7] Huang F J, O K K. Metal-oxide semiconductor field-effect transistors using Schottky barrier drains[J]. *Electronics Letters*, 1997, **33**(15): 1341 - 1342.

[8] Godi G, Sauleau R, Thouroude D. Performance of reduced size substrate lens antennas for Millimeter-wave communications[J]. *IEEE Transactions on Antennas & Propagation*, 2005, **53**(4):1278 - 1286.

[9] Rein H, Schroter M. Base spreading resistance of square-emitter transistors and its dependence on current crowding[J]. *IEEE Transactions on Electron Devices*, 1989, **36**(4):770 - 773.

[10] Liu C, Li F. Determination of Schottky barrier height independent on temperature via reverse current - reverse voltage and temperature[J]. *Computational Materials Science*, 2015, **107**:170 - 174.

[11] Han R, Zhang Y, Coquillat D, *et al*. A 280 GHz Schottky diode detector in 130 nm digital CMOS[J]. *IEEE Journal of Solid-State Circuits*, 2010, **46**(11):2602 - 2612.