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86 mV/dec subthreshold swing of back-gated MoS_2 FET on SiO_2

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Abstract: Back-gated (BG) Multi-layer MoS_2 field effect transistors (FETs) have been fabricated on SiO_2/Si (P^{++}) substrate and electrically characterized. By optimizing the fabrication process and scaling down the SiO_2 thickness to 10 nm, the device exhibit excellent switching performance with a subthreshold swing of 86 mV/dec and an I_{on}/I_{off} ratio $\sim 10^7$. The little hysteresis and small SS jointly suggest tiny magnitude of interface traps or attached oxidants. The noise current induced by gate leakage can affect the measured switch ratio by overwhelming the effective I_{off} current defined by V_{DS}. According to the behaviors of MoS_2 FETs expressed by this work and others', BG devices with SiO_2 insulator present good performance and valuable potentials underutilized for rich applications.

Key words: MoS_2 FETs, excellent subthreshold swing, SiO_2 dielectric, interface state density
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具有86 mV/dec亚阈值摆幅的MoS_2/SiO_2场效应晶体管

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摘要:在SiO_2/Si(P^{++})衬底上制备了多层MoS2背栅器件并进行了测试.通过合理优化和采用10 nm SiO_2栅氧,得到了良好的亚阈值摆幅86 mV/dec和约10^7倍的电流开关比.该器件具有较小的亚阈值摆幅和较小的回滞幅度,表明该器件具有较少的界面态/氧化物基团吸附物.由栅极漏电造成的漏极电流噪声淹没了该器件在小电流($\sim 10^{-13}$ A)处的信号,限制了其开关比测量范围.基于本文以及前人工作中MoS_2器件的表现,基于薄层SiO_2栅氧的MoS_2器件表现出了良好的性能和潜力,显示出丰富的应用前景.

关 键 词:MoS_2场效应晶体管;良好的亚阈值斜率;SiO_2栅介质;界面态密度

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Introduction

Molybdenum disulfide (MoS_2), as a layered material with atomic thickness and proper bandgap (1.2 eV for multilayers and 1.8 eV for monolayer)[1], has attracted considerable attention for the possibility to extend Moore's law in coming decades[2-3]. MoS_2 is also a potential 2D semiconductor for bio-sensor[4], optical devices[5] and flexible circuits[6-7]. While monolayer MoS_2 with a thickness of 0.65 nm[8] shows good availability in nanoscale devices and optical applications, multi-layer MoS_2 with a certain thickness exhibits higher mobility and better immunity to circumstance-induced scatterings[9-10]. In early studies, thermally grown SiO_2 with a thickness of 300 nm, which is in purple color, was proved a good substrate for spotting the layer number of a MoS_2 membrane exfoliated on it[11]. Thus the following researchers usually choose 300-nm SiO_2 as the dielectric in fabricating BG mono/multi-layer MoS_2 FETs[12-14] to study the electrical characteristics of MoS_2 in different applications. Nevertheless, SiO_2 has not been chosen as the top gate oxide when preparing top-gated (TG) FETs with sandwiched MoS_2 membranes, but high-κ dielectric instead. Such device with single-layer MoS_2 surrounded by SiO_2 and HfO_2 has exhibited a high I_{on}/I_{off} ratio $\sim 10^8$ and a very low *SS* at 74 mV/decade[15], which agrees with the theoretical prediction that high-κ surroundings could effectively screen the coulomb scattering from traps near the conducting channel[10]. As contrast, SiO_2-based MoS_2 devices are seemingly overmatched by a landslide when referring to subthreshold swing (*SS*)[14, 16-17], carrier mobility[18] and on-state current[19]. However, most comparisons above took place between TG/BG devices with thin high-κ insulators and BG devices with thick SiO_2 insulator, and the latter ones' MoS_2 channels are usually exposed to ambient environment. It's not fair to ideologically assume a poor outlook of SiO_2-based devices if the following points are noticed: i) *SS* closely relate with the equivalent oxide thickness (EOT), ii) coulomb scattering in SiO_2 circumstance will be decreased when increasing the MoS_2 layer number, iii) foreign impurities from the ambient will severely suppress the device's performance. Actually, a recent research predicted that high-κ dielectrics can increase the electron mobility of a 2D semiconductor only when the impurity density is very high, while clean samples surrounded by low-κ materials such as SiO_2 show a much higher electron mobility than in high-κ conditions[20]. Thus, comprehensive consideration should be made for MoS_2 devices in specific circumstances.

Compared with preparing high-κ dielectric by ALD (atomic layer deposition) or sol-gel method, it is easier to get a high-quality SiO_2 layer with a uniform thickness by thermal growth. SiO_2 with a stronger breakdown electric field than that of high-κ materials is suitable for high performance BG devices that widely used in bio-chemical sensors, optical detectors and other related researches, especially when the electrode pads are overlapped by the back gate, which increases the risk of dielectric breakdown and induces a non-negligible gate leakage.

In this work, BG MoS_2 FETs with SiO_2 dielectric of different thicknesses were fabricated. The device with a thin SiO_2 layer (10 nm) performs as well as some reported devices with high-κ oxide. An I_{on}/I_{off} ratio $\sim 10^7$ and a minimum *SS* at 86 mV/dec were achieved. It is the best *SS* value to our knowledge among those SiO_2-based BG MoS_2 FETs.

1 Device fabrication

SiO_2 layers of different thicknesses (10, 20, 30, 50, 100, 200 and 300 nm) were thermally grown on p^{++} doped silicon wafers ($\rho < 0.001\ \Omega \cdot cm$), and further confirmed by a SC620 ellipsometer. All the SiO_2 surfaces were treated by O_2 plasma for 5 mins to improve the surface adhesive force, and followed by mechanical exfoliation of MoS_2 films with a scotch tape. To get rid of the residual organic pollutant from the tape, we dipped the wafer in Acetone for 10 mins and in alcohol for 5mins. Considering that the source/drain metal with a low work function (WF) promotes small schottky barriers[19], we chose a 200 nm aluminum (WF ~4.2 eV) layer deposited by EBE (electron-beam evaporation) as the contact metal to the MoS_2 membrane. Next, 200℃ annealing in a forming gas for 2 hours was carried to further lower the contact barrier[21].

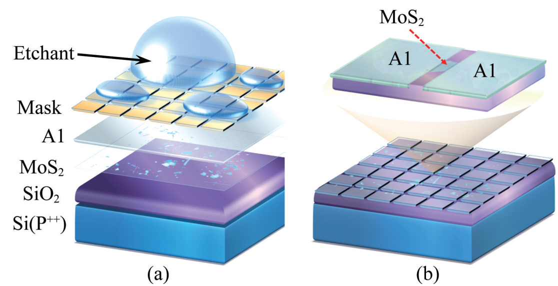

Fig. 1 (a) Fabrication processes of the BG multi-layer MoS_2 FETs. (b) Schematic of the finished chip
图 1 (a) 背栅多层 MoS_2 场效应晶体管制备流程,(b)制备完成的器件芯片

As shown in Fig. 1 (a), MoS_2 sheets of different shapes and thicknesses are randomly distributed on the SiO_2 surface. To expediently fabricate as many devices as possible, we designed a mask with thousands densely arranged square pads. According to the Buffon's needle experiment, a MoS_2 "needle" with several-microns scale will have a good possibility to be contacted by two Al pads. All the pads with 70-μm side lengths are separated by 3-μm-long channels. And all the pads were defined by ultra-violet lithography technology. Considering the MoS_2 films attached to the SiO_2 surface by Van der Waals force are easily to be washed away in a lift-off process, a mixed solution (10% DI water +5% nitric acid +5% acetic acid +80% phosphoric acid) was chosen to uniformly etch the Al metal that coated on the channel area.

As displayed in Fig. 1(b), devices with properly positioned MoS_2 sheets were selected with a Leica microscope. The thicknesses of these membranes were measured by a BRUKER AFM. In order to decrease the attached impurities[22-23], all the devices were placed in a vacuum chamber (10^{-4} mbar) for more than 24 hours before electrical characterization. The electrical tests with Agilent B1505 were finished in one hour after the chips' exposure to the ambient environment.

2 Results and discussion

Device with 11.17 nm (~17 layer) MoS_2 shown in Fig. 1 (a) was fabricated with a 10 nm SiO_2 layer. Figure 2 (b) displays the device's transfer characteristics with an I_{on}/I_{off} ratio ~10^7, a carrier mobility at 24.5 $cm^2/V \cdot s$ and a *SS* at 86 mV/dec. It is the best *SS* value to our knowledge among the reported SiO_2-based BG devices[12, 16, 24-29]. The testing process in Fig. 2(b) was carried in a dark chamber at $T = 300$ K, in a step of 0.05 V. The blue triangle shows the ideal *SS* slope. The interface state density (D_{it}) can be estimated by the following equation[30]:

$$SS = \frac{kT}{q}\ln(10) \times \left(1 + \frac{(C_S + C_{it})}{C_{OX}}\right) , \quad (1)$$

where k is the Boltzmann constant, T is the characterization temperature in Kelvin, C_S is the depletion capacitance of MoS_2, C_{it} is the MoS_2/SiO_2 interface state capacitance, and C_{OX} is the gate capacitance at 3.45×10^{-7} F/cm^2 (10 nm SiO_2). When V_G is near to the threshold voltage, C_s can be neglected compared with C_{it}. Thus, we can further get the effective interface state density by[31]

$$D_{it} = \frac{C_{it}}{q^2} \approx \left(\frac{qSS}{kT\ln(10)} - 1\right) \times \frac{C_{OX}}{q^2} . \quad (2)$$

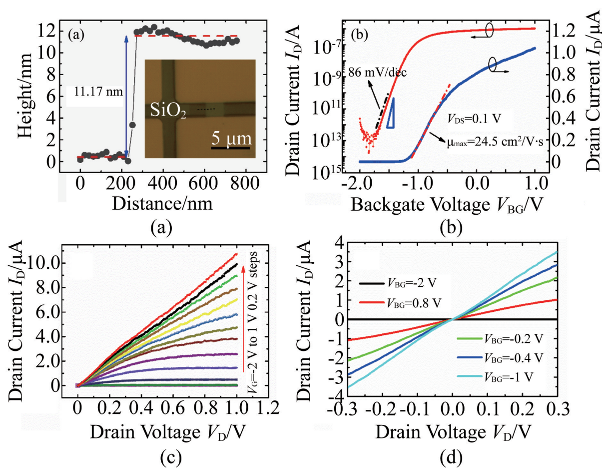

Fig. 2 (a) The optical image of the BG MoS_2 FET and a thickness scan along the dash line across the MoS_2 sheet. (b) Transfer characteristics, (c) Output characteristics, (d) The details of I_{DS}-V_D curves across the point of $V_D = 0$ V

图 2 (a) 背栅 MoS_2 场效应晶体管的光学图像,以及 MoS_2 薄膜的厚度扫描结果,(b) 转移特性曲线,(c) 输出特性曲线,(d) $V_D = 0$ V 附近的 I_DS-V_D 曲线

The interface state density D_{it} is calculated to be $9.55 \times 10^{11}/cm^2 \cdot eV$, which is a relatively low value among the previous works[1, 16, 18, 32], as indicating less coulomb scattering. A field effect mobility of 24.5 $cm^2/V \cdot s$ is extracted using[1]:

$$\mu = \left[\frac{dI_D}{dV_G}\right]_{max} \times \frac{L}{WC_{OX}V_D} , \quad (3)$$

where $L/W = 0.66$, $V_D = 0.1$ V. It is a conventional mobility among SiO_2-based BG MoS_2 devices[16, 24, 33]. However, the mobility is yet underestimated due to neglecting the contact resistance, which will be discussed subsequently.

The output characteristics with fixed back gate voltages were presented in Fig. 2(c), the current bending with an increasing V_D is induced by the pinch-off in MoS_2 channel. Before V_D reaches the pinch-off points, all the output curves arranged in Fig. 2(d) are almost linear, which suggests a good Al/MoS_2 contact. Nevertheless, a recent research indicates that the seemingly Ohmic contact could be a false appearance of a thermally assisted tunneling Schottky barrier[19]. According to the Fowler-Nordheim (FN) tunneling current function as described in Ref. [31], both the tunneling intensity and the resistance of Schottky barrier are V_{BG} dependent. We can briefly express the contact resistance as $R_c = R_m + R_s$, where R_c is the total resistance of the $Metal/MoS_2$ contacts, R_m is the voltage independent Ohmic resistance, R_s is the temperature/voltage dependent Schottky barrier resistance.

In a typical two-probe mobility measurement, the voltage dropping across the channel region will be overrated at the presence of R_c. By assuming that R_s varies little when the device is overdriven[35], the Y-function method developed by Ref. [34] and verified by Ref. [35] was applied to obtain the R_c. The resistance induced by source/drain contacts is extracted as 41.5 kΩ, or 221.2 Ω·mm. It is a relatively smaller value when compared with that of Refs. [36-38], but obviously higher than that of Refs. [19, 39], which suggest that the device's performance could be further improved by a forward decrease of R_c. Relevant researches have been developed by Refs. [19, 21, 40-42]. Finally, a modified mobility of 42.3 $cm^2/V \cdot s$ is deduced, 72.7% higher than the primary value calculated through the typical method.

For most BG MoS_2 FETS with their channel exposed to the ambient environment, hysteresis is commonly exist when taking two-direction gate sweeps. The hysteresis is mainly induced by the trapping and de-trapping processes dominated by the channel potential[43]. As exhibited in Fig. 3 (a), traps not only exist at the MoS_2/SiO_2 interface[29], but also forms at the upper face of the MoS_2 membrane with attached H_2O, O_2 and other impurity molecules by Van der Waals force or electrostatic force[44]. For devices fabricated in a rather clean environment, the hysteresis during tests is mainly induced by the foreign impurities from the ambient[16]. Interestingly, the dynamic balance of the absorption magnitude can be changed by the applied gate voltage[45]. Both the atta-

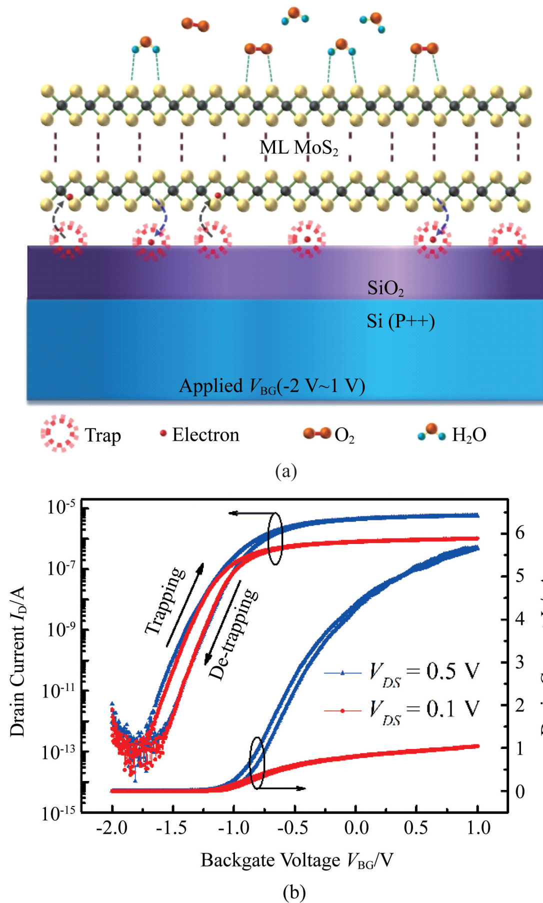

Fig. 3 (a) Schematic of the trap sources that cause hysteresis in two-direction gate sweeps. (b) Transfer characteristics of a two-direction sweep

图 3 (a) 在双向扫描中引起回滞的缺陷态,(b) 双向扫描的转移特性曲线

ched molecules and the interface traps act as an adjustable capacitance in series with the channel region and gate dielectric, thus bringing a shift to the transfer curves. The magnitude of voltage shift corresponds to the amount of traps. As presented in Fig. 3(b), the hysteresis width is 0.13 V at V_{DS} = 0.1 V, and expands as 0.17 V at V_{DS} = 0.5 V, where the device is measured in a dark chamber at 300 K, and the relative humidity is controlled under 30% [44]. The small hysteresis [16, 29, 43, 45] of our device indicates a mild influence induced by the trap-formed 'capacitance'. The expand of the hysteresis window at V_{DS} = 0.5 V might be jointly induced by the residual attachment from the 0.1 V test and an enhanced absorption of impurities in the 0.5 V test due to stronger electron current in MoS_2.

To eliminate the impurities attached to MoS_2 membrane, one can simply apply a negative voltage stress to the device, which would decrease the 'doping level' in MoS_2, therefore less polar molecules (water) or electrophilic molecules will keep sticking in the 2D MoS_2 layers[43]. A dryer atmosphere[44] or a vacuum testing environment also works in decreasing the hysteresis. Vacuum annealing would remove the foreign matter more thoroughly[22]. However, as long as the MoS_2 channel is exposed to ambient, the device's performance will be severely suppressed. It is better to coat a passivation layer or high-reduction-potential molecules over the channel region[14, 16, 46].

The gate induced drain noise (GIDN) was also taken into consideration. As shown in Fig. 4 (a), G stands for the conductance of each branch circuit. The adjustable resistances of the MoS_2 channel in Fig. 4 (a)

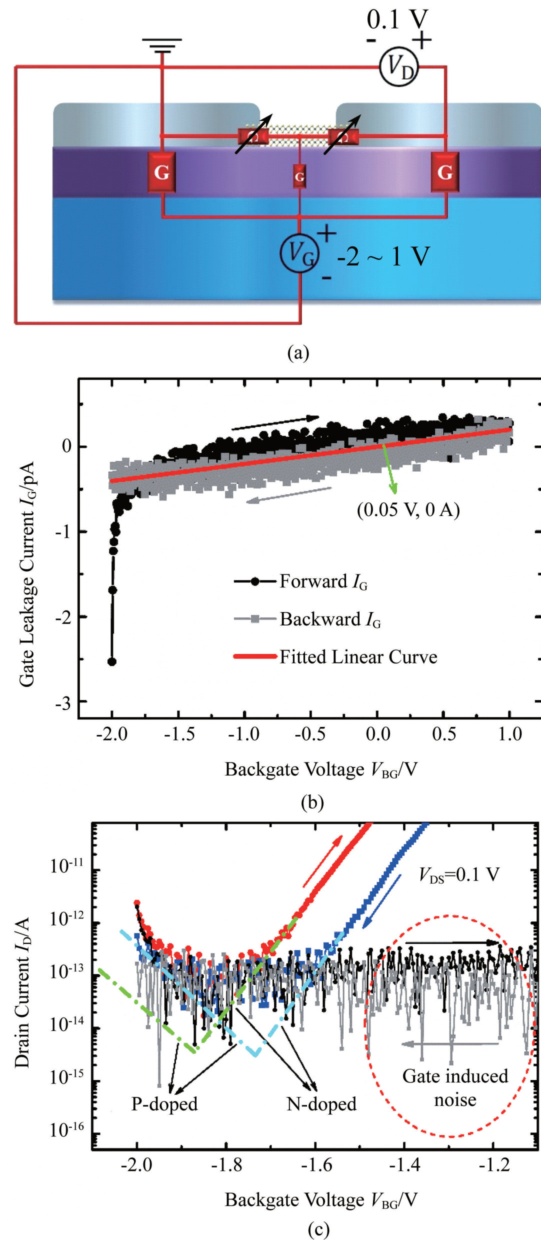

Fig. 4 (a) A simple circuit model of the gate leakage paths, (b) Gate leakage current in two sweep directions (black for forward and gray for backward) and the linear fitted curve, (c) Part of the drain current signal is swallowed by the gate induced noise at the off-state region

图 4 (a) 描述栅极漏电流的简单模型,(b) 两个方向扫描的栅极漏电(黑色代表正向,灰色代表反向),以及直线拟合电流,(c) 关断区域的部分漏极电流信号被栅致漏极噪声淹没

are the sums of the S/D contact resistances and the channel resistance. Most gate leakage in our device is induced by the overlap among two Al metal pads (70 μm × 70 μm) and the back gate. Considering the small area and high resistance of the MoS_2 sheet, the current between MoS_2 channel and back gate can be neglected. As displayed in Fig. 4 (b), I_D reaches ~10^{-12} A at the start points of the forward sweep. It is induced by a foreign pulse from the parasitic capacitance of the test system. Interestingly, a tiny hysteresis is also observed in the gate leakage of two directions, which could be a consequence of the altered tunneling conditions induced by trap movement in the SiO_2 layer[47]. However, the fitted linear curve calculated from the two-direction I_{BG} current rightly goes through the point (0.05 V, 0 A), where I_{DG} (the branch current from drain to backgate) compensates I_{SG} (the branch current from backgate to source). It will help us to confirm the circuit model in Fig. 4(a) (assuming $R_{SG} = R_{DG}$, R_{SG} and R_{DG} are the resistances between source/drain pad and backgate). Thus we can get a gate leakage density of 4.12 nA/cm^2 under a 2×10^8 V/m field, which suggests a good quality of the dielectric[18, 48-49]. We can further get the GIDN (I_{GIDN}) by

$$I_{GIDN} = -I_{BG} - \frac{V_S - V_{BG}}{R_{SG}} = \frac{V_{BG}}{R_{SG}} - I_{BG} \quad , \quad (4)$$

I_{GIDN} in two directions are presented in Fig. 4 (c), and the extended dash lines present the I_D signal of practical situation. The I_{on}/I_{off} ratio of our device is seemingly decreased by two orders. The gate leakage shrinks with less overlap area, thus the switch ratio will be further improved.

To further verify the influence of the dielectric thickness on the BG devices, devices with SiO_2 layers of different thicknesses were fabricated and characterized. The thicknesses of MoS_2 membranes vary from 5 nm to 35 nm. As presented in Fig. 5(a), *SS* degrades with increasing SiO_2 thickness. To intuitively make a comparison among the transfer curves, all the curves are rearranged by properly setting the V_{off} values. The extracted *SS* values from this work and other literatures ((SiO_2)[25, 26, 28-29, 50-51], (Al_2O_3)[7, 16, 52-54], (HfO_2)[18, 52, 55] and (HfTiO)[32]) are together displayed in Fig. 5(b). All the devices included are BG Multi-layer (3 ~ 50 nm) MoS_2 FETs with their channel exposed to the ambient. In Fig. 5(b), three fitted curves are extracted from Eq. 2, where C_s is assumed negligible and D_{it} values are set as 3×10^{11}, 2×10^{12} and 8×10^{12} $cm^{-2} \cdot eV^{-1}$. Given Eq. 1 and the assumption that C_S is negligible, we can simply deduce that:

$$SS \propto (1 + A \cdot D_{it} \cdot T_{OX}) \quad , \quad (5)$$

where T_{OX} is the thickness of the SiO_2 layer, A is constant coefficient. Thus the *SS* of a BG MoS_2 FET is mainly determined by the interface trap density and EOT. During a wide D_{it} range from 3×10^{11} to 8×10^{12} $cm^{-2} \cdot eV^{-1}$, a trend is observed in Fig. 5(b) that the *SS* value decreases when EOT becomes thinner. Interestingly, no obvious evidence is shown here that the D_{it} of MoS_2/SiO_2 interface is larger than that of MoS_2/high-κ dielectric interface. Ref. [54] concludes that the distribution of D_{it} and the peak of D_{it} at native MoS_2 MOS interfaces are not strongly dependent on the gate dielectrics. Since the attached impurities will introduce a hysteresis to the BG devices, the D_{it} calculated here is probably a sum of interface traps and channel attachments. Further studies should be developed to research the impact on *SS* brought by ambient impurities. In summary, the *SS* of a SiO_2-

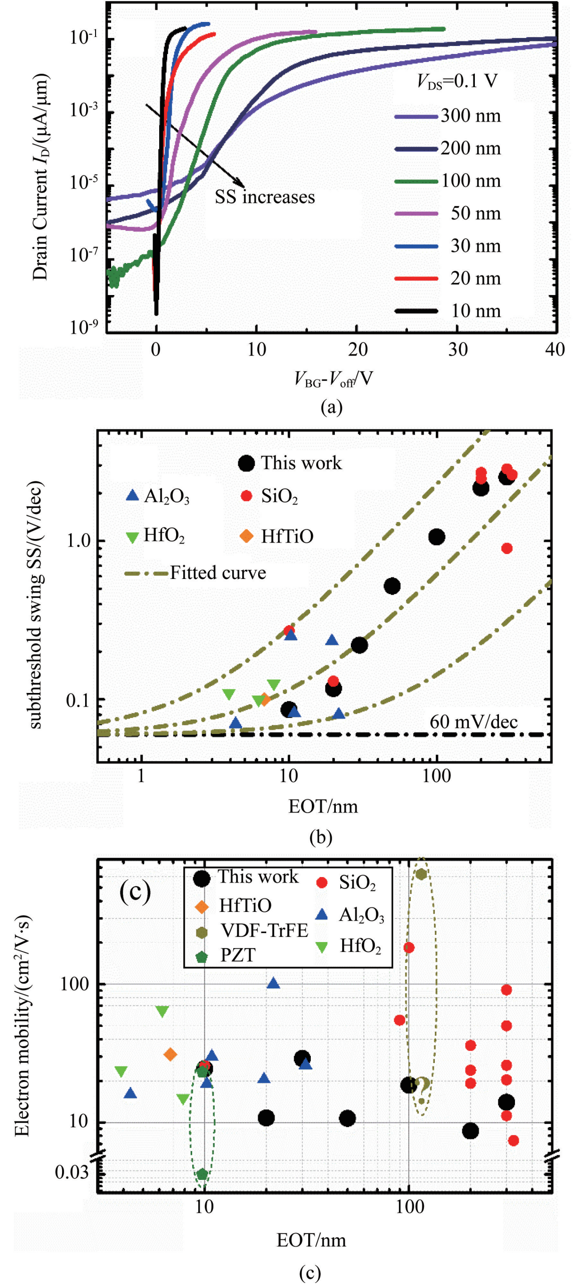

Fig. 5 (a) Transfer characteristics of BG ML-MoS_2 devices with different thickness of SiO_2 insulator, (b) *SS* as a function of EOT with different dielectric, (c) The mobility of BG MoS_2 devices with different dielectric

图 5 (a) 具有不同 SiO_2 介质厚度的背栅多层 MoS_2 器件的转移特性,(b) 亚阈值斜率与不同电介质的等效氧化层厚度(EOT)的关系,(c) 基于不同介质材料的背栅器件的迁移率

based BG device is possible to be properly shrunk.

Meanwhile, the mobility values of BG devices based on different dielectric have been displayed in Fig. 5(c), mobility values are from this work and Refs. [5, 13, 16, 18-19, 23, 28-29, 39, 50-51, 56] (SiO_2), Refs. [7, 16, 52-54, 57] (Al_2O_3), Refs. [18, 52, 55] (HfO_2), Ref. [32] (HfTiO), Ref. [58] (VDF-TrFE) and Ref. [59] (PZT). All the mobility values are extracted through a two-probe test, using Eq. 3. No obvious relationship was observed between EOT and mobility. Surprisingly, the mobility values of BG MoS_2 FETs based on high-κ dielectric are not distinctly higher than those of SiO_2-based devices, which is contrary to the previous results[18]. Generally, the contact resistance and the scattering rate are critical to a device's characteristics. Compared with the performance of devices based on low-κ dielectrics, a mobility of 184 $cm^2/V \cdot s$ (SiO_2) was reached by Ref. [19], owing to a rather small contact resistance and extremely low Schottky barrier. An average mobility of 305 $cm^2/V \cdot s$ (SiO_2) was observed in Ref. [13], where a four-probe test system was applied, thus the negative influence of contact resistance was eliminated. Both results above present a promising outlook for SiO_2-based MoS_2 FETs. For devices characterized by a two-probe testing system, Y-function method is proved effectively in extracting the real field effect mobility[35]. In the past works, the low tested mobilities of devices based on SiO_2 are probably suppressed by high level of impurities and poor metal/MoS_2 contacts. As predicted in Ref. [20], MoS_2 devices based on low-κ dielectrics may perform better than those based on high-κ dielectrics at room temperature, as long as the impurity level is reduced so that surface optical phonon scattering set the upper limit of carrier mobility.

In addition, devices with MoS_2 and ferroelectrics dielectrics have emerged recently. They have good potential in non-volatile memory and negative-capacitance transistors. The mobilitis versus different dielectrics (VDF-TrFE and PZT) are displayed in Fig. 5(c). Due to the domain switching in ferroelectric membrane, memory windows are formed with transfer curves in two directions going anticlockwise[58-59], thus two maximum mobility values can be extracted within one device. As presented in Ref. [59], these two mobility values differ greatly due to the change of ferroelectric polarization direction. While Ref. [58] only presents the higher mobility value, leaving the smaller one unknown.

3 Conclusion

In summary, back-gated multi-layer MoS_2 FETs based on different-thickness SiO_2 substrates have been fabricated and characterized. With the SiO_2 thickness scaling down to 10 nm, a minimum *SS* at 86 mV/dec has been achieved. As far as we know, it is the best *SS* value among the reported SiO_2-based BG devices. A mild hysteresis is observed in two direction sweeps, and it is mainly induced by the absorption/desorption process of impurities. The gate leakage of our device is very small, which suggests good electrical quality of the SiO_2 layer. When I_D reaches $\sim 10^{-13}$ A, the drain current signal is overwhelmed by GIDN, thus the switch ratio is underestimated. Smaller overlap area between Al pad and back gate will help to decrease GIDN. The SS and mobility are contrastively analyzed among the BG MoS_2 devices based on different oxide layers. Compared with D_{it}, EOT shows a stronger influence on *SS*. More important, no evidence is observed that high-κ dielectric is necessary in boosting the carrier mobility. The first thing before dielectric application in a MoS_2 FET is to consider the trade-off between impurity level and surface optical scattering. As discussed in this work, the MoS_2/SiO_2 system shows undeveloped potentials for further exploration.

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