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f_T = 220 GHz InAlN/GaN HFETs with regrown ohmic contacts

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Abstract: Scaled InAlN/GaN heterostructure field-effect transistors (HFETs) with high unity current gain cut-off frequency (f_T) on sapphire substrate were fabricated and characterized. In this device, scaled source-to-drain distance (L_{sd}) of 600 nm was realized by metal organic chemical vapor deposition (MOCVD) based on regrow non-alloyed n^+-GaN Ohmic contacts. Moreover, a 50 nm rectangular gate was fabricated by self-aligned-gate technology. A high drain saturation current density (I_{ds}) of 2.11 A/mm @ V_{gs} = 1 V and a peak extrinsic transconductance (g_m) of 609 mS/mm were achieved in the InAlN/GaN HFETs. In addition, from the small-signal RF measurements, the values of f_T and maximum oscillation frequency (f_{max}) for the device with 50-nm rectangular gate were extrapolated to be 220 GHz and 48 GHz. To our best knowledge, the value of f_T is the best reported one for InAlN/GaN HFETs in China.

Key words: InAlN/GaN, HFET, f_T, regrown n^+-GaN ohmic contacts

PACS: 85.30.De, 71.55.Eq, 85.30.Tv, 78.55.Cr

基于再生长欧姆接触工艺的220 GHz InAlN/GaN场效应晶体管

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摘要:在蓝宝石衬底上研制了具有高电流增益截止频率(f_T)的InAlN/GaN异质结场效应晶体管(HFETs).基于MOCVD外延n^+-GaN欧姆接触工艺实现了器件尺寸的缩小,有效源漏间距(L_{sd})缩小至600 nm.此外,采用自对准工艺制备了50 nm直栅.由于器件尺寸的缩小,V_{gs} = 1 V下器件最大饱和电流(I_{ds})达到2.11 A/mm,峰值跨导达到609 mS/mm.根据小信号测试结果,外推得到器件的f_T和最大振荡频率(f_{max})分别为220 GHz和48 GHz.据我们所知,该f_T值是目前国内InAlN/GaN HFETs器件报道的最高结果.

关 键 词:InAlN/GaN;HFET;f_T;再生长n^+-GaN欧姆接触

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Introduction

Attributed to the large electron velocity and high critical breakdown field, nitride heterostructures have attracted great attention for the excellent potential application in high-power and high-voltage operations at high frequency band[1-2]. In the last two decades, AlGaN/GaN heterostructure field-effect transistors (HFETs) have been extensively studied and made a great progress. Nowadays, the great advance in the performance of AlGaN/GaN HFETs have made possible the application solid-state high-power broadband power amplifiers (PA), covering L-band to W-band[3-5]. AlGaN/GaN HFETs, with their super characteristics, lead to PAs with high efficiency, large output power density, wide operational bandwidth and high linearity, which will promote the next generation of phased array radars, high-data-rate communication systems and active imagers.

However, once the size of devices is scaled to im-

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prove the RF characteristics, the short channel effects (SCEs) seriously disrupt in the conventional AlGaN/GaN HFETs, especially as the gate length below 100 nm. Since a relatively thick AlGaN barrier layer is necessary to induce enough two dimensional electron gas (2DEG) density between AlGaN barrier and GaN buffer layer, the barrier thickness reduction to suppress the SCEs is not feasible.[6] So far, the recorded unity current gain cut-off frequency (f_T) of AlGaN/ GaN HFETs is 225 GHz, but with a poor maximum oscillation frequency (f_{max}) of 120 GHz.[7] The application of AlGaN/GaN HFETs above W-band is facing challenge.

A lattice-matched $In_{0.17}Al_{0.83}N$/GaN heterostructure, having high 2DEG density with an ultra-thin barrier due to the strong spontaneous polarization, was proposed as an ideal alternative to overcome above challenges. To offer a solution to some of the strain-related device reliability, Kuzmík proposed an alternative lattice matched InAlN barrier for GaN-based HFETs,[8] since the defects induced by the lattice mismatch in the lattice matched hetero-junction with no piezoelectric polarization can be decreased, providing a better reliability. In the InAlN/GaN HFETs, thin InAlN barrier layer allows high ratio of gate length to barrier thickness as device scaling, which can effectively suppress the SCEs and improve the RF characteristics. In recent years, the frequency performance of InAlN/GaN HFETs has made outstanding progress with the new lattice matched heterostructures. 100-nm gate length lattice-matched InAlN/GaN HFETs showing f_T with 144 GHz (f_{max} = 137 GHz) were reported by Sun *et al*.[9] The same group reported a combined 205-GHz-f_T and 191-GHz-f_{max} in a 55-nm-gate-length InAlN/GaN HFET with a 10-nm top barrier.[10] RF transconductance (g_m) collapse was reduced by oxygen plasma treatment, and Lee *et al*. fabricated devices with high f_T of 245 GHz using gate length of 30 nm.[11] The same group introduced InGaN back barrier to suppress the SCEs, and achieved high f_T of 300 GHz using gate length of 30 nm.[12] A record f_T of 400 GHz was reported by Yue *et al*. using gate length of 30 nm in an ultrascaled InAlN/GaN HFET.[13] The great advancement in the frequency properties of InAlN/GaN HFETs allows application above W-band. However, the domestic development of the RF characteristics in InAlN/ GaN HFETs is much slow. Our group fabricated a 70-nm T-shaped InAlN/GaN HFET with 162-GHz f_T and 176-GHz f_{max} using alloyed Ohmic contacts.[14]

In this work, we show the fabrication and characterization of InAlN/GaN HFETs with high value of f_T. To improve the high frequency performance, regrown n^+-GaN Ohmic contacts were adopted to scale the source-to-drain distance (L_{sd}). Moreover, a 50 nm rectangular gate is realized by self-aligned-gate technology. The fabricated InAlN/GaN HFETs show a maximum drain saturation current density of 2.11 A/mm at V_{gs} = 1 V, combined with a peak extransic transconductance (g_m) of 609 mS/mm. In addition, the devices with 50-nm rectangular gate show a high f_T of 220 GHz and combined f_{max} of 48 GHz.

1 Experiments

As shown in Fig. 1 (a), the InAlN/GaN heterostructure for this study consists of a 5 nm lattice matched $In_{0.17}Al_{0.83}N$ barrier, a 1 nm AlN spacer, and a semi-insulating GaN buffer on (0001) sapphire substrate, using metal organic chemical vapor deposition (MOCVD). The as-grown material show a 2DEG electron density of 1.9×10^{13} cm^{-2} and an electron mobility of 1300 $cm^2/V \cdot s$ by van der Pauw hall effect measurements at room temperature. The mesa isolation of device processing was achieved using a Cl_2/BCl_3 plasma-based dry etch. Subsequently, the InAlN/GaN heterostructure was deposited with SiO_2 mask for n^+ GaN regrowth by plasma enhanced chemic vapor deposition (PECVD), then using reactive ion etching (RIE), the source and drain regions were patterned. The distance between source and drain with n^+ GaN (i.e., $L_{sd\text{-}regrown}$) of 600 nm was defined to reduce the parasitic resistance and capacitance. n^+-GaN was regrown by MOCVD with doping Si at the doping level about $\sim 3 \times 10^{19}$ cm^{-3}. After regrowth, the n^+-GaN above SiO_2 layer was removed by HF. A 50-nm rectangular Ni/Au gate was then self-aligned to the n^+-GaN non-alloyed ohmic contacts by electron-beam lithography and lift-off technology. The Schottky gate was in the middle between the source and drain contacts. Finally, SiN passivation layer was deposited by PECVD and patterned for contact pads using RIE. Figure 1 (b) demonstrates the scanning electron micrograph (SEM) image of the fabricated InAlN/GaN HFETs, indicating a source-to-drain distance (L_{sd}) of 600 nm.

2 Results and Discussion

Using the transmission line method (TLM) measurements, the Ohmic resistance components of the regrown contacts were analyzed. Before analysis, the dimensions of the patterns in TLM were all confirmed by SEM. As seen from the insertion in Fig. 2, the total resistance of the regrown contact (R_{tot}) includes three parts, i.e. the resistance (R_c) at metal/n^+-GaN interface, n^+-GaN access resistance from the regrown edge to ohmic ($R_{n+\text{-}GaN}$) and the resistance (R_{int}) at the interface of n^+-GaN/2DEG.[15] Using the TLM patterns and regrown contacts in the InAlN/GaN channel, a sheet resistance of 260 Ω/sq and a total contact resistance (R_{tot}) of 0.36 Ω · mm were calculated. Besides, using the TLM patterns and regrown contacts in the regrown n^+-GaN channel, a regrown n^+-GaN sheet resistance of 100 Ω/sq and a contact resistance (R_c) of 0.12 Ω · mm were extracted. Based on the obtained sheet resistance of n^+-GaN and the spacing between metal contacts and the regrown region, $R_{n+\text{-}GaN}$ of about 0.02 Ω · mm was obtained. Thus, the resistance (R_{int}) at the interface of n^+-GaN/ 2DEG was calculated to be 0.22 Ω · mm. Due to the relatively low Si doping level ($\sim 3 \times 10^{19}$ cm^{-3}), the value of R_c is higher than other reported results. Moreover, according to our former results, the

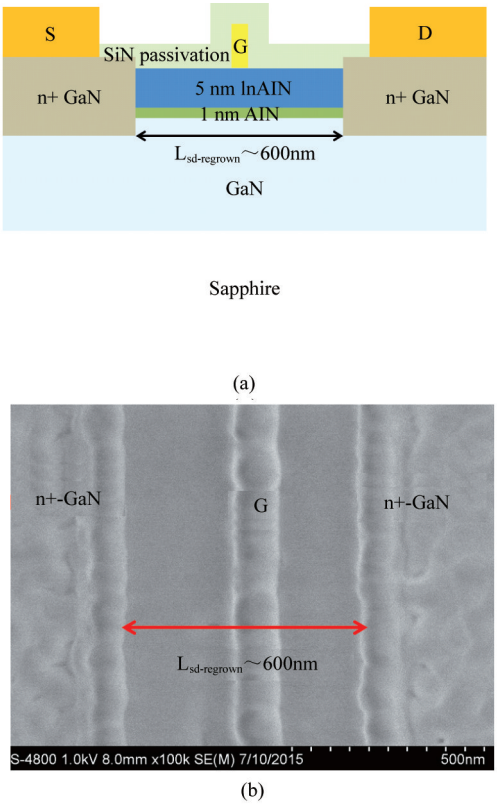


Fig. 1 (a) Schematic cross section and (b) the SEM plan form of the fabricated InAlN/GaN HFETs
图1 InAlN/GaN HFETs 器件截面示意图(a)和扫描电镜平面图(b)

sidewall obliquity at the n^+-GaN regrown interface seriously effects the ohmic resistance at the interface of n^+-GaN/2DEG, resulting in a higher value of R_{int}.[16]

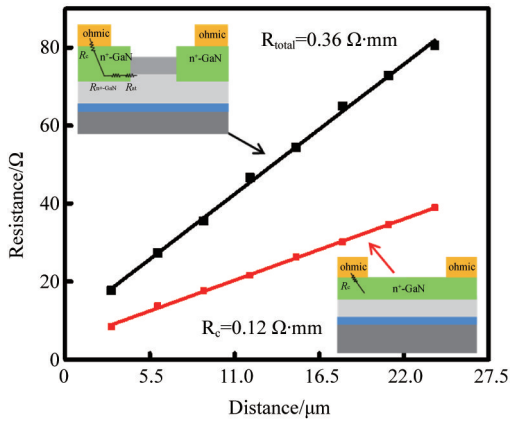


Fig. 2 TLM results of regrown contacts
图2 再生长欧姆接触 TLM 结果

Figure 3 exhibits the DC output (a) and transfer (b) characteristics of the InAlN/GaN HFETs with regrown contacts, which were measured using a semiconductor characterization system. In the measurements of DC output curve, the drain-source voltage ranges from 0 V to 8 V, stepped by 0.05 V. The gate voltage ranges from 1 V to -6 V, stepped by -1 V. While in the measurements of transfer curve, the drain bias is set as 5 V, and the gate voltage ranges from 1 V to -7 V, stepped by -0.1 V. A maximum drain saturation current density (I_{ds}) of 2.11 A/mm is achieved at V_{gs} = 1 V. Besides, at V_{gs} = -1.9 V and V_{ds} = 5 V, a peak extrinsic transconductance (g_m) with 609 mS/mm is measured. To our best knowledge, this is a very high value of I_{ds} with a thin barrier layer below 5 nm. This is mainly due to the effective scaling of source-drain distance. The value of on-resistance (R_{on}) for the fabricated device was extracted to be 1.36 Ω · mm at V_{gs} = 0 V and V_{ds} in the range between 0 V and 0.5 V. This R_{on} value is higher than the total values of the channel resistance and source/drain resistances ($R_s + R_d + R_{sheet}$ = 1.21 Ω · mm) extracted from the TLM results. The reason for the additional 0.15 Ω · mm may be due to the effect of gate metal or electric field on the channel electron density, which induces the increase of channel resistance. At gate bias of -7 V, with the drain bias ranging from 0 V to 5 V, the drain current density reaches to 10 mA/mm, and becomes much worse with further increasing drain bias. As seen from Fig. 3 (b), the poor pinch off behavior is mainly resulting from the large gate leakage. The gate leakage current can be decreased by oxygen plasma treatment, which induces a thin oxide layer at the surface of InAlN/GaN heterostructure.[11] Besides, although the rate of gate length to InAlN barrier layer is larger than 9, it was observed some evidences of short-channel effects that output conductance increased at V_{ds} > 5 V. This may be because of the increase of 2DEG electron density under the access region after SiN passivation.

On-wafer small-signal RF properties of the device were measured from 100 MHz to 50 GHz with 0.05 GHz step using a vector network analyzer. The analyzer used an LRRM calibration with off-wafer impedance standards. The system was calibrated with an off-wafer line reflect match calibration standard. The S-parameters were measured using on-wafer open/short calibration structures. Figure 4 characterizes the current gain $|H_{21}|^2$ and the maximum available gain (MAG) derived from measured S-parameters plotted against frequency at the peak f_T bias of V_{gs} = -1.9 V and V_{ds} = 5 V. Extrapolation of $|H_{21}|^2$ and MAG -20 dB/dec roll-off yields f_T of 220 GHz and f_{max} of 48 GHz. To our knowledge, the extrapolated f_T of 220 GHz is the best reported for InAlN/GaN HFETs in domestic. From the cold-FET and the measured S-parameters of the devices[17], the equivalent circuit model parameters were extracted and shown in Fig. 4 (b). Attributed to the effective scaling of source-drain distance, the values of source resistance (R_s), drain resistance (R_d) and channel resistance (R_i) are very small, which are propitious to improve the RF characteristics. However, the rectangular Schottky gate induces large value of gate resistance (R_g), resulting in a comparable small f_{max}. Using T-shaped gate can reduce the value of R_g, and improve the maximum oscillation fre-

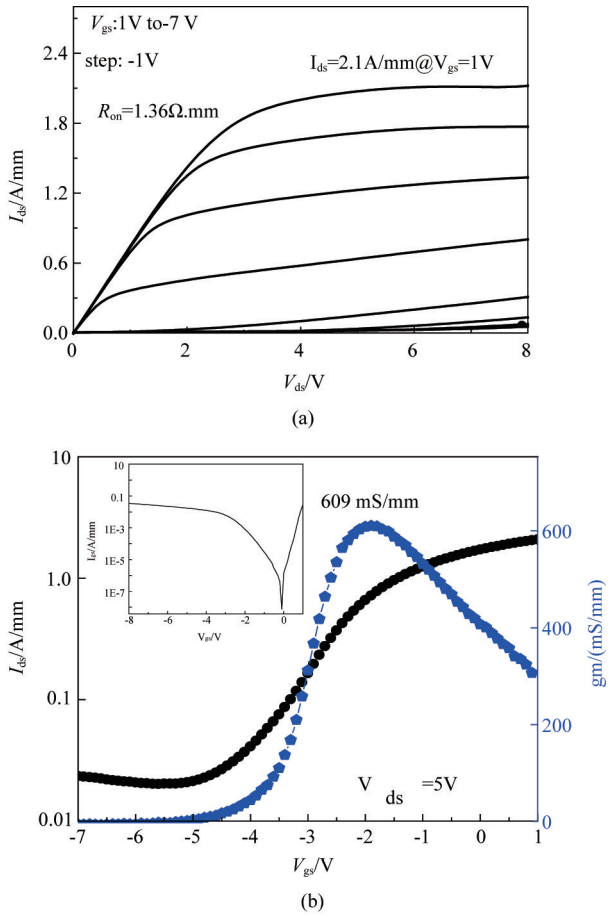
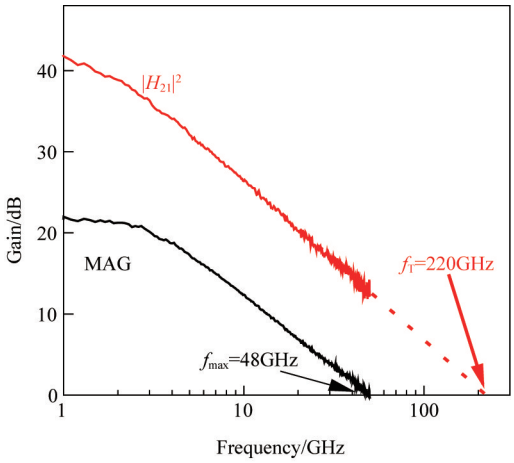


Fig. 3　DC output (a) and transfer (b) characteristics of the fabricated InAlN/GaN HFETs
图 3　InAlN/GaN HFETs 器件直流输出曲线(a)和转移特性曲线(b)



C_{gs}	375 fF/mm
C_{gd}	108 fF/mm
C_{ds}	210 fF/mm
g_{ds}	120 mS/mm
g_m	810 mS/mm
R_g	18 Ω·mm
R_s	0.43 Ω·mm
R_d	0.54 Ω·mm

(b)

Fig. 4　(a) Small signal RF performance and (b) the model parameters
图 4　小信号射频性能(a)和模型参数(b)

quency.

Figure 5 shows the measured f_T vs L_g compared with the results of other groups. The fabricated device shows a comparable high value of f_T with 50 nm gate length. The electron saturation velocity (ν_{sat}) in the InAlN/GaN HFETs can be calculated as following:

$$f_T = \frac{v_{sat}}{2\pi L_g} \quad . \quad (1)$$

Using the above equation, the electron saturation velocity of our device and other groups are calculated. As plotted in Fig. 5, the highest electron saturation velocity of reported results is about 0.9×10^7 cm/s, and the value of ν_{sat} in our device is about 0.7×10^7 cm/s, which is in a comparable high level. However, the calculated ν_{sat} value is much lower than the theoretical one 3×10^7 cm/s,[18] this is mainly because that the calculated ν_{sat} value is extrinsic, which does not consider the influence of all the parasitical parameters. Moreover, the imperfect crystal quality also affects the electron saturation velocity due to the defect scattering. To further improve the RF performance, the gate length needs to be further scaled, and crystal quality also needs to be optimized.

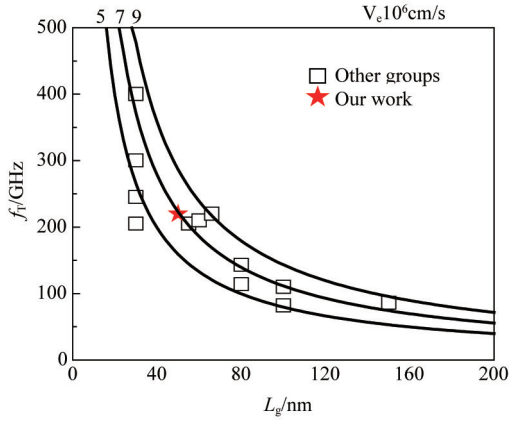


Fig. 5　Comparison of measured f_T vs L_g with other groups' results
图 5　本文结果同其他研究团队的结果对比(f_T vs L_g)

3　Conclusions

In summary, an InAlN/GaN HFET with high value of f_T was demonstrated on sapphire substrate. In order to

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tangular waveguide filter [J]. *Journal of Infrared, Millimeter, and Terahertz Waves*, 2013, **34**(12): 847-855.
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decrease the parasitical source/drain resistance, the source-to-drain distance (L_{sd}) was scaled to 600 nm using MOCVD to regrow n^+-GaN Ohmic contacts. In addition, a 50 nm rectangular gate was fabricated by self-aligned-gate technology in the middle of the source and drain. Due to the scaled source-to-drain distance, the InAlN/GaN HFET showed a high I_{ds} of 2.11 A/mm @ $V_{gs}=1$ V and a peak g_m of 609 mS/mm. On-wafer small-signal RF measurements indicate that the values of extrapolated f_T and f_{max} for the device were 220 GHz and 48 GHz, respectively. To our best knowledge, the extrapolated value of f_T is the best domestic reported one for InAlN/GaN HFETs.

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