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Design and analysis of a novel low dark count rate SPAD

YANG Jia[1,2], JIN Xiang-Liang[1,2*], YANG Hong-Jiao[1,2], TANG Li-Zhen[1,2], LIU Wei-Hui[1,2]

(1. School of Physics and Optoelectronics, Xiangtan University, Xiangtan, China, 411105;
2. Hunan Engineering Laboratory for Microelectronics, Optoelectronics and System on a Chip, Xiangtan, China, 411105)

Abstract: A novel low dark count rate single-photon avalanche diode (SPAD) device was designed and fabricated with the 0.18 μm CMOS Image Sensor (CIS) technology in this paper. The device is comprised of an effective P+/LNW (light N-well doping) junction for photon detecting and a low concentration N-type diffusing circular guard-ring formed by the deep N-well diffusion. The latter prevents premature edge breakdown (PEB) of the junction and ensures it to operate in Geiger mode. The measured results show that the SPAD achieves a low dark count rate (DCR), and the DCR is 260 Hz at an excess bias voltage of 2V for 8 μm diameter active area structure at room temperature.

Key words: single-photon avalanche diode (SPAD), premature edge breakdown (PEB), complementary metal oxide semiconductor(CMOS)

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一种新型低暗计数率单光子雪崩二极管的设计与分析

杨　佳[1,2], 金湘亮[1,2*], 杨红姣[1,2], 汤丽珍[1,2], 刘维辉[1,2]

(1. 湘潭大学 物理与光电工程学院,湖南 湘潭　411105;
2. 湖南省微光电与系统集成实验室,湖南 湘潭　411105)

摘要:基于0.18 μm互补金属氧化物半导体(CMOS)图像传感器工艺提出一种新型的低暗计数率(Dark Count Rate)单光子雪崩二极管(SPAD)器件.该器件是利用P+/LNW(Light N-well doping)结检测光子,并通过低浓度的N型扩散圆形保护环抑制边缘击穿,确保其工作在盖格模式.测试结果表明在室温环境下,直径为8 μm的SPAD器件,雪崩击穿电压为14.2 V,当过调电压设置为2 V时,暗计数率为260 Hz,具有低的暗计数率特性.

关　键　词:单光子雪崩二极管(SPAD);边缘击穿(PEB);互补金属氧化物半导体(CMOS)

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Introduction

Single-photon avalanche diodes (SPADs) are widely used in various fields of sciences, such as nuclear physics, chemistry, biomedicine, and astronomy[1-2]. Many of these applications require the acquisition of images in the circumstance of extreme weak optical signals at high speed, such as extraordinary low levels of fiuorescence correlation spectroscopy[3] and high speed time-correlated single-photon counting[4], etc. However, traditional optical devices, like charge coupled devices (CCDs)[5], active pixel sensors (APS)[6], silicon photomultipliers (SiPMs)[7] and depleted field effect transistors (DEPFETs)[8], are generally unable to offer the desired accuracy and high speed at moderate fabrication cost.

Compared with traditional optical devices, SPADs show properties of low noise, high resolution, ultimate optical sensitivity, and low power consumption. It is difficult for traditional SPADs to meet all these requirements simultaneously. Recently, various CMOS devices based

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Biography: YANG Jia (1988-), male, Fenghuang, China, M. E. Research area is photoelectric sensor and integrated circuit design.
E-mail: javayang4@163.com

* **Corresponding author**: E-mail: jinxl@xtu.edu.cn

on SPADs along with different PN junctions and guard-rings have been proposed to improve their performances since Rochas et al. reported the first detector in 0.8 μm CMOS technology[9]. More specifically, the SPAD usually consists of two parts, including P +/deep N-tub junction and light P-type doping tub which serves as a guard-ring to prevent SPAD from premature edge breakdown (PEB). With device scaling, depletion regions at two sides of p-tub may merge so that the active area of SPAD is almost fully depleted. Therefore SPAD cannot operate in Geiger mode to implement photo detection. In 2006, Finnkelstein et al.[10] proposed a new SPAD structure using shallow trench isolation (STI) guard-rings around the active p +/N-well junction which can effectively avoid the edge breakdown and increase fill factor. However, DCR of the device by this design is much higher than that by other existing designs (hundreds of kHz) due to much higher trap energy levels from the STI interface than that of others. In 2011, the first SPAD in 65 nm CMOS technology reported by Karami et al. shows high DCR level (tens of kHz) caused by high doping concentration[11]. Another important characteristic of SPAD is photon detection efficiency (PDE), which refers to the efficiency of a photon being absorbed in the detector active area to generate an electron-hole pair capable of triggering an avalanche. The PDE depends on diode's quantum efficiency as well as the excess bias voltage V_E. Nowadays, many researchers focus on integration of low DCR, small size pixel, low breakdown voltage, and high PDE SPADs in state-of-the-art deep sub-micrometer CMOS processes, as well as larger SPAD arrays with increasing levels of in-pixel and on-chip signal processing. All the efforts are made to further scaling of CMOS SPAD.

In this paper, a novel SPAD is achieved in 0.18-μm CMOS image sensor (CIS) technology to reduce DCR. The SPAD includes a light N-well doping (LNW), which is established in the central region to enhance the electric field. What's more, an N-type doping circular guard-ring is created by deep N-well diffusion. This paper is organized as follows. Section 2 gives the design of the proposed SPAD structure. In Sec. 3, the experimental set-up is described, and the measurement results of the breakdown voltage, DCR of SPAD are discussed in detail. Finally, the paper is concluded in Sec. 4.

1　SPAD structure

The SPAD was fabricated with the 0.18-μm CIS technology, which typically offers a triple well process. This process can isolate P-well regions from the substrate to reduce substrate noise effects[12]. The deep N-well retrograde doping makes doping concentration increase from a low level at the surface to a high level deeper into the wafer. As a result, the layer serves as both field-enhancer and virtual guard-rings.

As can be seen in Fig. 1 (a), the SPAD consists of a P +/LNW (light N-well doping) junction and a circular virtual guard-ring by blocking the formation of P-well[12]. The LNW layer is used to define the active region for photo detection, where avalanche multiplication occurs. A rare trap center in LNW region decreases DCR greatly. Another N-type doping is implanted with a deep N-well retrograde doping profile. The periphery of the P + region is lightly doped due to the retrograde characteristic of the layer. Thus a virtual guard-ring is created to prevent edge breakdown. The upward diffuse of doped atoms in the deep wafer improves the active region's ability of collecting charges. Moreover, all the non-active areas of SPAD are covered with the metal layers to avoid lighting, which are shaped by the order of metal 1, metal 2 etc. As Fig. 1 (b) shows, the depletion region is below the active area. The red region has high electrical field while the blue region has low electrical field in the simulation results. It is obvious that the electrical fields around guard ring are lower than that of multiplication region. The PEB can be effectively prevented by the guard-ring.

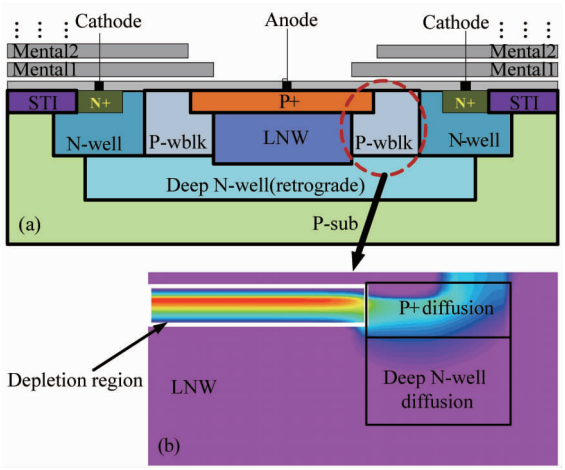

Fig. 1　(a) The structure of SPAD. (b) Simulation result of electrical field

图 1　(a) SPAD 结构图, (b) 电场强度仿真结果

Figure 2 shows the microphotograph of the circular SPAD with an 8-μm diameter active area. The virtual guard-ring of SPAD is covered with metals to prevent photon from being absorbed in the guard-ring region, which can result in high DCR and high afterpulsing probability[11]. Moreover, surface generation from the STI interface is likely to increase DCR[10]. Therefore the guard-ring region is devised without STI of SPAD structure.

2　Experimental set-up and measurement results

Generally, there are two different circuit configurations used to fabricate the SPAD avalanche sensing[13]. The method shown in Fig. 3 has been chosen to measure the characteristics of SPAD in this paper. The cathode of SPAD is connected to the source of the excess bias voltage V_E and the breakdown voltage V_BR, and the anode is connected to ground through a quenching resistor. In this case, the output of SPAD will be a high voltage modulated by quenching resistor. The deep N-well/P-Sub junction capacitance has no influence on increasing the afterpulsing probability and dead time of SPAD when imple-

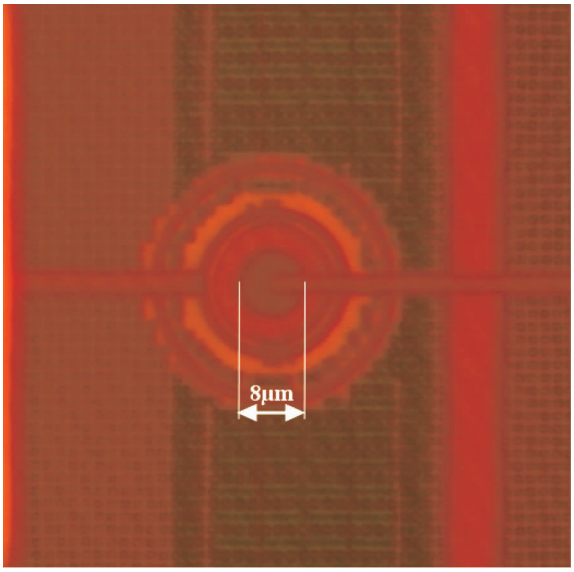

Fig. 2 Microphotograph of the SPAD fabricated in 0.18 μm CIS technology
图2 基于0.18 μm CIS工艺的SPAD显微镜照片

menting in-pixel photon detection. Thus, the $C_{parasitic}$ is the sum of parasitic capacitance of SPAD and I/O PADs in this circuit. The high quenching resistor ($R_{quenching}$) is typically chosen as hundreds of kilohm. As a result, the dead time of SPAD is set to be long.

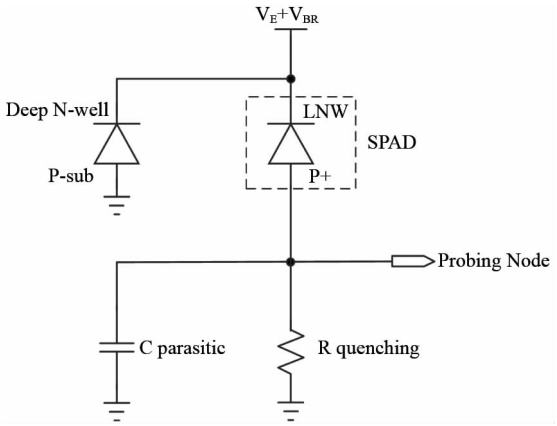

Fig. 3 Measurement circuit of the SPAD device
图3 SPAD器件的测试电路

The doping concentration levels are increased with the CMOS technology scaling down, which increases the peak electric field at the depletion region of SPAD, and decreases the breakdown voltage and the width of the depletion region[14]. Figure 4 shows the measured *I-V* characteristics of two different SPAD structures in reverse bias mode. As can be seen, the rectangular labeled *I-V* characteristics curve of SPAD illustrates that the premature edge breakdown occurs, and the guard-ring fails to make SPAD operate in Geiger mode. The triangle labeled *I-V* characteristics curve shows that the breakdown voltage of SPAD is approximately 14.2 V, which indicates that the breakdown mechanism of P+/LNW junction is avalanche, and the virtual P-wblk guard-ring can effectively eliminate the PEB[3].

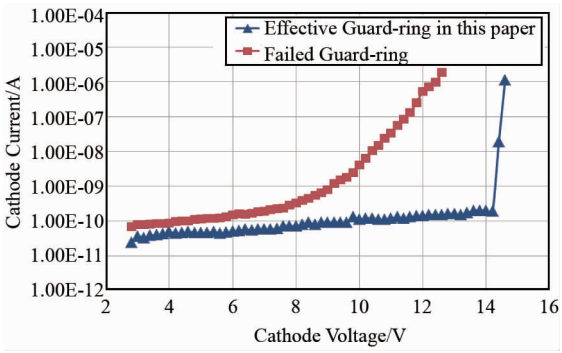

Fig. 4 *I-V* characteristics of the SAPD at room temperature
图4 常温下SPAD的*I-V*特性曲线

3 DCR measurement results

The DCR was measured by counting the number of avalanches pulse when the SPAD was biased by a voltage that is larger than its breakdown voltage. The DCR measurement was performed in the dark condition. The probing node was connected to a high performance oscilloscope to count DCR. Moreover, the excess bias voltage ranging from 0.4 V to 3.6 V were applied with a 0.4 V step. The relationship of DCR and V_E is illustrated in Fig. 5. We can see that DCR increases linearly with the increase of V_E, which is mainly due to the band-to-band tunneling and trap-assisted tunneling carrier generation. When V_E increases from 0 to 3.6V, the DCR of P+/LNW SPAD varies from 0.05 kHz to 0.85 kHz while the DCR of P+/N-well SPAD varies from 0.13 kHz to 3.6 kHz. The results indicate that our design has achieved a low DCR. The low DCR of P+/LNW SPAD benefit from the light and pure N-type doping concentration in LNW region, which results in rare trap centers.

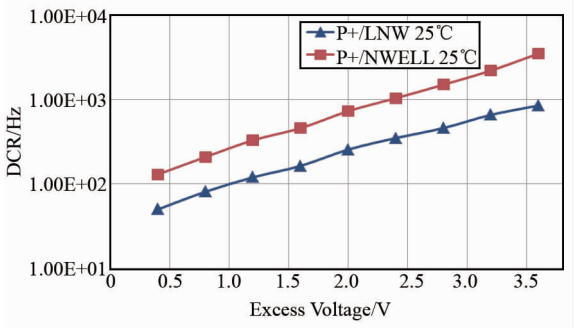

Fig. 5 The DCR of SPAD at different excess bias voltage
图5 SPAD加不同额外偏置电压的DCR特性

Figure 6 shows the DCR of SPAD at different temperature when V_E remains at 2.0 V. The DCR of P+/LNW SPAD and P+/N-well SPAD increases from 0.055 kHz to 0.52 kHz and from 0.13 kHz to 1.52 kHz, respectively, with the temperature varying from -20 ℃ to 45℃. This is mainly caused by Shockley Read Hall

(SRH) thermal generation. At the same time, tunneling effect also contributes to this phenomenon[11]. Therefore, it is necessary to make SPAD properly operate in Geiger mode to exhibit acceptable levels of DCR in practice applications.

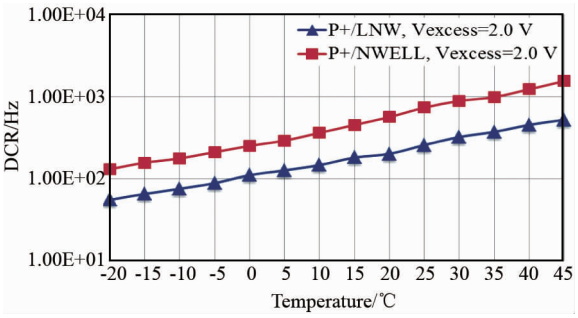

Fig. 6 The DCR of SPAD at different temperature
图 6 SPAD 在不同温度下的 DCR 特性

4 Conclusions

A novel low dark count rate (DCR) single-photon avalanche diode (SPAD) has been designed and fabricated with the 0.18 μm CMOS image sensor (CIS) technology. The proposed SPAD adopts a P+/LNW junction structure. It also has a guard-ring achieved with low concentration of N-type doping circular region, which can prevent PEB effectively. The DCR of the SPAD is 260 Hz at 2V excess bias voltage for 8 μm diameter active area structure at room temperature. Moreover, *I-V* curves of the SPAD has also been demonstrated and the breakdown voltage of the SPAD is about 14.2 V.

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