文章编号: 1001 - 9014(2016)02 - 0172 - 05

DOI:10.11972/j.issn.1001 - 9014.2016.02.009

Direct extraction method of equivalent circuit parameters for stacked transformer

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Abstract: A parameter-extraction approach for the stacked on-chip transformer, which combines the analytical approach and the empirical optimization procedure, was developed. The model parameters determined from the analytical expressions were considered as an initial guess of a subsequent optimization procedure leading to the final model parameters. Good agreement was obtained between simulated and measured results for a stacked transformer on silicon substrate in the frequency range 100 MHz ~ 60 GHz.

Key words: parameter-extraction approach, equivalent circuit, stacked transformer
PACS: 85.30.De

片上叠层式变压器的建模及参数提取

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摘要:结合分析法和优化法,针对片上叠层式变压器提出了一种参数提取方法.分析法得出的参数值作为优化法的初始值,从而得出最终的模型参数值.结果表明,在100 MHz ~ 60 GHz频率范围内,硅衬底的叠层式变压器S参数的仿真结果和测试结果吻合很好.

关 键 词:参数提取方法;等效电路;叠层式变压器

中图分类号:TN386.6 **文献标识码**:A

Introduction

Radio frequency integrated circuits (RFICs) such as low-noise amplifiers, voltage-controlled oscillators, mixers, and power amplifiers rely on a number of passive components including capacitors, varactors, resistors, inductors, transformers, and transmission lines. On-chip transformers are widely used to implement functions such as impedance conversion, resonant load, low-noise feedback, bandwidth enhancement, and differential-to-single conversion[1-7].

Due to their multi-metal layer structures, on-chip transformers manufactured in RF-CMOS technology can have various structures. Since the amount of silicon area occupied by transformers can be a limiting factor in most applications, interleaved or tapped structures are often replaced by stacked configurations, which offer higher magnetic coupling and area efficiency, albeit at the expense of increased parasitic capacitances[8-10].

With the increase in demand of high-performance stacked transformers, accurate compact models are especially valuable for efficient simulation for RF circuit design. Because of the accuracy of the model is really dependent on the model parameters, an accurate procedure for extraction of the model parameters is extremely important for optimizing device performance of on-chip transformer based on silicon material system[11-13].

The model parameters can be obtained from S-parameters measurements by using numerical optimization

Received date: 2015 - 05 - 19, **revised date**: 2015 - 12 - 14 **收稿日期**:2015 - 05 - 19, **修回日期**:2015 - 12 - 14
Foundation items:Supported by National Natural Science Foundation of China (61474044)
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techniques. However, the accuracy of the numerical optimization methods that minimizes the difference between measured and modeled data can vary, depending on the optimization method and starting values, while the analytical methods allow us to extract the equivalent circuit model parameters in a straightforward manner[14-15].

The analysis and modeling of monolithic stacked transformers on silicon were addressed. This method is a combination of numerical optimization and direct extraction methods. It overcomes the drawbacks of both methods, while retaining their advantages. Section I describes the basic formalism of the new method used in the extraction procedure. In section II, extraction results are given and discussed. The conclusions are discussed in section Ⅲ.

1 Theoritical analysis

1.1 Equivalent circuit model

The dynamics of the stacked transformer can be captured in a compact model similar to the coupled inductors, as shown in Fig. 1, where $C_{\rm oxi}$ and $C_{\rm oxo}$ represent the oxide capacitances between the metal segments and Si substrate. $C_{\rm io}$ represents the isolation capacitance between the input and output pad, and can be neglected because its small value (less than 1 fF normally) and does not affect the frequency response. $C_{\rm subi}$, $C_{\rm subo}$ and $R_{\rm subi}$, $R_{\rm subo}$ are the capacitances and resistances of the Si substrate, respectively. L_1 is the inductance of primary alone and L_2 is that of the secondary alone. R_1 and R_2 are the losses of primary and secondary, respectively. The parameter K, which represents the mutual inductance between the two wings, is related with the inductance L_1 and L_2.

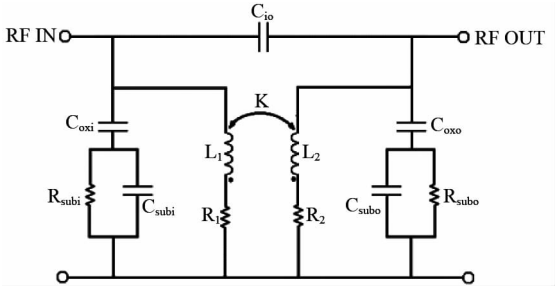

Fig. 1　Equivalent circuit model for stacked transformer
图 1　叠层式变压器的等效电路模型

An alternative form of the equivalent circuit with an impedance inverter $K = \dfrac{L_m}{\sqrt{L_1 L_2}}$ can be used to represent the coupling, as shown in Fig. 2, where L_m indicates the degree of coupling between primary and secondary. This equivalent circuit model can be divided into two parts. The outer part contains just pad parasitics, and the inner part contains intrinsic elementary cell.

1.2 Extraction of equivalent circuit parameters

Figure 3 shows the open test structure layout with the corresponding equivalent circuit model. The short circuit Y-parameters of the equivalent circuit can be expressed as the following:

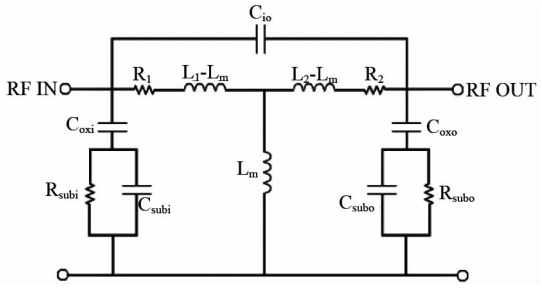

Fig. 2　Modified equivalent circuit model for stacked transformer
图 2　叠层式变压器的简化等效电路模型

$$Y_{11} = j\omega C_{\rm io} + Y_i \quad , \quad (1)$$

$$Y_{22} = j\omega C_{\rm io} + Y_o \quad , \quad (2)$$

$$Y_{12} = Y_{21} = -j\omega C_{\rm io} \quad , \quad (3)$$

where

$$Y_i = \frac{1}{\dfrac{1}{j\omega C_{\rm oxi}} + \dfrac{R_{\rm subi}}{1 + j\omega R_{\rm subi} C_{\rm subi}}} \quad , \quad (4)$$

$$Y_o = \frac{1}{\dfrac{1}{j\omega C_{\rm oxo}} + \dfrac{R_{\rm subo}}{1 + j\omega R_{\rm subo} C_{\rm subo}}} \quad . \quad (5)$$

In the low-frequency ranges, the oxide capacitances and substrate resistances can be determined as follows:

$$C_{\rm oxi} = -\frac{1}{\omega {\rm Im}\left(\dfrac{1}{Y^o_{11} + Y^o_{12}}\right)} \quad , \quad (6)$$

$$C_{\rm oxo} = -\frac{1}{\omega {\rm Im}\left(\dfrac{1}{Y^o_{22} + Y^o_{12}}\right)} \quad , \quad (7)$$

$$C_{\rm io} = -\frac{{\rm Im}(Y^o_{12})}{\omega} \quad , \quad (8)$$

$$R_{\rm subi} = {\rm Re}\left(\frac{1}{Y^o_{11} + Y^o_{12}}\right) \quad , \quad (9)$$

$$R_{\rm subo} = {\rm Re}\left(\frac{1}{Y^o_{22} + Y^o_{12}}\right) \quad . \quad (10)$$

In the high frequency ranges, the substrate capacitance ($C_{\rm subi}$ and $C_{\rm subo}$) can be determined from imaginary parts of $1/(Y^o_{11} + Y^o_{12})$ and $1/(Y^o_{22} + Y^o_{12})$:

$$C_{\rm subi} = \frac{1}{\omega}{\rm Im}\left\{1/\left[\left(\frac{1}{Y^o_{11} + Y^o_{12}}\right) - \frac{1}{j\omega C_{\rm oxi}}\right]\right\} \quad , (11)$$

$$C_{\rm subo} = \frac{1}{\omega}{\rm Im}\left\{1/\left[\left(\frac{1}{Y^o_{22} + Y^o_{12}}\right) - \frac{1}{j\omega C_{\rm oxo}}\right]\right\} \quad . (12)$$

The superscript o denotes the open test structure.

As shown in Fig. 4, after de-embedding parasitics, S-parameters are transformed to Z-parameters, the intrinsic elements can be determined directly as:

$$R_1 = {\rm Re}(z^i_{11}) \quad , \quad (13)$$

$$R_2 = {\rm Re}(z^i_{22}) \quad , \quad (14)$$

$$L_{1{\rm m}} = \frac{{\rm Im}(z^i_{11} - z^i_{12})}{\omega} \quad , \quad (15)$$

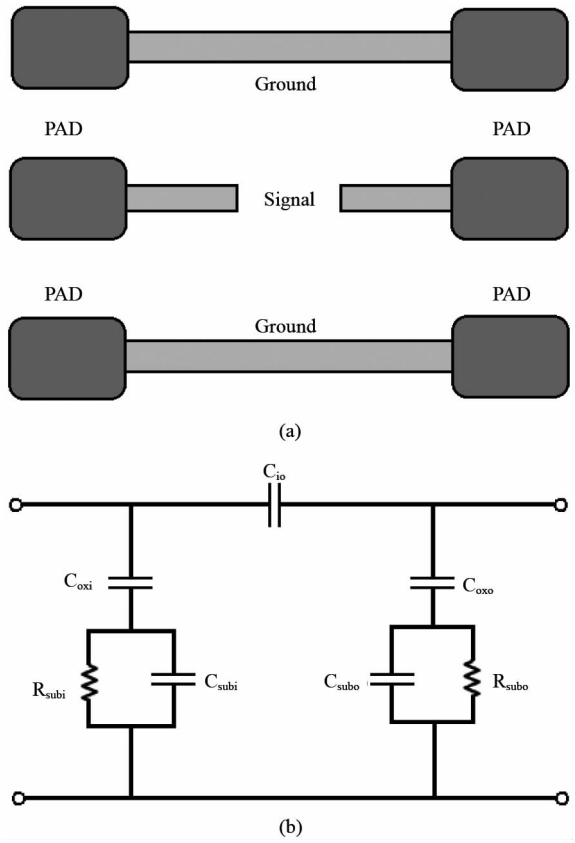

Fig. 3 (a) open test structure, (b) equivalent circuit model
图3 (a) 开路测试结构, (b) 开路等效电路模型

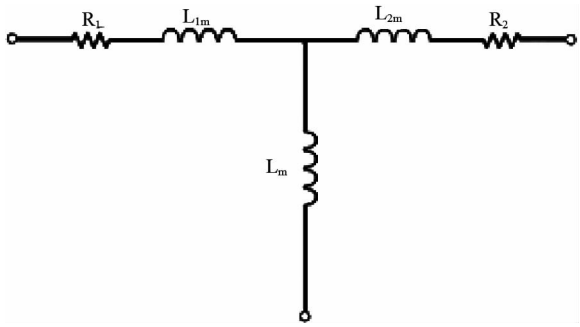

Fig. 4 Transformer intrinsic cell
图4 变压器本征单元

$$L_{2m} = \frac{\mathrm{Im}(z_{22}^{i} - z_{12}^{i})}{\omega} \quad , \quad (16)$$

$$L_{m} = \frac{\mathrm{Im}(z_{12}^{i})}{\omega} \quad . \quad (17)$$

The superscript i denotes the intrinsic structure.

This method also can be considered as an initial guess of a subsequent optimization procedure leading to the final model parameters.

The optimization error is defined by the RMS (Root Mean Square) error of S-parameters as error function criterion:

$$\text{RMS target} = \sqrt{\frac{1}{N}\sum_{i=1}^{N} |S_{ij}^{m}|^2} \quad , \quad (18)$$

$$\text{RMS error} = \sqrt{\frac{1}{N}\sum_{i=1}^{N} \frac{|S_{ij}^{s} - S_{ij}^{m}|^2}{[\text{RMS target}]^2}} \quad , \quad (19)$$

where the superscript m denotes the measured S-parameters, s denotes the simulated S-parameters.

2 Results and discussions

To illustrate the above model and parameter extraction method, we presented the extracted model parameters for the stacked on-chip transformer using IBM 130 nm 1P8M RF CMOS technology, as shown in Fig. 5.

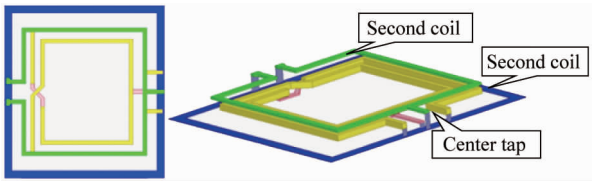

Fig. 5 Structure of the stacked transformer
图5 叠层式变压器结构

In this work, stacked transformer with one turn as primary coil on the first layer and two turns as secondary on another layer has been designed. The metal width is 3 μm for both two coils, the thickness of primary is 1.325 μm and the secondary one is 3.3 μm. The gap between the two metals is 1.45 μm. Open-loaded S-parameters were measured and de-embedded for the parasitics introduced by GSP PAD up to 60 GHz using an Agilent E8464A network analyzer.

Figure 6 shows the initial extracted capacitances C_{oxi} and C_{oxo} in the low frequency range. Over a wide frequency range, the value variations are very small and almost negligible, and rather constant values are observed. It is noted that C_{oxi} and C_{oxo} are very close, because the test structure is symmetric. Figure 7 shows the initial extraction of substrate capacitance C_{subi} and C_{subo}. It is observed that the substrate capacitances at input and output ports are very close. Extracted results of inductances L_{1m}, L_{2m} and L_m are shown in Fig. 8. It is found that the values of L_{1m}, L_{2m} and L_m are independent of frequency from 1GHz to 60 GHz, in spite of slight slopes of the extracted L_{1m} and L_{2m} in the low frequency ranges.

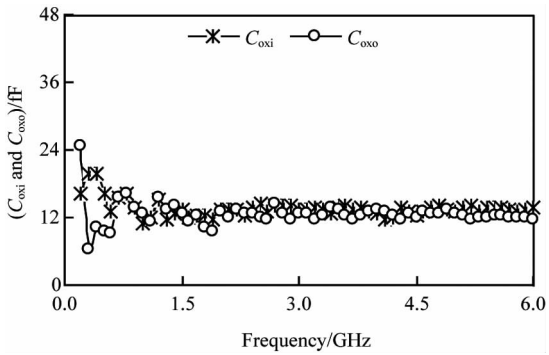

Fig. 6 Extracted pad capacitances versus frequency
图6 提取的pad电容随频率变化的曲线图

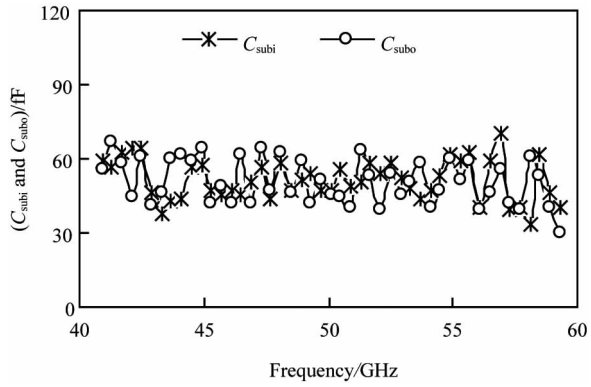

Fig. 7　Extracted substrate capacitances versus frequency
图 7　提取的衬底电容随频率变化的曲线图

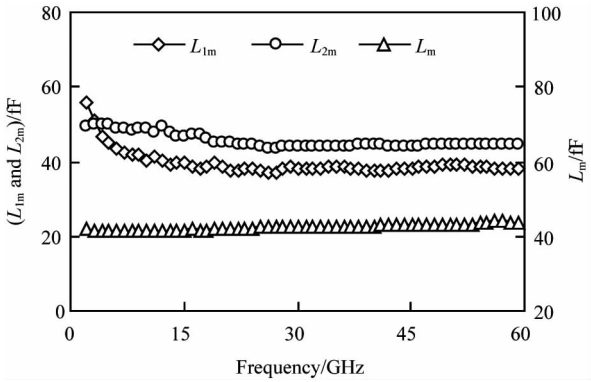

Fig. 8　ExtractedL_{1m}, L_{2m} and L_m versus frequency
图 8　提取的线圈自感 L_{1m}、L_{2m}和互感 L_m 随频率变化的曲线图

Table 1 summarizes the extracted model parameters using the analytical method mentioned above, and optimized values are given for comparison. The final values are very close to the analytical values.

Table1　Extracted and optimized values of model parameters
表 1　提取的模型参数值和优化的模型参数值

Model parameters	Extracted values	Optimized values
C_{io}/fF	0.06	0.06
C_{oxi}/fF	13.4	13.5
C_{oxo}/fF	13.2	13.0
C_{subi}/fF	44	43
C_{subo}/fF	49	50.1
R_{subi}/Ω	36	35
R_{subo}/Ω	35.5	35
L_{1m}/pH	37.8	38
L_{2m}/pH	43.7	44
L_m/pH	44.1	44
R_1/Ω	1.44	1.45
R_2/Ω	1.32	1.3

Figure 9 compares the magnitude and phase of measured and modeled S-parameters for the stacked transformer in the frequency range of 100 MHz ~ 60 GHz. The circle indicates the modeled values and the lines the measured ones. It is noted that there are slight

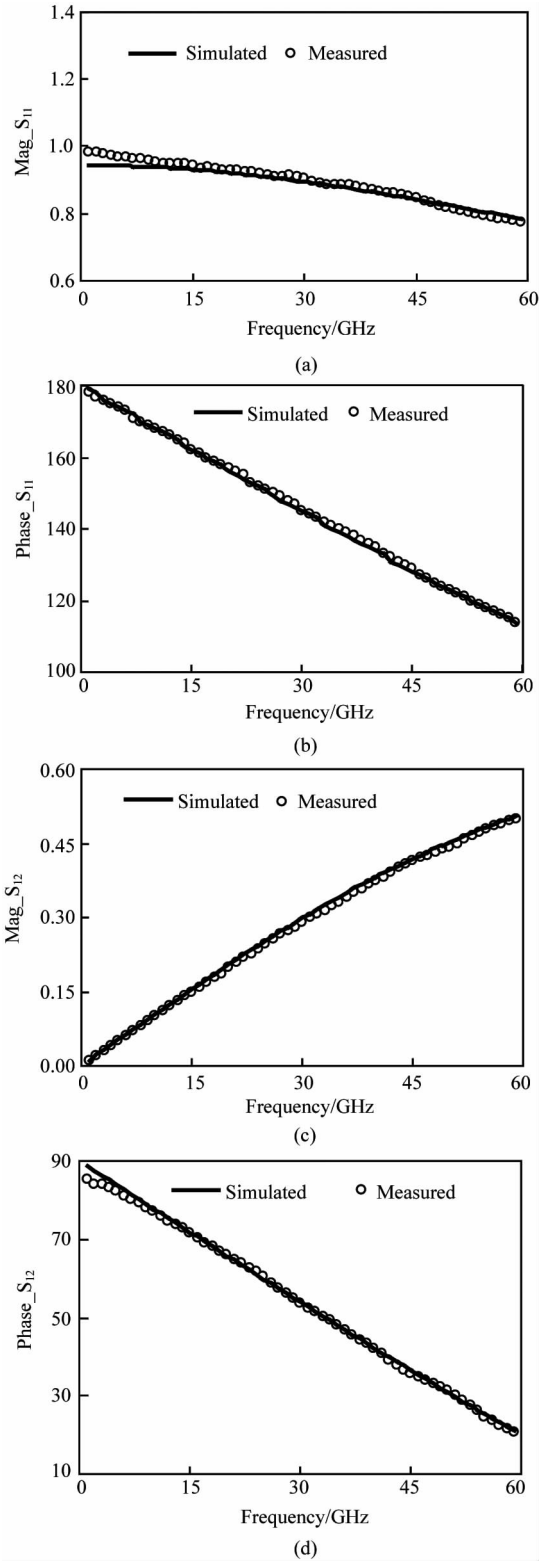

Fig. 9　Comparison of measured and simulated S-parameters of the stacked spiral transformer. (a) Magnitude of S_{11}, (b) phase of S_{11}, (c) magnitude of S_{12}, and (d) phase of S_{12}
图 9　叠层式变压器的测量和仿真 S 参数比较图(a) S_{11}的幅值随频率变化的曲线图,(b) S_{11}的相位随频率变化的曲线图,(c) S_{12}的幅值随频率变化的曲线图,(d) S_{12}的相位随频率变化的曲线图

slopes of the modeled S-parameters against measured ones in low frequency. The modeled S-parameters agree very well with the measured S-parameters, validating the accuracy of the proposed model and parameter extraction method. Good agreement was obtained between simulated and measured results with a RMS error less than 5%. Therefore, the accuracy of the model is validated in the frequency range 100 MHz ~ 60 GHz.

3 Conclusion

A parameter-extraction approach for the stacked on-chip transformer, which combines the analytical approach and the empirical optimization procedure was presented. The accuracy of the proposed method was validated by the excellent agreement between the simulated and measured results of the stacked spiral transformer using IBM 130 nm 1P8M RF CMOS technology in the frequency range 100 MHz ~ 60 GHz.

Acknowledgements

This work was supported in part by the National Natural Science Foundation of China under Grant 61474044, and Shanghai Minhang Excellent Talents.

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