第 37 卷第 2 期
2018 年 4 月

红 外 与 毫 米 波 学 报
J. Infrared Millim. Waves

Vol. 37, No. 2
April, 2018

文章编号: 1001 - 9014(2018)02 - 0135 - 05

DOI:10.11972/j.issn.1001 - 9014.2018.02.002

Design and realization of THz InAlAs/InGaAs InP-based PHEMTs

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Abstract: In this paper, 90-nm T-shaped gate InP-based $In_{0.52}Al_{0.48}As/In_{0.65}Ga_{0.35}As$ pseudomorphic high electron mobility transistors (PHEMTs) with well-balanced cut-off frequency f_t and maximum oscillation frequency f_{max} are reported. This device with a gate-width of 2 × 25 μm shows excellent DC characteristics, including a maximum saturation current density I_{dss} of 894 mA/mm, and a maximum extrinsic transconductance $g_{m,max}$ of 1 640 mS/mm. The off-state breakdown voltage ($BV_{off\text{-}state}$) defined at a gate current of 1mA/mm is 3.3 V. The RF measurement is carried out covering the full frequency range from 1 to 110 GHz, an extrapolated f_t of 252 GHz and f_{max} of 394 GHz are obtained, respectively. These results are obtained by the combination of gate size scaling, parasitics reduction and the on-wafer measurement in the full frequency band from 1 to 110 GHz.

Key words: InP, PHEMTs, InAlAs/InGaAs, on-wafer measurement, monolithic microwave integrated circuits (MMICs)
PACS: 84.40.-x

太赫兹 InP 基 InAlAs/InGaAs PHEMTs 的研制

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摘要:研制了一种 T 型栅长为 90 nm 的 InP 基 $In_{0.52}Al_{0.48}As/In_{0.65}Ga_{0.35}As$ 赝配高电子迁移率晶体管(PHEMTs). 该器件的总栅宽为 2 × 25 μm, 展现了极好的 DC 直流和 RF 射频特性, 其最大饱和电流密度和最大有效跨导分别为 894 mA/mm 和 1 640 mS/mm. 采用 LRM + (Line-Reflect- Reflect -Match)校准方法实现系统在 1 ~ 110 GHz 全频段内一次性校准, 减小了传统的分段测试多次校准带来的误差, 且测试数据的连续性较好. 在国内完成了器件的 1 ~ 110 GHz 全频段在片测试, 基于 1 ~ 110 GHz 在片测试的 S 参数外推获得的截止频率 f_t 和最大振荡频率 f_{max} 分别为 252 GHz 和 394 GHz. 与传统的测试到 40 GHz 外推相比, 本文外推获得的 f_{max} 更加准确. 这些结果的获得是由于栅长的缩短, 寄生效应的减小以及 1 ~ 110 GHz 全频段在片测试的实现. 器件的欧姆接触电阻率减小为 0.035 Ω · mm.

关 键 词:磷化铟;赝配高电子迁移率晶体管;InAlAs/InGaAs;在片测试;单片集成电路

中图分类号:TN385　　**文献标识码**:A

Introduction

Monolithic microwave integrated circuits (MMICs) and systems operating beyond 100 GHz have gained increased academic and commercial interest over the recent years[1]. They are of great interests for high-resolution imaging, next generation automotive collision avoidance radars, environmental sensors, security detection of con-

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Received date: 2017-06-24, **revised date**: 2017-09-01　　**收稿日期**:2017-06-24, **修回日期**:2017-09-01
Foundation items: Supported by National Natural Science Foundation of China (61275107)

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cealed weapons, broadband satellite communications and low noise detector[1-2]. Due to high carrier density and superior electron mobility and velocity in the high InAs mole fraction InGaAs channel, InP-based pseudomorphic high electron mobility transistors (PHEMTs) have demonstrated high frequency, low noise, high gain and low power consumption performance. Therefore, these devices are considered to be a unique candidate for those applications. Many high performance InP-based PHEMTs have been reported[3-5].

Excellent performance can be obtained by the combination of gate size scaling, parasitics reduction, and an increase of InAs mole fraction in the channel that improves electron transport properties. However, with In-content increased, the impact ionization effects will become serious due to the decreased energy band gap E_G, which have a number of negative consequences, such as reduced breakdown voltages, increase in output conductance and Kink effects, and permanent device degradation[6]. A method of increasing the effective energy band gap $E_{G,\mathrm{eff}}$ in the channel is to introduce energy quantization by reducing the channel thickness to dimensions comparable to the electron wavelength, which is shown in Fig. 1[6-7].

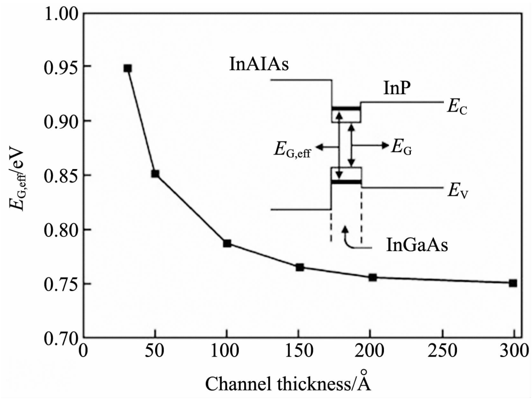

Fig. 1 Effective energy-gap $E_{G,\mathrm{eff}}$ as a function of channel thickness

图 1 有效能带宽度随沟道层厚度的变化

In this paper, the InAs mole fraction has been increased to 0.65, the thickness of channel was reduced to 11 nm for channel quantization, and the gate-length was reduced to 90-nm. The devices exhibit the RF characteristics of $f_t = 252$ GHz and $f_{\max} = 394$ GHz. Excellent DC characteristics are also demonstrated with a maximum saturation current density of 894 mA/mm and a $g_{m,\max}$ of 1 640 mS/mm.

1 Device epitaxial structure

The epitaxial wafer was grown by molecular beam epitaxy (MBE) on 3-inch semi-insulating InP (100) substrate. As shown in Fig. 2 and Table 1, the structure consists of a 10-nm thick n^+ $In_{0.6}Ga_{0.4}As$ and a 10-nm thick n^+ $In_{0.53}Ga_{0.47}As$ cap layer for enhanced ohmic contacts, a 14-nm thick undoped $In_{0.52}Al_{0.48}As$ as Schottky barrier, a unstrained 3-nm thick undoped $In_{0.52}Al_{0.48}As$ as spacer layers, a 11 nm thick quantized and strained $In_{0.65}Ga_{0.35}As$ channel layer, and a 400 nm thick undoped $In_{0.52}Al_{0.48}As$ buffer layer. A Siδ-doping (5E12 cm^{-2}) was inserted in the Schottky layer to supply electrons for current conduction.

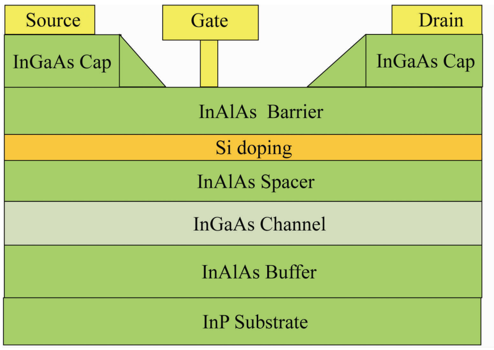

Fig. 2 The schematic cross-section of InP-based PHEMT

图 2 InP PHEMT 截面示意图

Table 1 InP-based PHEMT epitaxial Structure

表 1 InP PHEMT 外延结构示意图

Layer	Material	Doping	Thickness
Cap layer1	$In_{0.6}Ga_{0.4}As$	$2\times10^{19}cm^{-3}$	10 nm
Cap layer2	$In_{0.53}Ga_{0.47}As$	$5\times10^{18}cm^{-3}$	10 nm
Barrier layer	$In_{0.52}Al_{0.48}As$	undoped	14 nm
Si δ-doping layer	5×10^{12} cm^{-2}		
Spacer layer	$In_{0.52}Al_{0.48}As$	undoped	3 nm
Channel layer	$In_{0.65}Ga_{0.35}As$	undoped	11 nm
Buffer layer	$In_{0.52}Al_{0.48}As$	undoped	400 nm
S. I. InP Substrate			

A room temperature electron mobility of 10 500 $cm^2/V\cdot s$ has been achieved with a sheet charge of 3×10^{12} cm^{-2}.

2 Device fabrication

As shown in Fig. 2, the gate electrode is located at an offset position from the center toward the source. Due to minimizing the gate-to-drain capacitance (C_{gd}) and the source resistance (R_s) by reducing in the distance between the source and gate, the structural improvement enhances the maximum stable gain (MSG), as well as the extrinsic transconductance (g_m).

The short foot of the T-shaped gate enhanced the cut-off frequency (f_t) as well as the wide head of the T-shaped gate minimized the parasitic gate resistance (R_g). In this device, the space of source-drain and space of source-gate were 2 μm and 0.8 μm.

The PHEMTs fabrication was based on both optical and electron beam lithography (EBL). Firstly, the transistor mesa was chemically wet etched to provide isolated active areas by removing a ~200 nm thickness to expose the buffer layer. Secondly, source and drain ohmic contacts were spaced 2μm apart by a lift-off process, followed by the formation of ohmic contacts. The contact resistance (R_c) of 0.035Ω · mm and the specific contact resistivity of 1.3×10^{-7} Ω · cm^{-2} were obtained by using Transmission Line Method (TLM).

The most important process was the gate fabrication, which included gate lithography, recess, and metallization. The active devices feature T-shaped Ti-Pt-Au gates, which were defined by electron beam lithography in a three-layer resist (PMMA) process. At first, three layers of electron beam resist were coated on the surface, then electron beam lithography (EBL) were carried out in turn. Secondly, the gate recess was etched using a succinic acid based solution till barrier layer. Finally, a Ti-Pt-Au gate metal was evaporated and lifted off.

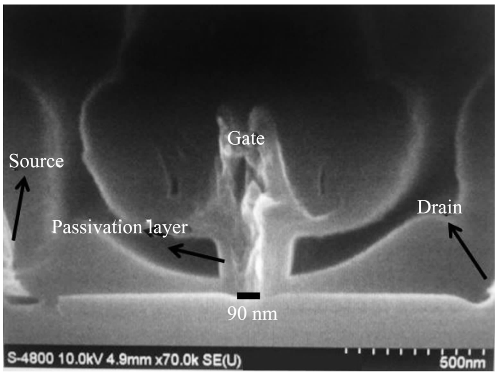

Fig. 3　The SEM photograph of T-gate
图 3　T 型栅的 SEM 照片

At last, the devices were passivated with 200-nm plasma enhanced chemical vapor deposited (PECVD) Si_3N_4 for good reliability, robustness, low leakage current and high breakdown Voltage. The SEM photograph of the fabricated T-gate is shown in Fig. 3.

3　Device performance

3.1　DC characteristics

The DC characteristics were measured by an HP 4142B semiconductor parameter analyzer. Fig. 4 shows the characteristics of drain current (I_{ds}) versus drain-source voltage (V_{ds}) with various gate-source voltage (V_{gs}) of the device at room temperature. The gate-source voltage (V_{gs}) increased from −0.6 V (bottom) to 0.2 V (top) by a step of 0.2 V. It can be seen from Fig. 4 that the PHEMTs exhibited good pinch-off characteristics and saturation drain current. This device can be well pinched off with a threshold voltage (V_{th}) of −0.6 V.

However, the kink effect occurs obviously as shown in Fig. 4, which is caused mainly by two factors. The first one is linked with traps in the InAlAs buffer layer, the traps capture energetic electrons and release them when drain bias increases. It can be reduced by improving the quality of InAlAs buffer layer. The other one is attributed to impact ionization process in the InGaAs channel, as the content of InAs in the channel increased, the energy gap decreased, so the impact ionization phenomenon became serious. When the drain bias increases to certain value, impact ionization is initiated at the drain-side gate edge and extends all the way to the drain contact, details were shown in our previously work[8]. In this work, energy quantization is introduced to increase the energy gap for reducing the impact ionization phenomenon.

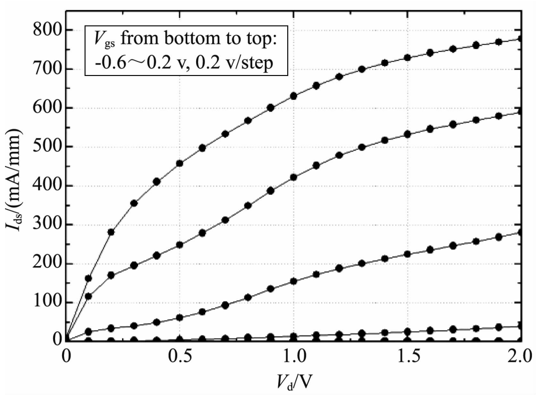

Fig. 4　DC characteristics of the device
图 4　器件的直流特性曲线

As shown in Fig. 5, the characteristics of the transconductance g_m and the drain current I_{ds} versus V_{gs} at V_{ds} of 1.5 V are demonstrated. The maximum g_m of the device at a V_{ds} of 1.5 V and a V_{gs} of −0.15V was 1 640 mS/mm. This high transconductance is due to the superior electron transport properties in the $In_{0.65}Ga_{0.35}As$ channel and low ohmic contact resistance. A high drain current density of 894 mA/mm was observed at a V_{gs} of 0.6 V.

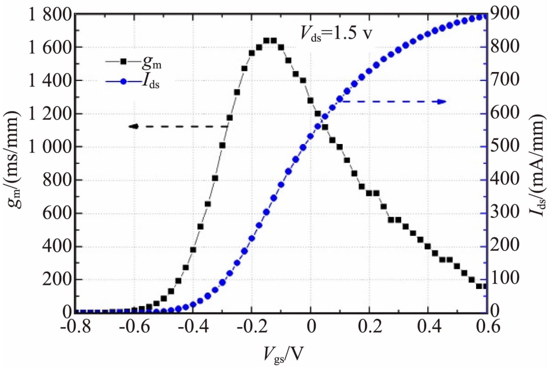

Fig. 5　I_{ds} and g_m versus V_{gs}
图 5　器件源漏电流和有效跨导随栅源电压的变化曲线

As shown in Fig. 6, the off-state breakdown voltage ($BV_{off\text{-}state}$) defined at a gate current of 1 mA/mm is 3.3 V, which benefited from the 200 nm thick Si_3N_4 passivation layer and quantized channel. The gate leakage current was very small, which was crucial for the lower frequency LNA applications since gate current was a contributing component to shot noise[9].

3.2　RF characteristics

The on-wafer RF measurement was performed by using an Anritsu MS4647A series vector network analyzer and an Anritsu 3 743 A frequency extender module (70 KHz ~ 110 GHz) in National Institute of Metrology from 1 to 110 GHz with 0.5 GHz/step. At the meantime, the

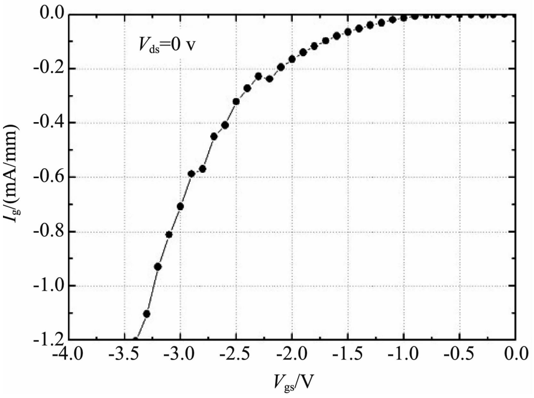

Fig. 6 The gate leakage current of the device
图6 器件的栅极泄漏电流曲线

Cascade probe station Summit 12 K, the CPW I110-A-GSG-100 probe and Impedance standard substrate (ISS) were used as well.

LRM + (Line-Reflect-Reflect-Match) calibration was performed on the ISS to calibrate the system covering the full frequency range from 1 to 110 GHz at a time. The approach relies on three kinds of standards: a Line standard, two reflection standards and a match standard, which are shown in Fig. 7. The LRM + calibration procedure is used to make the measurement reference plane at the tip of the probe, details on the calibration procedure are shown in references[10-11]. The S-parameters after LRM + calibration are shown in Fig. 8, which is shown that the return loss is less than −25 dB up to 110 GHz.

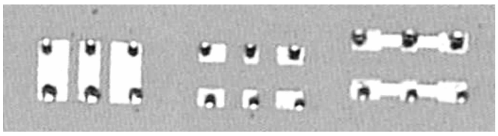

Fig. 7 Line-Reflect-Match standards
图7 直线-反射-匹配标准件

In order to obtain accurate S-parameters of the device, the S-parameters of the pads which were fabricated for on-wafer measurement should be removed. The comparisons of S-parameters before and after de-embedding are shown in Fig. 9.

Compared with traditional measurement in separate frequency bands such as 0 ~ 40 or 50 GHz, 50 ~ 75 GHz, 75 ~ 110 GHz, the continuity of the measured data is much better. As shown in Fig. 10, the H_{21} gain, and MAG/MSG versus the frequency are demonstrated. The current gain H_{21} decreased roughly with a −20 dB/decade slope as the frequency increased, so the f_t = 252 GHz was obtained by extrapolating H_{21} to 0 dB with the same slope.

The maximum power gain MSG and MAG are related to the stability factor k of the device: when $k < 1$, the maximum gain is MSG, which decreased with a slop of −10 dB/decade; when $k > 1$, the maximum gain is MAG, which decreased with a slop of −20 dB/decade.

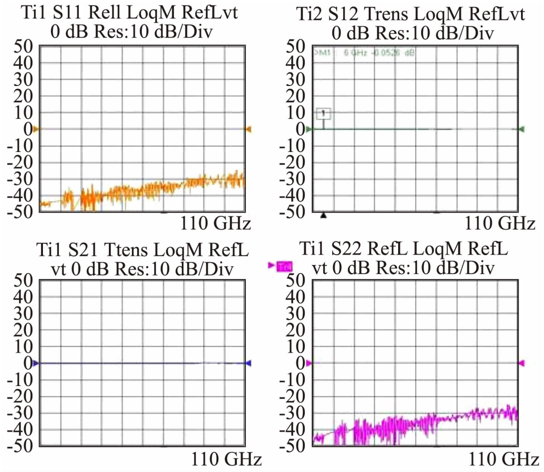

Fig. 8 Result after LRM + calibration from 1 to 110 GHz
图8 LRM + 校准结果(1 ~ 110 GHz)

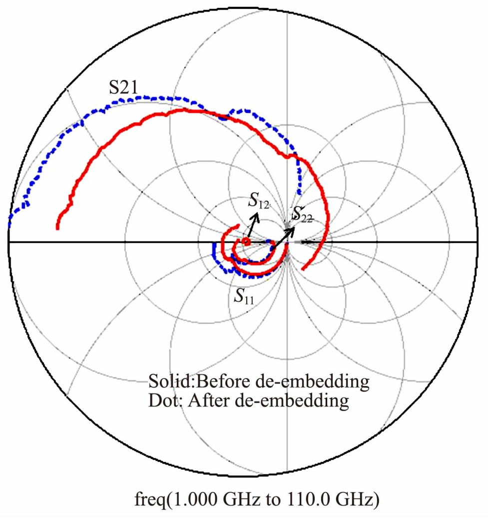

Fig. 9 S-parameters Comparisons
图9 去嵌入前后的 S 参数的史密斯对比图

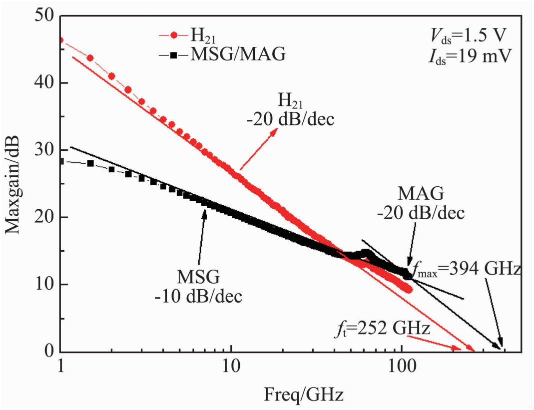

Fig. 10 H_{21} and MAG/MSG versus frequency
图10 H_{21}和 MAG/MSG 随频率的变化曲线

The inflection point ($k = 1$) was measured at 102 GHz, where a maximum gain of 11.8 dB was obtained, so the $f_{max} = 394$ GHz was obtained by extrapolation with a -20 dB/decade slope.

Excellent DC and RF performance are shown in Table 2 comparison with published HEMTs.

Table 2 Comparison with published HEMTs
表 2 与已发表 HEMTs 器件的对比

Reference	L_g /nm	I_{dss} /mA·mm^{-1}	g_m /mS·mm^{-1}	f_T/f_{max} /GHz	Test range /GHz
[12]	150	582	1 052	151/303	0 ~ 40
[13]	150	681	952	164/390	0 ~ 40
[14]	100	850	1 150	180/ -	-
[15]	100	530	700	183/230	-
[16]	100	900	1 200	220/300	1 ~ 110
[17]	88	591	765	150/ 201	0 ~ 40
[18]	70	700	1 600	300/300	-
[16]	50	1 300	1 600	380/380	1 ~ 110
This work	90	894	1 640	252/394	1 ~ 110

Previously, due to the instrumentation limit or the discontinuities caused by measured separately in several different bands from 1 to 110 GHz, such as 0 ~ 40/50 GHz, 50 ~ 75 GHz and 75 ~ 110 GHz, there would be many system errors and the continuity of data is bad. So most of the HEMTs were measured from 0 to 40 GHz, and the characteristics beyond 40 GHz were extrapolated[12-13,17]. However, the inflection point was usually beyond 40 GHz, there would be a bigger error by extrapolation if the inflection point was not measured. So our extrapolated f_{max} based on inflection point is much more accurate than those without inflection point[12-13,16-17].

4 Conclusion

90 nm InP-based PHEMTs with well-balanced cutoff frequency f_t and maximum oscillation frequency f_{max} were reported. Due to the scaling gate size, parasitics reduction and the on-wafer measurement in the full frequency band from 1 to 110 GHz, excellent performance has been achieved, including a maximum saturation current of 894 mA/mm, and a maxmium extrinsic transconductance of 1 640 mS/mm, f_t and f_{max} of 252 GHz and 394 GHz, respectively.

Acknowledgement

This research is supported by the National Natural Science Foundation of China (Grant No. 61275107). The authors would like to thank the members from National Institute of Metrology for their helpful discussions and strong technical support on 1 ~ 110 GHz on-wafer measurement. The authors also would like to express their appreciations to Director He Da-Wei, Engineer Liu Ya-Nan and Du Guang-Wei of Hebei Semiconductor Research Institute for their help.

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