第31卷第6期
2012年12月

红外与毫米波学报
J. Infrared Millim. Waves

Vol. 31, No. 6
December, 2012

文章编号:1001-9014(2012)06-0491-06

DOI:10.3724/SP.J.1010.2012.00491

Design of a D-band balanced frequency doubler with quartz substrate

GUO Jian, XU Zheng-Bin, QIAN Cheng, DOU Wen-Bin

(State Key Laboratory of Millimeter Waves, Southeast University, Nanjing 210096, China)

Abstract: A D-band frequency doubler with quartz substrate is proposed in this paper with commercial planar Schottky diodes DBES105a. The balun in the doubler is implemented by finline-suspended-stripline coupler (FSSC). The waveguide-to-finline transition suit for quartz substrate has only 0.15 dB measured insertion loss. Compared with traditional coupler in balanced doubler and mixer designs, it has the advantage of easier bias for the diodes. Measured results of the doubler showed that the maximum output power is 3.39 mW with 0.4 V reverse bias voltage and 26.3 mW drive power. Its corresponding peak efficiency is 12.9%. The output power of the doubler is reduced from 3.1 mW to 2.0 mW when the bias voltage deviates from its optimum bias condition. The finding shows that proper external DC bias for Schottky varistor multiplier is as important as for schottky varactor diode frequency multiplier.

Key words: D-band; balanced frequency doubler; quartz substrate; finline-suspended-stripline coupler; DC bias

PACS: 85.30.Hi

基于石英基片工艺的D频段平衡式二倍频器设计

郭 健, 许正彬, 钱 澄, 窦文斌

(东南大学 毫米波国家重点实验室,江苏 南京 210096)

摘要:设计了一款D频段基于商用平面肖特基二极管DBES105a以及石英基片的二倍频器.通过对传统的用于平衡式混频器及倍频器的鳍线/悬置微带线巴伦耦合器进行改进,提出了一种方便为肖特基二极管外加偏置的平衡式倍频结构.首先,提出了一种适用于石英基片的波导/鳍线过渡结构,并且通过仿真及实验对该结构进行了验证,测试结果表明,这种过渡结构的损耗只有0.15 dB.在驱动功率为26.3 mW、外加反偏电压为0.4 V时,倍频器的测试最大输出功率为3.39 mW,对应倍频效率为12.9%.在外加偏置电压偏离最佳偏置点时,倍频器的输出功率从3.1mW降低到2.0 mW.这也说明:为了达到最大倍频输出功率,也需要为肖特基变阻二极管倍频器提供外加直流偏置.

关 键 词:D频段;平衡式倍频器;石英基片;鳍线/悬置微带线耦合器;直流偏置

中图分类号:TN771 **文献标识码**:A

Introduction

Used as local oscillator (LO) for the heterodyne receivers in Millimeter-wave and submillimeter-wave systems, solid-state frequency multipliers using planar schottky diodes are becoming more popular, especially in high resolution atmosphere and astronomy fields[1-2]. Performances of these multipliers have been kept improving for the last two decades, with the development of advanced process and design approach. One example is that, the output frequency of the schottky varactor multiplier can reach around 3 THz with 0.1μW output power[3]. It is powerful enough to drive hot electron bolometer (HEB). Other types of frequency sources, such as backward oscillator (BWO) and far-infrared (FIR) laser, will be gradually substituted by Schottky diodes multipliers. This is because of the advantages of Schottky multipliers: more compact, less power consuming, and more reliable. These make them especially suitable for airborne and space application, such as SOFIA[2] and Herschel Observatory[1] and so on.

Received date: 2011-11-16, **revised date**: 2012-07-11 **收稿日期**:2011-11-16, **修回日期**:2012-07-11

Foundation items: Supported by Research Foundation of the General Armament Department of China (51301020603), and Research Foundation of China (9140A01020209JW0601).

Biography: GUO Jian(1982-), male, Nanjing, China, lecturer. Research field is microwave and millimeter-wave circuit and system. E-mail: james@seu.edu.cn.

Generally there are two types of Schottky diodes for the design of frequency multiplier: Schottky varactor and Schottky varistor. Varactors are adopted for high power and high efficiency frequency multipliers, while the varistors could be used for broadband application. Researchers at Jet Propulsion Laboratory (JPL) and Virginia Diode Inc. (VDI) benefited from their extraordinary Schottky varactor diode and multiplier chip process, and outstanding performances have been fulfilled[4-8]. European scientists have designed and fabricated mixers and multipliers with their local diode process for the past few years [9-10], which is the berried-epilayer-Schottky (BES) varistor from UMS, France.

The D-band frequency doubler in this paper adopted the commercial schottky varistor DBES105a. It is also fabricated by UMS BES process. It is widely believed that the DC bias is vital for varactor frequency multipliers to achieve optimum performance, but few of the published varistor multipliers are working under DC bias. In this paper, DC bias for the varistor frequency multipliers has been investigated and the findings are described in later sections of this paper.

The remainder of this paper is organized as follows. Section 1 describes the design of proposed balun coupler. Section 2 illustrates the design of waveguide-to-finline transition. Section 3 focuses on the design of balanced frequency doubler. Section 4 are the measurements and findings. Conclusions are drawn in Section 5.

1 Design of the balun coupler for balanced frequency doubler

Balun coupler is the heart of a balanced frequency doubler, while finline-suspended-stripline coupler (FSSC) is a popular implementation, because of the quasi-planar configuration and the ease of fabrication and mounting. As balanced frequency doubler only produces even harmonics[11], it can simplify the design of the idler circuits. Comparisons between the architecture of balanced frequency doubler using traditional FSSC and the proposed one in this paper are shown in Fig. 1. The traditional frequency doubler with anti-parallel-series diodes is shown in Fig. 1 (a), where the suspended stripline (SSL) operates as the input port and the finline as the output port. The configuration proposed in this paper with anti-series diodes is merely on the contrary, as shown in Fig. 1(b). In both of the configurations, input signals arrive at the two diodes out of phase, while the output second harmonics produced by the diodes are combined in phase. However, the anti-series configuration in Fig. 1(b) is the better choice in terms of getting the two diodes easily biased by an external DC voltage. The cathodes of the two diodes connected to two fins are in the same voltage potential, as they are bonded to the same metal channel. Thus the metal channel provides both DC and RF grounding. The DC bias is fed to the diodes via a hammer-head low-pass filter[12-13] connected to the probe for SSL-to-waveguide transition.

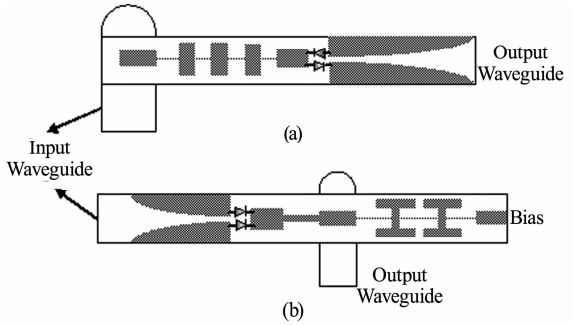

Fig. 1 Architectures for balanced frequency doubler (a) anti-parallel-series diodes, (b) anti-series diodes
图1 平衡式二倍频器结构 (a)二极管反向并串联,(b)二极管反向串联

2 Design of the waveguide-to-finline transition

The waveguide-to-finline transition should provide both RF and DC groundings as mentioned above. Serrated-end finline tapper is usually adopted for waveguide to finline transition, either open-ended or short-ended style[14]. The short-ended one is preferred because the fins are bonded to RF and DC ground. However, experimental results show that the short-ended one has higher insertion loss. That means neither of these two transitions is suitable for this balanced frequency doubler application. The finline transition with vias is also popular for soft substrate. Two rows of vias are arranged on both ends of the finline, which are then bonded to the metal block by conductive epoxy. But this transition still could not be applied on quartz substrate, as the via process on quartz substrate is not available under most situation.

The transition method adopted in this paper is il-

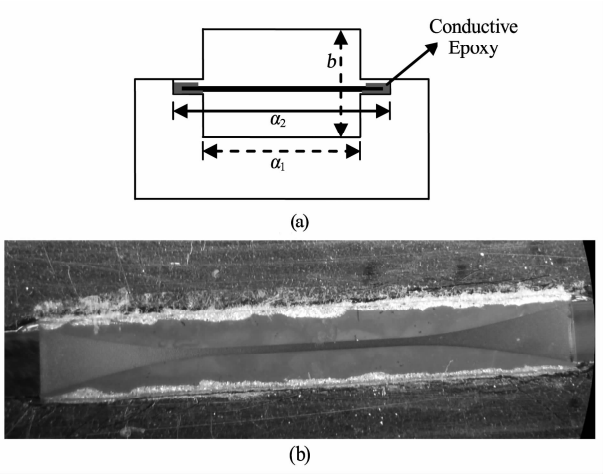

Fig. 2　waveguide-to-Finline transition (a) schematic, (b) photo
图 2　波导 – 鳍线过渡 (a)示意图,(b)照片

lustrated in Fig. 2. The input waveguide was split into two parts: the upper block and lower block. The quartz substrate was bonded on the lower block with conductive epoxy, and the epoxy was further spread to the finline on the upper side of the quartz substrate to provide effective grounding. Most important, the height of grooves on the lower block should be larger than the thickness of the substrate to prevent the substrate from clashing when the two metal blocks are mounted together. Besides, all of the details should be included in the EM simulation. A back-to-back waveguide-to-finline transition was fabricated as in Fig. 2(b). Measured results of the fabricated transition are presented in Fig. 3.

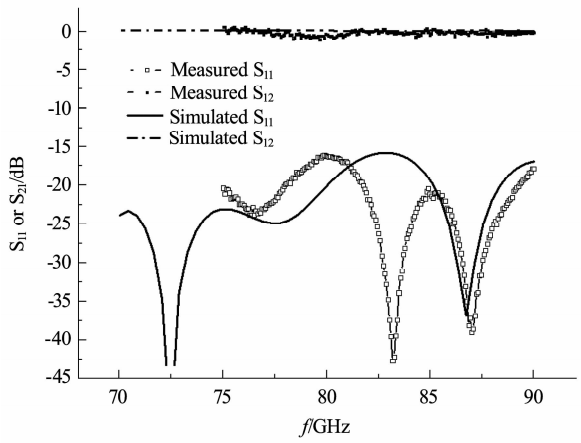

Fig. 3　Performance of waveguide-to-finline transition with quartz substrate
图 3　石英基片波导 – 鳍线过渡性能

The measured two port S-parameters agree well with simulated ones. The return loss (S_{11}) is more than 15 dB from 75 to 90 GHz, and the insertion loss (S_{12}) is less than 0.3 dB (0.15dB for each transition) at 75 GHz, which verifies the validity of the transition method.

3　Design of the balanced frequency doubler

The doubler design begins with the modeling of the diode DBES105a. This diode uses the UMS BES process, so the three-dimentional (3D) architecture is slightly different from the traditional Schottky diodes. The Epilayer of the BES diodes is buried in the buffer layer without air channel in the surface. The 3D modeling of the BES diode in HFSS is similar to the one described by Saini[15] by treating the buffer layer as perfect conductor and adopting a coaxial port at the Schottky contact. The chip DBES105a actually includes two diodes in series. In order to extend the application frequency, the chip was usually cut into two halves to reduce the parametric capacitance and inductance[15-16]. Similar manipulation has been done in this paper by shorting one of the diodes with conductive epoxy.

The key step of the doubler design is to derive the input and output matching impedances. To do this, the models of FSSC and the diode were built in HFSS, which is a 4-port network, including the input finline port, the output SSL port and two coaxial ports each for two diodes. Then, the simulated 4-port S parameters were exported to ADS. The optimum impedances are obtained by the optimization for maximum doubling efficiency. The optimum input impedance is (10 + j5) Ohm and output impedance is (249 + j167) Ohm. Third, the matching circuits were designed in HFSS according to the optimum impedances. The input matching circuit was fulfilled by step impedance finline, while the output matching circuit was realized by step impedance SSL.

Table 1　Dimensions of D-band frequency doubler
表 1　D 频段倍频器的主要尺寸

Parameters	a_r	b_r	w_e	a_j	a_t	gap	w_m
Sizes/mm	2.54	0.75	0.1	1.2	0.4	0.035	0.02

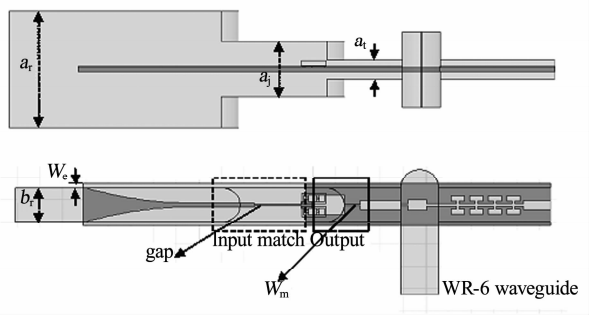

Fig. 4 Model of the D-band frequency doubler (not including the input waveguide-finline transition)
图4 D频段二倍频器模型(输入波导-鳍线过渡不包括在此模型中)

Finally, all the models in HFSS were combined and simulated in HFSS. The structures are shown in Fig. 4. The key parameters of the channel and matching circuits are listed in Table 1.

4 Test of the D-band frequency doubler

The quartz substrate and the module for the D-band doubler were fabricated and tested. The test bench is illustrated in Fig. 5. An E-band MMIC frequency doubler is excited by Agilent signal generator E8257D to dirve the D-band doubler under test. Power meter PM4 with waveguide transition from WR-28 to WR-6 is used to measure the output power of the D-band frequency doubler. The output power of the E-band MMIC frequency doubler is given in Fig. 6.

Measured results of the doubler are illustrated in

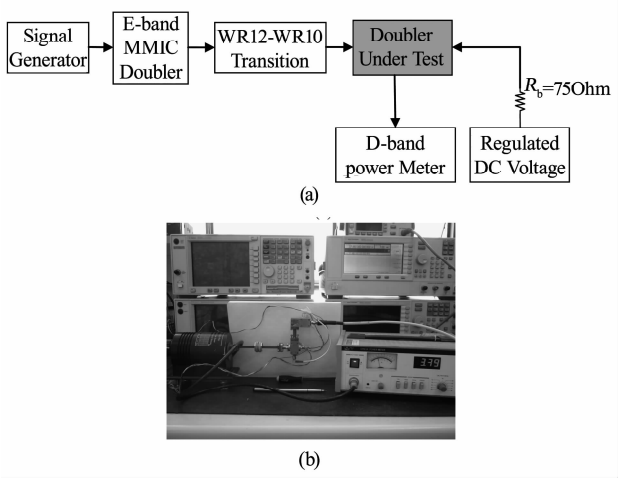

Fig. 5 Measurement set-up of the D-band frequency doubler (a) schematic, (b) photo
图5 D频段二倍频器测试方法(a)示意图,(b)照片

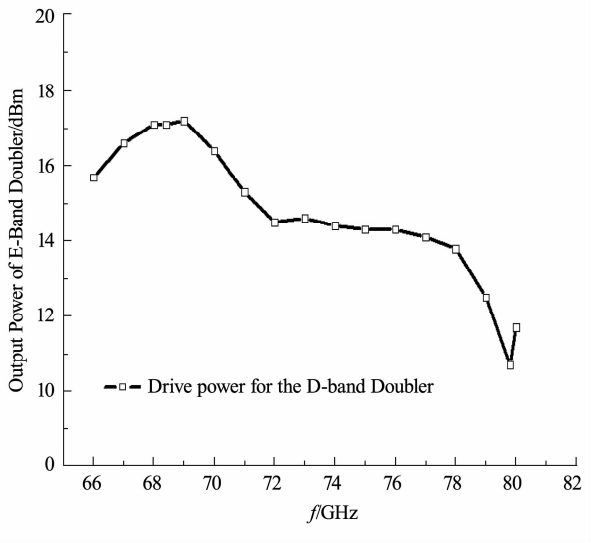

Fig. 6 Drive power of the D-band frequency doubler
图6 D频段二倍频器的驱动功率

Fig. 7. The output power without the input isolator presents more than 12 dB ripple. One main reason is poor output VSWR of the E-band drive douler. And the ripple is obviously reduced after adding an E-band isolator with 75 GHz center frequency and 2 GHz bandwidth, with only 4 dB range now. However the output power is reduced because of the 1 dB insertion loss of the isolator. The maximum output power without the isolator is 3.39 mW when the diodes is reverse biased at 0.4 V with 14.4 dBm drive power,

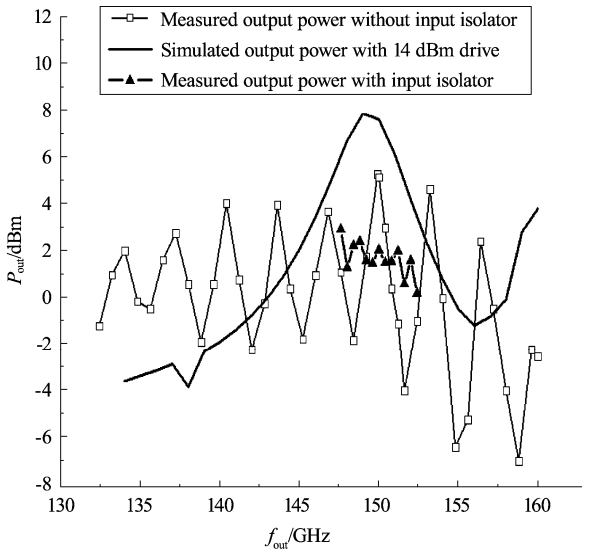

Fig. 7 Measured output power of the D-band frequency doubler
图7 D频段二倍频器输出功率的测试结果

and the peak conversion efficiency is about 12.9% calculated from:

$$\eta = (P_{in}/P_{out}) \times 100\% \quad , \qquad (1)$$

where P_{in} is the input power of the doubler, and P_{out} is the output power of the second harmonic. The output power with the input isolator is 1.05 to 1.97 mW at the frequencies from 147.6 to 152.4 GHz, and the corresponding efficiency is 4.9% to 9.2%.

The measured output power of the doubler at 150 GHz with different diode bias voltages is shown in Fig. 8. The drive power is 26.3 mW. It can be seen that the optimum diode bias voltage is about -0.2 V with 3.1 mW output power. Any bias voltage higher or lower than -0.2 V will decreases the output power, which verifies that the varistor frequency doubler could achieve higher output power with an external bias.

The comparisons between the performance of our doubler and other reported ones are listed in Table 2. It shows that our doubler presents higher output power and conversion efficiency than the ones also designed with DBES105a varistor, but not as good as the varactor frequency doubler both in output power and conversion efficiency.

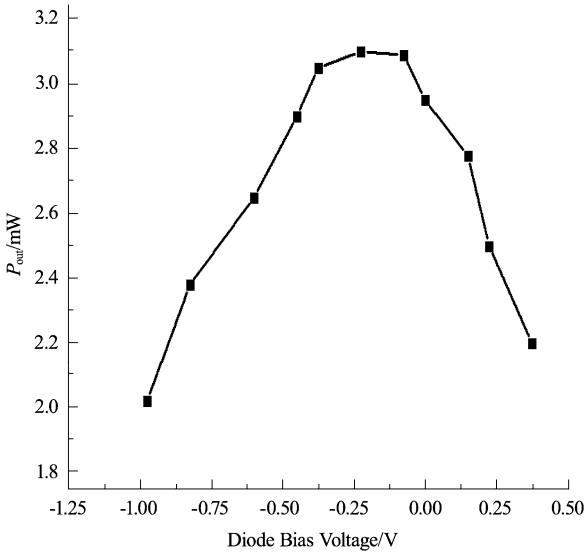

Fig. 8　Ouput power vs. bias voltage of the D-band frequency doubler
图 8　D 频段二倍频器的输出功率与偏置电压的关系

Table 2　Summary of previously reported frequency multipliers and this work
表 2　文中所报道倍频器与已发表倍频器性能的比较

References	[17]	[5]	VDI[18]	VDI[18]	[19]	[20]	[21]	This work	
Harmonics	2	2	2	2	2	3	2	2	
Devices	VDIVaractor	JPLVaractor	Varistor	VDIVaractor	DBES105a Varistor	DBES105a Varistor	DBES105a Varistor	DBES105a Varistor	
f_{out}/GHz	190 ~ 200	185 ~ 195	180 ~ 260	168 ~ 198	180 ~ 190	114 ~ 135	140 ~ 160	133 ~ 160	147.6 ~ 152.4
P_{in}/dBm	19	20			16	19.8	15	14	13.3
P_{out}/dBm	8.5 ~ 9	14.9 ~ 15.3	2 ~ 11	12 ~ 18	−6 ~ −0.8	−10 ~ 5.4	−6 ~ 1.8	−6.4 ~ 5.2	0.2 ~ 2.9
Conversion Efficiency (%)	9 ~ 10	30.6 ~ 33.5	10	>30	0.6 ~ 2.1	3.5	0.5 ~ 3.3	1 ~ 12.9	4.9 ~ 9.2
Year	1999	2004			2010	2010	2010	2011	

5　Conclusions

The design of the D-band frequency doubler with quartz substrate has been introduced in this paper. The structure and assembly of the waveguide-to-finline transition were also introduced. The effectiveness of the transition has been verified by simulation and measurement, with only 0.15 dB insertion loss. Based on the transition, the frequency doubler was built using FSSC. It has the advantages of biasing the diodes easily. Measured results show that the maximum output power is 3.39 mW with 12.9% conversion efficiency. Compared with other reported frequency multipliers also designed with varistors, it shows higher output power and conversion efficiency. That means by finding the optimum bias voltage, the doubler's power performances can be improved correspondingly.

REFERENCES

[1] Goldsmith P F. Spectroscopy with the Herschel Space Observatory[C]. *In* 18*th International Symposium on Space Terahertz Technology*. California. 2007:25 − 31.

[2] Becklin E E, Casey S C, Tielens X. SOFIA: An observatory for THz science and technology[C]. *In* 18*th International Symposium on Space Terahertz Technology*. California. 2007:19 − 24.

[3] Martin S, Nakamura B, Fung A, *et al*. Fabrication of 200 to 2700 GHz multiplier devices using GaAs and metal membranes[C]. *In* 2001 *IEEE MTT-S International Microwave Symposium Digest*. 2001. 3: 1641 − 1644.

[4] Maestrini A, Ward J, Gill J, *et al*. A 1.7-1.9 THz local oscillator source[J]. *IEEE Microwave and Wireless Components Letters*, 2004, **14**(6): 253-255.
[5] Ward J, Schlecht E, Chattopadhyay G, *et al*. Capability of THz sources based on Schottky diode frequency multiplier chains[C]. *In* 2004 *IEEE MTT-S International Microwave Symposium Digest*. 2004. 3: 1587-1590.
[6] Maestrini A, Ward J S, Gill J J, *et al*. A 540-640-GHz high-efficiency four-anode frequency tripler [J]. *IEEE Transactions on Microwave Theory and Techniques*, 2005, **53**(9): 2835-2843.
[7] Porterfield D, Crowe T, Bishop W, *et al*. A high pulsed power frequency doubler to 190 GHz[C]. *In The Joint* 30*th International Conference on Infrared and Millimeter Waves and* 13*th International Conference on Terahertz Electronics*. 2005. 1: 78-79.
[8] Jeffrey L, Hesler W L B, Thomas W. Crowe multiplier development for the upper ALMA local oscillator bands[C]. *In* 17*th International Symposium on Space Terahertz Technology*. Paris. 2006: 215-218.
[9] Siles J V, Maestrini A, Alderman B, *et al*. A single-waveguide in-phase power-combined frequency doubler at 190 GHz[J]. *IEEE Microwave and Wireless Components Letters*, 2011, **21**(6): 332-334.
[10] Wang H, Rollin J-M, Alderman B, *et al*. Design of a low noise integrated sub-harmonic mixer at 183GHz using European Schottky diode technology[C]. *In* 4*th ESA Workshop On Millimetre Wave Technology and Applications*. Finland, 2006.
[11] Faber M T, Chramiec J, Adamski M E. Microwave and millimeterwave diode frequency multipliers[C]. Boston-London: Artech House, 1995: 104-107.
[12] Oswald J E , Siegel P H. The application of the FDTD method to millimeter-wave filter circuits including the design and analysis of a compact coplanar strip filter for THz frequencies [J]. *IEEE MTT-S International Microwave Symposium Digest*. 1994. **1**: 309-312.
[13] McMaster T F, Schneider M V, Snell W W. Millimeter-wave receivers with subharmonic pump[J]. *IEEE Transactions on Microwave Theory and Techniques*, 1976, **24**(12): 948-952.
[14] Kezai T, Sciuto R, Vorst AV. Experimental evidence of mounting grooves and serration patyerns on fin lines characteristics[J]. *International Journal of lnfrared and Millimeter Waves*. 1993, **14**: 1035-1046.
[15] Saini K S. A novel gallium arsenide-quart-based approach towards larger band-width Schottky diode frequency multipliers[D]: [Doctor Thesis]. Virginia: University of Virginia, 2003.
[16] Urzainqui I E. Electromagnetic band gap technology for millimetre wave applications[D]: [Doctor Thesis]. Pamplona: University Publica de Navarra, 2004.
[17] Porterfield D. A 200 GHz broadband, fixed-tuned, planar doubler[C]. *In Proceedings of the Tenth International Symposium on Space Terahertz Technology*. 1999: 463.
[18] [OL]. http://vadiodes.com/
[19] Zhang Y, LinY G. 185GHz solid-state circuits frequency doubler[J]. *Journal of University of Electronic Science and Technology of China*, 2010, **39**(2): 232-235.
[20] Zhang S, Zhang B, Fan Y. Design of a 114GHz-135GHz passive tripler[C]. *In* 2010 *International Symposium on Signals Systems and Electronics* (*ISSSE*). Nanjing. 2010, 1-3.
[21] Yao C. Reaearch on microwave and millimeter wave frequency mixing and multiplying techniques and their applications[D]: [Doctor Thesis]. Nanjing: Southeast University, 2010.

(上接485页)

tum well waveguides [J]. *Applied Physics Letters*, 1987, **50**(5): 273-275.
[2] Lu W, Li L, Zheng H L, *et al*. Development of an infrared detector: Quantum well infrared photodetector[J]. *Science in China Series G: Physics, Mechanics & Astronomy*, 2009, **52**(7): 969-977.
[3] Rogalski A. Quantum well photoconductors in infrared detector technology[J]. *Journal of Applied Physics*, 2003, **93**(8): 4355-4391.
[4] Rogalski A. Material considerations for third generation infrared photon detectors[J]. *Infrared Physics & Technology*, 2007, **50**(2-3): 240-252.
[5] Harrison P. *Quantum wells, wires, and dots: Theoretical and computational physics of semiconductor nanostructure* [M]. Second ed. John Wiley & Sons Hoboken, NJ, 2005.
[6] Jin J P, Lin C. Design of optimized Quantum well infrared photodetector's structure including higher order effects[J]. *Proc. of SPIE*, 2010, 7658: 76581U1-76581U6.
[7] Panda S, Panda B K, Fung S. Effect of conduction band nonparabolicity on the dark current in a quantum well infrared detector[J]. *J. Appl. Phys.* 2007, **101**(4): 043705.
[8] Hirayama Y, Smet J H, Peng L H, *et al*. Feasibility of 1.55 μm intersubband photonic devices using InGaAs/AlAs pseudomorphic quantum well structures[J]. *Japanese J. Applied Phys.*, 1994, **33**: 890-895.
[9] Liu H C. Quantum well infrared photodetectors: The basic design and new research directions[J]. *Chinese Journal Of Semiconductor*, 2001, **22**(5): 529-537.
[10] Schneider H, Liu H C. *Quantum well infrared photodetectors: Physics and applications*[M]. 1 ed. Springer, New York, 2007.
[11] Vurgaftman I, Meyer J R , Ram-Mohan L R. Band parameters for III-V compound semiconductors and their alloys [J]. *J. Appl. Phys.*, 2001, **89**(11): 5815-5875.