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An InGaAs/InP W-band dynamic frequency divider

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Abstract: An ultra-high-speed 2:1 dynamic frequency divider based on clocked-inverter was designed and fabricated using our own f_T = 214 GHz, f_{max} = 193 GHz InGaAs/InP heterojunction bipolar transistor technology. The frequency divider was designed to operate from 60 GHz to 100 GHz. However, it was only demonstrated from 62 GHz to 83 GHz, due to the limitation of the measurement system. The circuit consumed 1060.8 mW with a supply voltage of -5.2 V and 596.4 mW with a reduced supply voltage of -4.2 V. The successful fabrication of the divider was of great importance on building a phase-locked loop operating at W band.

Key words: InP, DHBT; dynamic frequency divider; clocked-inverter

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W 波段 InGaAs/InP 动态二分频器

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摘要: 采用 f_T = 214 GHz, f_{max} = 193 GHz 的 InGaAs/InP 异质结双极型晶体管工艺,设计了一款基于时钟驱动型反相器的动态二分频器. 该分频器工作频段为 60 ~ 100 GHz,但由于测试系统上限频率的限制,只能测出 62 ~ 83 GHz 的工作范围. 在-4.2 V 和-5.2 V 的单电源直流偏置下该分频器的功耗分别为 596.4 mW、1060.8 mW. 此分频器的成功制作对于工作在 W 波段锁相环的构建有较大的意义.

关 键 词: 磷化铟;异质结双极型晶体管;动态分频器;时钟驱动型反相器

中图分类号: TN431.2 **文献标识码**: A

Introduction

Recently, the rapidly increasing demands for millimeter-wave applications, like 60 GHz broadband communication networks, 77 GHz automotive radar systems and 94 GHz millimeter-wave imaging devices, have driven the development of cost effective and high performance millimeter-wave frequency sources such as high frequency phase-locked loop (PLL). The high-speed frequency divider plays a crucial role in implementing high frequency PLL and can be divided into two types, including static ones based on master-slave flip-flop (MS-FF), and dynamic ones. Although the static ones operating up to 200 GHz have been demonstrated[1], the dynamic frequency divider usually has higher speed and provides higher data rates. There are two categories of dynamic frequency divider (DFD), the analog divider and the digital divider. The regenerative frequency divider (RFD) and the injection locked oscillator frequency divider (ILOFD) are well known as analog frequency dividers. The digital clocked-inverted toggle flip-flop

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(CI-TFF) structure, which eliminates the latch from the MS-FF structure, is often preferred and typically shows much higher operation speed than static structures. With an operation speed trade-off, compared with those analog structures, CI-TFF structure can provide broader frequency bandwidth without tuning the bias condition.

Besides structures of the dividers, various device technology used in the high-speed dynamic frequency divider design have experienced a significant development and supported the enhancement of the high-speed frequency divider performance. For example, using InP HBT technology, a 330 GHz frequency divider design has been published[2] and regenerative dividers in SiGe HEMT technology, operating up to 168 GHz have also been reported[3]. These circuits benefit from the enhanced device process as well as the elaborate design of the interconnections.

The design and demonstration of a 40 GHz static frequency divider has been reported in our early paper[4]. It can be used in the design of a PLL in Ka-band. In this paper, we present a 2∶1 dynamic frequency divider in our own InGaAs/InP heterojunction bipolar transistor process. The frequency divider employed clocked-inverted toggle flip-flop (CI-TFF), and was tested to operate from 62 GHz up to 83 GHz (limited by the available Spectrum analyzer). The successful fabrication of the divider was of great importance on building a phase-locked loop (PLL) operating at W band.

1 InP DHBT Technology

In the fabrication of the dynamic frequency divider, the InP HBT technology with emitter width of 1 μm was used. The epitaxial layers consist of a 40 nm carbon-doped base layer and a composite collector. Details concerning the epitaxial layer design and radio frequency (RF) characteristics of the InGaAs/InP HBTs employed in the CI-TFF dynamic dividers can be found in References[5-7].

The HBT IC process included thin-film resistors (50Ω/sq), MIM capacitor, 2-level of interconnect (M1, M2), Benzocyclobutene (BCB) passivation of the devices and planarization of the wafer after device formation. Coplanar waveguide wiring (CPW) was employed for its predictable characteristics, controllable impedance and ability to maintain signal integrity at very high frequencies within dense mixed-signal ICs. S-parameter measurements of the HBT demonstrated an extrapolated current gain cutoff frequency of 214 GHz and an extrapolated maximum oscillation frequency of 193 GHz, at the bias of $Ic = 30.5$ mA and $V_{CE} = 1.5$ V. The circuit operating bias point should be optimized so as for the critical HBTs to achieve the highest f_T value.

The chip microphotograph is shown in Fig. 1. The area of the chip is 924 μm × 717 μm.

Fig. 1 Chip photo of the dynamic frequency divider
图1 动态分频器电路的实物图

2 IC Design

The HBT device model used in our circuit was discussed in detail in References[8,9]. As shown in Fig. 2, the divider architecture consists of a transformer, an input buffer, a frequency divider core, and an output buffer.

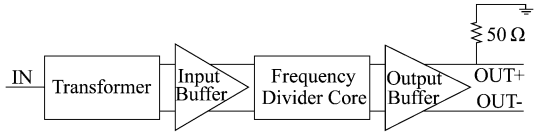


Fig. 2 Block diagram of the dynamic frequency divider
图2 动态分频器的结构框图

2.1 Transformer

When the high frequency divider is employed as a component in a complicated system or instrumentation, a single-ended input requires the least external components and finally reduces overall system cost. Meanwhile, considering the convenience of testing, single-ended input signal is usually preferred. However, the clock signals of the frequency divider core are differential, so the on-chip input network must consequently consist of a transformer converting the single-ended input signal to a differential signal. Due to the finite frequency performance of the device, an active transformer can not bring into high-quality balanced signals of opposite phase in W-band frequencies. For that reason, a passive Marchand balun[10-11] shown in

Fig. 1 was designed and adopted. The length, width and the gap were optimized to obtain promising coupling and finally low transformer loss (S21, S31) through momentum electromagnetic (EM) simulation in Agilent's Advanced Design System (ADS).

2.2 Input buffer

The schematic of the input buffer of the divider is shown in Fig. 3. Three stage differential emitter followers are adopted here. The saturation of the differential pairs of the core part is thus avoided by shifting the input signal levels, before the signals are connected to the input terminals of the clock pair.

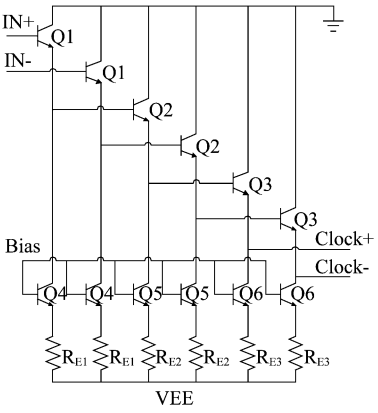


Fig. 3　Input buffer for the frequency divider circuits
图 3　动态分频器的输入驱动

2.3 Dynamic divider core

Adoping the clocked-inverted TFF (CI-TFF) structure, the dynamic frequency divider core is composed of two clocked inverters (Fig. 4).

To operate at high frequency with low power dissipation, the R_{load}, the current and the logic swing C_{cb} $\triangle V_{logic}/I_c$ of the divider should be traded off. The HBTs of the critical part should operate at bias of Ic = 30.5 mA and V_{CE} = 1.5 V so as to achieve the highest f_T value. To reduce the parasitic capacitance and inductance which ultimately slow down the divider, it is critical to construct the divider layout compactly. The frequency divider core was symmetrically laid out and the transistors in the flip-flop were oriented to minimize the critical feedback path of the flip-flop as well as other less critical signal paths.

2.4 Output buffer

The circuit also contains an output buffer (Fig. 5) to drive 50 Ω loads. Q16 serves as a level shifter for the subsequent differential pair. Simulations have shown that a cascade of two emitter followers tends to ring if its input lead length exceeds approximately 200 μm. Therefore, we have used single emitter follower as the output buffer.

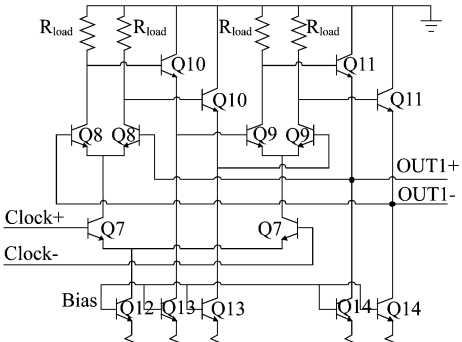


Fig. 4　Schematic of the frequency divider core
图 4　动态分频器核心的原理图

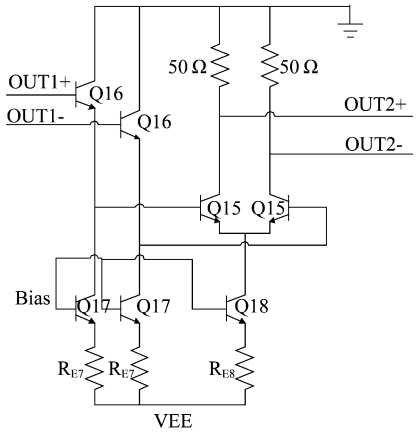
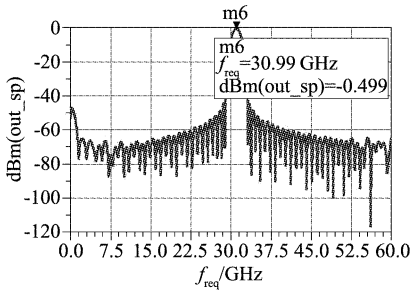
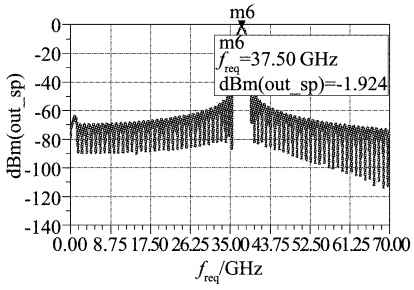


Fig. 5　Output buffer for the frequency divider circuits
图 5　动态分频器输出 buffer

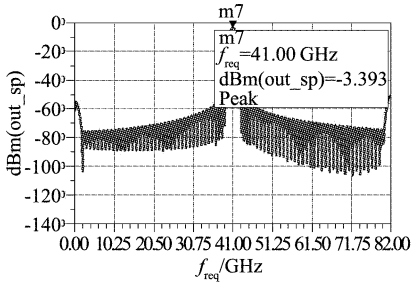
The distribution effects of the passive components were considered by momentum electromagnetic (EM) simulator in Agilent's Advanced Design System (ADS). The output frequency spectrums were shown in Fig. 6. The simulated frequency bandwidth of the CI-TFF was from 60 GHz to 100 GHz. The power consumption was 1005 mW with a single -5 V supply.



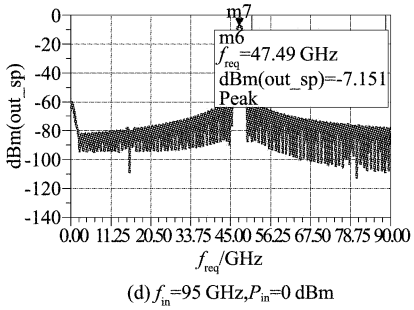
(a) f_{in}=62 GHz, P_{in}=-5 dBm



(b) f_{in}=75 GHz, P_{in}=-5 dBm



(c) f_{in}=82 GHz, P_{in}=-5 dBm



(d) f_{in}=95 GHz, P_{in}=0 dBm

Fig. 6 The simulated output spectrums of the dynamic frequency divider
图6 动态分频器的仿真输出频谱

3 Measurements, results and discussion

The frequency divider was characterized at room temperature of 25 ℃, by the on-wafer test setup shown in Fig. 7. The input signal was generated by a signal generator (E8257D, 250 kHz ~ 40 GHz, PSG analog signal generator) and multiplied by a frequency multiplier (FES-10 Frequency SOURCE 75 ~ 110 GHz, Farran tech) subsequently. The maximum input power of the W-band source can be 5 dBm. The frequency band of the source was decided by the multiplier, which was 75 ~ 110 GHz. The output spectrums of the frequency divider were monitored by spectrum analyzer (E4447A, 3 Hz ~ 42.98 GHz, PSA series). For Fig. 8 (a) the divider was biased at V_{EE} = -4.2 V, I_{EE} = 142 mA, consuming 596.4 mW dc power (P_{dc}) and biased at V_{EE} = -5.2 V, I_{EE} = 204 mA, consuming 1060.8 mW P_{dc} for Fig. 8 (b) (c) (d). The measured operating frequency bandwidth of the CI-TFF was from 62 GHz to at least 83 GHz. We can not measure the IC performance beyond 83 GHz, due to the spectrum analyzer limitation. The divider was not functional at frequencies below 62 GHz. The measured output spectrums were shown in Fig. 8.

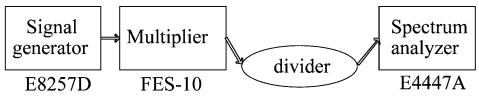
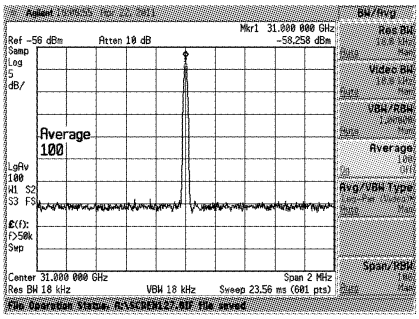
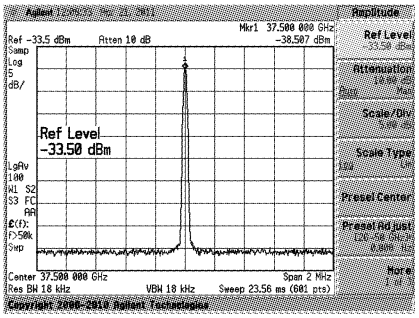


Fig. 7 On-wafer divider test setup
图7 分频器在片测试系统

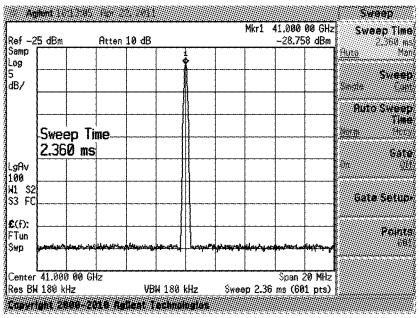
The divider was designed and measured with single-ended output signal, and the complementary output was left unconnected. The input signal power was about -5 dBm. The measurement was performed using the input waveguide and the output coaxial line. The calibration of waveguide and probe was not done in the measurement, which would induce a loss of 5 dB approximately. Specifically, the output spectrum shown in Fig. 8 (a) was obviously lower than others, and the reason was that the divider in Fig. 8 (a) operated at the frequency of 62 GHz which was below the lower frequency limit of the multiplier (75 GHz), thus the multiplier's transmission loss should be very high. In addition, it seems that the output power is lower than that simulated. The first reason may be the uncertainty of the power in our measurement. Another reason may be that all the passive elements and wirings were modeled by 2.5-D electromagnetic simulations of momentum electromagnetic (EM) simulator in Agilent's Advanced Design System (ADS). It was difficult to set the substrate the same as the actual



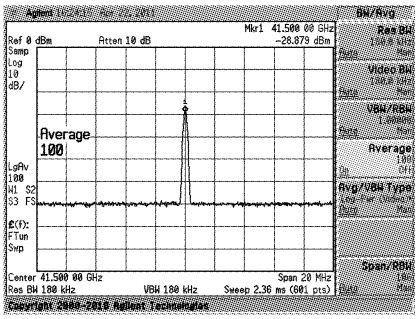
(a) f_{in}=62 GHz,f_{out}=31 GHz



(b) f_{in}=75 GHz,f_{out}=37.5 GHz



(c) f_{in}=82 GHz,f_{out}=41 GHz



(d) f_{in}=83 GHz,f_{out}=41.5 GHz

Fig. 8　The measured output spectrums of the divider
图 8　分频器测试输出

one. This may result in the difference between the simulation and measurement. A further investigation is necessary to identify the specific reason.

To improve the performance and the simulation accuracy of the divider, inverted-microstrip line (IMSL) process could be introduced to provide a ground layer for interconnection, which can increase the precision of the simulation. Meanwhile, more interconnection layers can be used to shorten the critical feedback path of the divider and other signal paths. Finally, in the simulation, more attention must be paid to the impedance matching, such as matching between the input buffer and the balun, to reduce return loss.

Comparing with the dynamic divider reported in the references[12-14], the divider in this work consumes more power. It needs to decrease the emitter area to reduce the power consumption. However, the successful fabrication of the divider is of great importance on building a phase-locked loop (PLL) operating at W band.

4　Conclusions

A W-band ultra high-speed dynamic frequency divider was designed and fabricated in our own HBT technology. The divider IC employed a clocked-inverted configuration with a maximum operating speed of at least 83 GHz. In order to further enhance the operating speed, the reduction of the internal logic swing and the use of clocked-inverted feed forward TFF structure may be effective. To reduce the dc power consumption, it would be helpful to bias the core and the other parts of the divider separately and optimize the size of HBTs in different parts respectively. The measurement results indicated that our InP DHBT technology is promising for W-band IC applications.

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