文章编号:1001-9014(2012)04-0294-05 DOI:10.3724/SP.J.1010.2012.00294

A 75 GHz 13.92 dBm InP DHBT cascode power amplifier

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Abstract: A 75 GHz monolithic-microwave integrated-circuit (MMIC) four- fingers cascode power amplifier in InP double heterojunction bipolar transistors (DHBT) technology with an f_{max} about 150 GHz was reported. The amplifier has $15\times4\ \mu m^2$ total emitter area and exhibits a power gain of 12.3 dB at 75 GHz with 13.92 dBm output saturated power. The amplifier achieves a peak output power of 14.53 dBm with 2 dBm input power at 72.5 GHz. The MMIC adopts coplanar waveguide (CPW) structure as the transmission line structure with area of $1.06\times0.75\ mm^2$.

Key words: InP double heterojunction bipolar transistors (DHBT); monolithic-microwave integrated-circuit (MMIC); millimeter wave; power amplifier
PACS: 84.30.Le

75 GHz 13.92 dBm InP DHBT 共射共基功率放大器

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摘要:报道了基于InP基双异质结双极晶体管(DHBT)工艺的四指共射共基75 GHz微波单片集成(MMIC)功率放大器,器件的最高振荡频率f_{max}为150 GHz. 放大器的输出极发射极面积为15 μm×4 μm. 功率放大器在75 GHz时功率增益为12.3 dB,饱和输出功率为13.92 dBm. 放大器在72.5 GHz处输入为2 dBm时达到最大输出功率14.53 dBm. 整个芯片传输连接采用共面波导结构,芯片面积为1.06 mm×0.75 mm.

关　键　词:InP双异质结双极晶体管(DHBT);微波单片集成;毫米波;功放
中图分类号:TN385, TN952, TN431.1　　**文献标识码**:A

Introduction

High frequency millimeter-wave bands offer exciting opportunities for various applications such as 60 GHz short-range communication[1-2] and 77 GHz emerging automotive radar systems[3-4]. The other E-band communications consists of frequency bands from 71 ~ 76, 81 ~ 86 and 91 ~ 94 GHz [5]. Millimeter-wave power amplifiers are key components for mm-wave wireless data networks. In addition, power amplifier is one of the most challenging components to design due to low power gain at W-band, low breakdown voltages and large loss on-chip passives. All the above impose a strong limit on output power at millimeter-wave bands. Therefore, the accuracy of device process, modeling and circuit design need to be considered carefully. Moreover, the double heterojunction bipolar transistors (DHBT) have the high efficiency and high linearity characteristics relative to high-electron-mobility field-effect-transistors (HEMT).

This paper presents a symbolically nonlinear large signal InP DHBT model in symbolically defined device (SDD)[6] and power amplifier design with coplanar waveguide (CPW) matching technique using 1 μm InGaAs/InP process. The amplifier adopts a four-finger cascode combining structure and open stubs for the matching network. The distributed effects of the passive components, including capacitances, power combiner and transmission lines, were considered by momentum electro- magnetic (EM) simulator in Agilent's advanced design system (ADS).

Received date: 2011-05-13, **revised date**: 2011-12-14　　**收稿日期**:2011-05-13, **修回日期**:2011-12-14
Foundation items: Supported by the National Basic Research Programme of China (2010CB327502).

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1 Device technology and modeling

The structure and material of the device is shown in Fig. 1, which is an InGaAs/InP heterostructure grown by gas source molecular beam epitaxy (GSMBE) on semi-insulating InP substrate[7]. The values of f_t and f_{max} for a single finger HBT device with an emitter size of 1.0 μm × 15 μm are 200 GHz and 150 GHz, respectively.

The improved InP DHBT model has been developed using SDD model in ADS platform[6]. The large signal model is based on charge-control relation and incorporates various physical mechanisms, including self-heating, DC current blocking, velocity modulation, Kirk effect and peripheral parasitic. Fig. 2 shows the equivalent circuit diagram of the large-signal model topology without pad parasitics. The intrinsic model is shown inside the dashed box.

All the DC model parameters, including the thermal resistor, are directly extracted from measured current-voltage (*I-V*) curves and Gummle plots at different temperatures[8]. The parameters of junction capacitances and transit time are extracted from multi-bias S-parameter measurements[9]. The comparison of device *I-V* curves between the measurements and the simulation of the proposed model are illustrated in Fig. 3 (a). It is shown that good agreement between measurement and model data is achieved in I_C-V_{CE} curves. There is a direct relation between nonlinearity and transistor f_t. Therefore, a good fit of the cutoff frequency versus bias voltage and collector current is required in order to achieve accurate distortion simulations. The transistor f_t is shown in Fig. 6 (b) in comparison with SDD model. It is observed that the extracted model closely resembles the measured data.

2 Amplifier design

A single stage four-finger cascode amplifier is designed through power combiner by open stub matching technique. The cascode amplifier architecture could give high gain in a small chip area and high reverse isolation. The schematic of the power amplifier is shown in Fig. 4 and the micrograph in Fig. 5 with size of 1.06 mm × 0.75 mm. The network comprises of CPW matching stubs, quarter-wave transmission lines, metal insulator metal (MIM) capacitances and thin film resistor (TFR). The input is matched for the 50 Ω source impedance using a symmetrical open stub network and the output matching network is designed trade-off between the gain and power. A 200 Ω AC grounded resistor is shunted at the end of the quarter-wave stub on the output port to ensure low frequency stability. In addition, bypass capacitors short-out these quarter-wave line in-band and isolate the rest of the amplifier from the power supply. The Rollett stability factor K for the amplifier was simulated greater than 10 for all frequencies between DC and 110GHz.

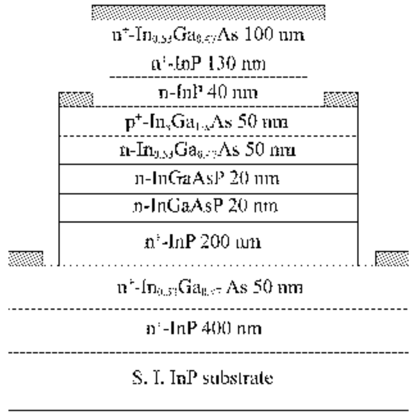

Fig. 1 Structure and material of the HBT
图 1 HBT 材料结构

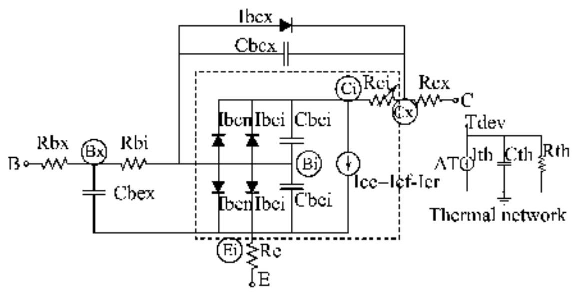

Fig. 2 Large signal equivalent circuit diagram for modeling InP DHBTs
图 2 InP DHBTs 大信号等效电路拓扑

The RF ground connection at the base terminal of the common-base stage of cascode need carefully design due to the parasitic series inductance at millimeter- wave frequencies[10]. The influence of the parasitic inductance is evident on the gain, stability and matching properties of the cascode amplifier. The layout parasitics of cascode power cell is accurately determined by momentum full-wave electromagnetic (EM) analysis using ADS. The size of the bypass capacitances at the base of the common base stage is

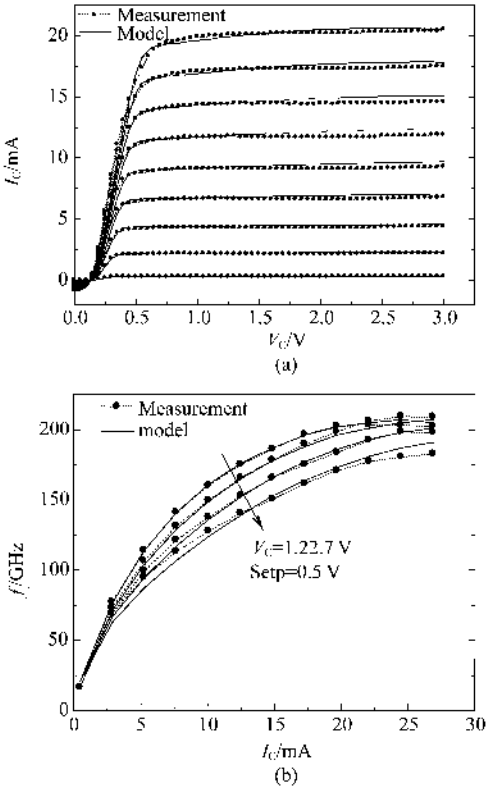

Fig. 3 The simulation results of HBT model in the size of 1 μm × 15 μm, (a) the *I-V* curves, and (b) the f_t versus collector current under different voltage bias
图3 1 μm × 15 μm HBT 模型结果 (a) 直流特性, (b) f_t 与偏置电流曲线

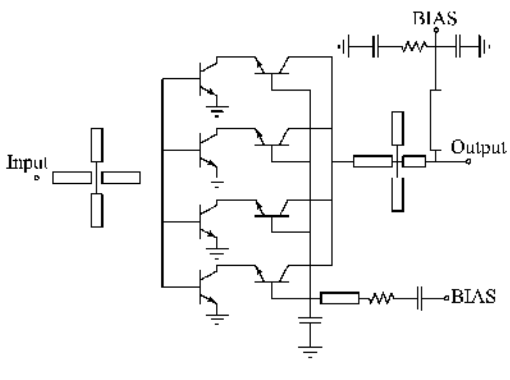

Fig. 4 Schematic of 75GHz cascode power amplifier
图4 75GHz 共射共基功率放大器原理图

75 μm × 75 μm with 2 pF at 75 GHz.

Another important design issue is the thermal stability. The fingers are spaced 16 μm apart to prevent excessive increase in the thermal resistance[11], the self-heating effects, and associated performance degradation.

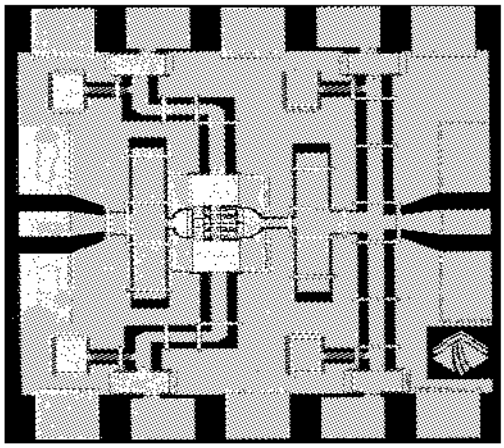

Fig. 5 Die micrograph of the 75GHz power amplifier, chip size: 1.06mm × 0.75mm
图5 75G Hz 芯片照片, 芯片面积为 1.06mm × 0.75mm

3 Measurements and discussion

The small signal characteristics of the amplifier was measured with HP8510C and W-band system made by the 41st Institute of China Electronics Technology Group Corporation on SUSS semi-automatic probe station. The power was measured using Farran Tech frequency doubler source and W-band power meter. Generally the W-band waveguide measurement setup is used for 75 ~ 110 GHz band, but the TE10 mode cutoff frequency for this waveguide is 59 GHz and will not affect the power measurement results between 70 ~ 75 GHz significantly[12].

A full 2-port Thru-Reflect Line (TRL) calibration is performed to define the reference planes to the probe tips before measuring the circuit. The amplifier is designed to operate in class A with bias point of 4.5 V and 60 mA. This corresponds to 15 mA per cascode finger. Measured and simulated *S*-parameters of the amplifier are shown in Fig. 6. It is seen from the small signal measurement results that the center frequency is 75 GHz with 12.3 dB gain. The proposed model agrees qualitatively with the measurement results, except that there are some variations S_{22} and S_{21} due to the thermal coupling among the fingers. In our DHBT model, the thermal coupling is not considered. Although the thermal coupling between fingers is reduced by large finger space of 16 μm, the finger space may also affect the characteristic of DHBT, especially the common-base-stage of the cascode, where the collecter-emitter voltage is high and the thermal effect may be serious.

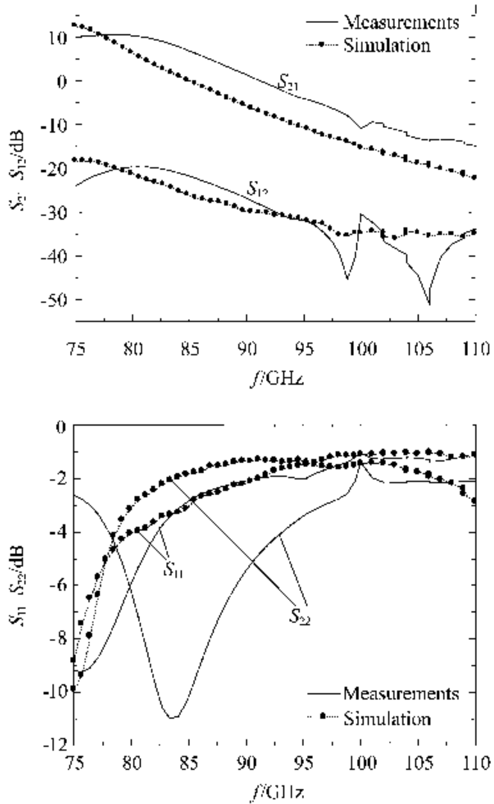

Fig. 6　Measured (dot) and simulated (line) S-parameters
图6　测试(点)与仿真(线)S参数对比

The loss of the connection components including probes and waveguides, need to be considered when measuring the large-signal parameters. The loss could be compensated by calibrating the Thru. The measured output power versus input power of power amplifier at 75 GHz is shown in Fig. 7 (a). The amplifier delivers output $P_{1\,dB}$ 12.2 dBm and saturated output power 13.92 dBm with 9.2 dB gain at room temperature. Fig. 7(b) shows the output power as a function of frequency. The input power of the amplifier is between 2 ~ 4 dBm from 70 to 80 GHz due to the nonlinear frequency doubler. The maximum output power is greater than 10 dBm in the frequency range of 70 ~ 77 GHz. The amplifier achieves a peak output power

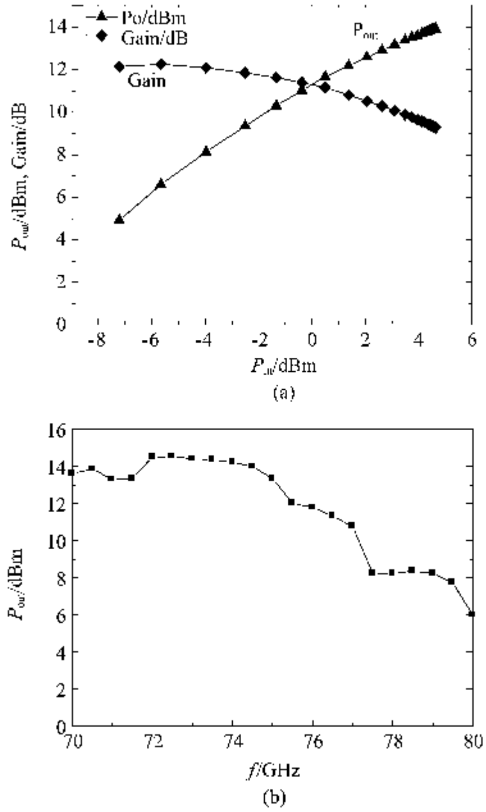

Fig. 7　(a) Measured output power at 75 GHz, and (b) output power from 70 ~ 80 GHz.
图7　(a) 在75 GHz处测试输出功率,(b) 70 ~ 80 GHz输出功率

of 14.53 dBm with 2 dBm input power at 72.5 GHz.

4　Conclusions

We have demonstrated a monolithic W-band four-finger cascode power amplifier based on a 1 μm InP/InGaAs/InP DHBT process. The power amplifier exhibits power gain 12.3 dB at 75 GHz with 13.92 dBm output saturated power. The peak output power achieves 14.53 dBm with 2 dBm input power at 72.5 GHz. The performance of the power amplifier was successfully predicted by our proposed model. Accurate device modeling enables the power amplifier design and predicts accurate performance in simulation.

Acknowledgement

The authors would like to acknowledge the assistance of Li Yankui and Ouyan Sihua for facilitating the measurement.

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(上接第 297 页)

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