

文章编号: 1672-8785(2024)08-0001-12

场效应晶体管太赫兹探测器在太赫兹成像领域的研究进展(下)

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摘 要: 太赫兹 (Terahertz, THz) 波具有能量低、穿透性强、分辨率高等特性, 因而 THz 成像技术在安全检测、医学诊断、无损探伤等领域具有广阔的应用前景。THz 探测器作为 THz 成像系统的重要组成部分, 其性能对成像分辨率、成像速度等有重要影响。由于具备可室温工作、易大面积集成、响应速度快等特性, 场效应晶体管 (Field Effect Transistor, FET) THz 探测器在成像应用中潜力巨大。综述了近年来 FET THz 探测器在 THz 成像领域的研究进展 (包括成像阵列、材料选择等方面), 分析了设计和制造中存在的问题; 指出天线和像素间距是限制大规模阵列化的重要因素, 并在此基础上对未来的研究方向进行了展望; 指出新的材料和结构设计将进一步改善器件性能, 从而实现更快速、更清晰的 THz 成像。

关键词: 太赫兹成像; 场效应晶体管; 太赫兹探测器; HEMT; CMOS; 低维材料

中图分类号: TN386 **文献标志码:** A **DOI:** 10.3969/j.issn.1672-8785.2024.08.001

Research Progress of Field Effect Transistor Terahertz Detector in Terahertz Imaging (II)

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收稿日期: 2024-01-12

基金项目: 国家自然科学基金项目 (61971395; 52075519)

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Abstract: Terahertz (THz) waves have characteristics such as low energy, strong penetration, and high resolution. Therefore, THz imaging technology has broad prospects in areas such as security inspection, medical diagnosis, and non-destructive testing. As an important component of THz imaging systems, the performance of THz detectors has a significant impact on imaging resolution and speed. Field effect transistor (FET) THz detectors, due to their characteristics of room temperature operation, easy large-scale integration, and fast response speed, have enormous potential in imaging applications. This paper reviews the research progress of FET THz detectors in the field of THz imaging in recent years, including advances in imaging arrays, material selection, and analysis of existing design and manufacturing issues. It points out that the antenna and pixel spacing are important factors limiting large-scale arraying. Based on this, it provides an outlook on future research directions, indicating that new materials and structural designs will further improve device performance, achieving faster and clearer THz imaging.

Key words: terahertz imaging; field effect transistor; terahertz detector; HEMT; CMOS; low dimensional material

2 FET THz 探测器的成像

2.2 Si 基 CMOS

十几年来, 基于 Si-CMOS 的 THz 探测器得到了广泛的研究。人们对使用 FET 作为 THz 探测器的真正大规模兴趣始于 2004 年左右^[10]。2004 年, Knap W 等人在 Si-CMOS FET 中首次进行亚太赫兹和太赫兹探测实验演示^[48]。2006 年, Tauk R 等人的研究表明 Si-CMOS FET 可以达到与传统室温 THz 探测器相媲美的 NEP, 响应速度极快^[49], 具有与 CMOS 技术兼容的优势, 可以制造探测阵列。这两项工作展示了 Si MOSFET 用作 THz 探测器的潜力。

2008 年, 第一个单片集成 CMOS THz FPA 被报道^[50]。如图 6(a)所示, 该探测器具有 3×5 像素, 每个像素均包含一个片上天线、一个 NMOS 非相干功率检测电路以及一个 43 dB 放大器, 响应度为 50 kV/W, NEP 为 400 pW/Hz^{1/2}, 性能可与商用高莱探测器相媲美。文献[50]给出了 0.6 THz 下的图像^[51], 如图 6(b)所示。实验证明了 FET THz 成像的可行

性, 并展示了硅集成 THz FPA 在未来低成本 THz 相机系统中的应用潜力。

2009 年, Pfeiffer U R 等人提出了一种用于 0.65 THz 外差成像的低成本 0.25 μm CMOS 工艺 FPA^[16], 如图 7 所示。首次将 0.25 μm CMOS 阵列用于 0.65 THz 单端口器件的平方律混频。 3×5 阵列完全集成在芯片上, 由差分贴片天线、通道金属氧化半导体(N-channel Metal Oxide Semiconductor, NMOS)平方律混频器和 43 dB 低中频放大器组成。

2012 年, Hadi R A 等人提出了一种完全集成在 65 nm 体 CMOS 工艺技术中的用于室温 THz 成像的 1k 像素摄像芯片^[52]。这是 CMOS FPA 首次用于实时捕获透射模式 THz 视频流, 且无需光栅扫描和源调制。该成像传感器将 THz 探测器和读出电路直接在 CMOS 芯片上互联, 因此具有集成度高和一致性好的优点。

2016 年, Knap W 等人通过同时开发晶体管阵列及其 PCB 板上的读出电路^[53]和特殊的衍射 3D 打印光学器件, 展示了 FET THz 探测

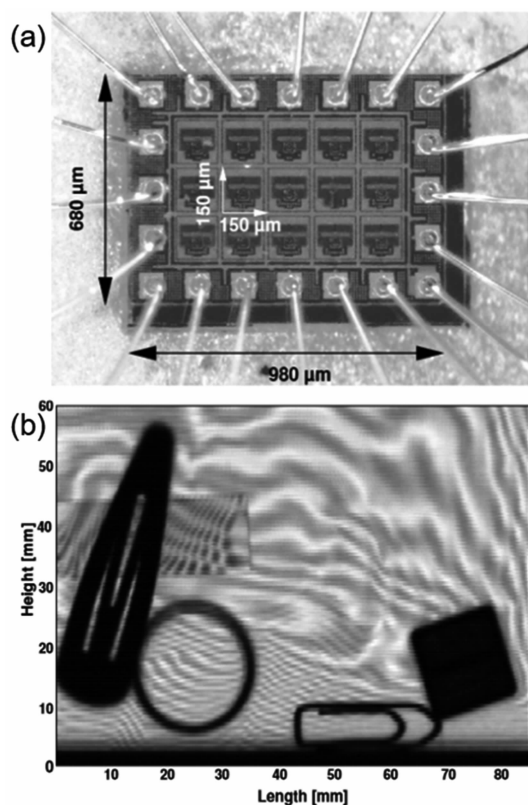


图 6 (a)3×5 像素的 FPA 显微图像; (b)捕获邮政信封的 0.6 THz 图像^[51]

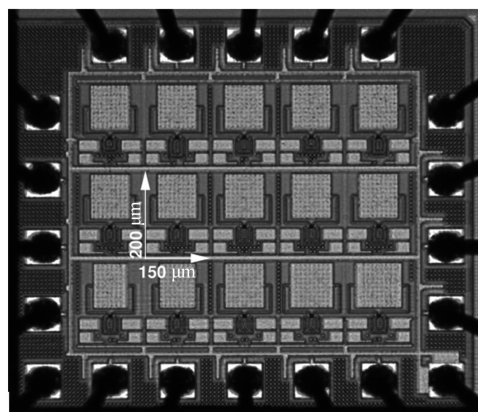


图 7 3×5 CMOS FPA 芯片显微图像^[16]

器的首次实际应用——为快速邮政安全和无损工业质量控制而开发的成像仪(相机和线性扫描仪)^[54-55],如图 8 所示。

由于像素间的串扰以及天线面积的影响,很难实现大规模的 THz 成像阵列。2023 年, Liu M 等人报道了 3~4 THz 波段的 16.4k 像素的 CMOS 图像传感器^[56]。这是首次在 3~4 THz 波段实现如此大规模的成像阵列。结构图如图 9 所示。特殊设计的接地平面上带有周

期性孔的缺陷接地结构(Defected Ground Structure, DGS),可以抑制相邻像素之间的干扰,有助于减小像素间距,提高阵列像素数。而且 DGS 结构还可以释放金属应力并保护大接地层免受潜在故障的影响。完整的像素间距为 60 μm,远小于其他已有报道数据,极大提高了成像的清晰度。

除体硅 CMOS 外,基于绝缘体上硅(Silicon-on-Insulator, SOI)的硅集成 THz FPA 也被报道^[42,57]。Sherry H 等人的研究表明,由于较低的器件寄生效应和高阻衬底,SOI 的效率比体 CMOS 至少高 6 倍,信噪比至少提高了 15 dB^[42]。同时,SOI 技术还可有效减小天线衬底效应的影响。

近几年用于成像领域的 CMOS THz 探测器的详细性能比较见表 3。CMOS 工艺是一种非常成熟的工艺。硅基 CMOS THz 探测器由于与现有 CMOS 技术高度兼容,可以依托 CMOS 工艺而快速发展。其探测电路可以与读出电路轻松集成,方案成熟,易阵列化,集成度高,成本较低,是一种紧凑型成像系统高效且经济的解决方案。但是在 THz 频段,CMOS THz 探测器的硅衬底对耦合 THz 波的高损耗性制约了其发展。从表 3 可以看出,基于 CMOS 的 THz 探测器探测频率偏低,很少有超过 1 THz 的。而且由于硅的迁移率较低,THz 波与等离子体波的相互作用较弱;另外其场效应跨导较小,导致探测器灵敏度相对较低^[28]。同时,由于击穿电压有限,静电放电灵敏度也较高^[40]。未来如何进一步提高硅基 CMOS THz 探测器的灵敏度和带宽是该技术发展的关键。

2.3 新型低维材料

石墨烯由于其高载流子迁移率、无带隙光谱以及与频率无关的吸收,是一种非常具有前途的材料,可用于开发工作在 THz 频段的探测器。人们已经提出了各种新颖的器件结构,例如不对称双光栅栅极 FET^[58],并成功实现了 THz 成像,如图 10 所示。

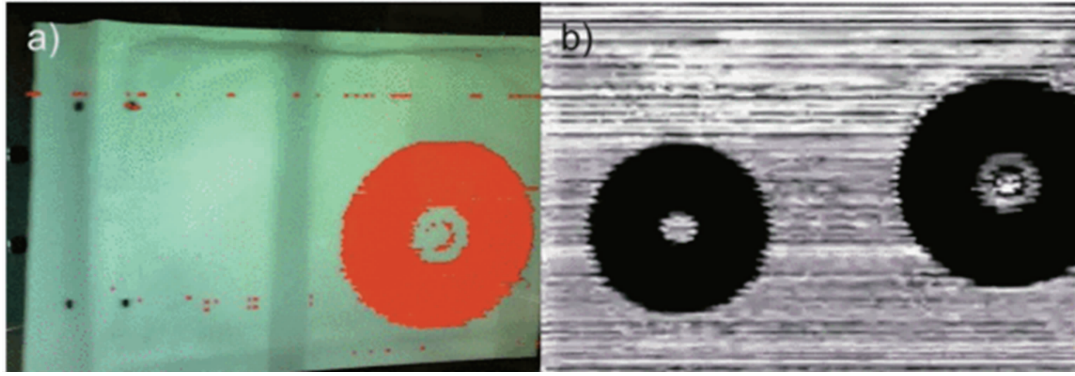


图 8 邮政扫描仪以两种不同的模式对 CD 光盘进行扫描：(a)THz 图像与可见光图像的融合结果；(b)仅 THz 图像^[55]

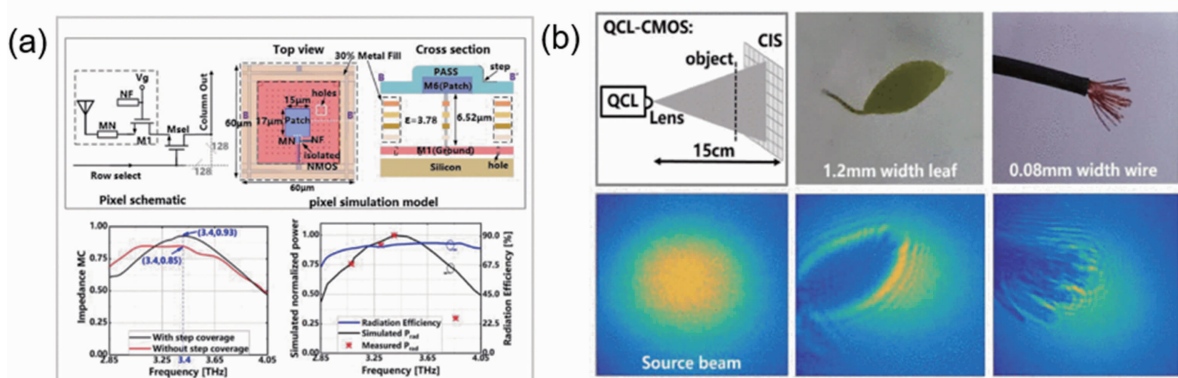


图 9 (a) 3 THz 波段 THz 探测器阵列的原理图、仿真模型和性能图；(b)以 8 fps 拍摄的 THz 图像^[56]

表 3 CMOS THz 探测器的性能比较

年代	器件类型	工作温度	频率	天线	响应度/ ($V \cdot W^{-1}$)	NEP/ ($pW \cdot Hz^{-1/2}$)	像素	有无 透镜	帧率/ fps	引用
2008	250 nm CMOS	室温	600 GHz	折叠偶极子天线	50000	400	3×5	—	扫描	[50]
2009	250 nm CMOS	室温	650 GHz	贴片天线	80000	300	3×5	—	扫描	[41]
2010	65 nm CMOS SOI	室温	650 GHz	折叠偶极子天线	72000	50	3×5	硅透镜	扫描	[57]
2011	65 nm CMOS	室温	600 GHz ~1 THz	折叠偶极子天线	800 @1 THz	66 @1 THz	3×5	硅透镜	扫描	[77]
2011	65 nm CMOS	室温	650 GHz	折叠偶极子天线	245	150	3×5	硅透镜	扫描	[42]
2011	65 nm CMOS SOI	室温	650 GHz	折叠偶极子天线	1930	17	3×5	硅透镜	扫描	[42]
2011	130 nm CMOS	室温	300 GHz ~1 THz	蝶形天线	90000 @300 GHz; 1800 @1.05 THz	—	3×4	—	扫描	[78]

续表 3 CMOS THz 探测器的性能比较

年代	器件类型	工作温度	频率	天线	响应度/ ($\text{V}\cdot\text{W}^{-1}$)	NEP/ ($\text{pW}\cdot\text{Hz}^{-1/2}$)	像素	有无 透镜	帧率/ fps	引用
2012	65 nm CMOS	室温	700 GHz ~1.1 THz	环形 天线	140000 @860 GHz	100 @860 GHz	32×32	硅透镜	500	[52]
2012	150 nm CMOS	室温	590 GHz	贴片 天线	—	43	12×12	—	8	[15]
2013	65 nm CMOS	室温	724 GHz	环形 天线	2200	14	1	硅透镜	—	[79]
2014	90 nm CMOS	室温	0.76~ 4.25 THz	贴片 天线	336 @2.52 THz; 308 @3.11 THz; 230 @4.25 THz	63 @2.52 THz; 85 @3.11 THz; 110 @4.25 THz	1	—	扫描	[80]
2015	150 nm CMOS	室温	600 GHz	贴片 天线	300	43	24×24	—	450	[81]
2016	130 nm CMOS	室温	270~ 600 GHz	蝶形 天线	300000 @270 GHz; 216000 @600 GHz	18.7 @270 GHz; 25.9 @600 GHz	31×31	—	100	[82]
2016	130 nm CMOS	室温	823 GHz	贴片 天线	2560	36.2	8×8	—	1000	[83]
2017	180 nm CMOS	室温	860 GHz	贴片 天线	3300	106	3×5	—	扫描	[84]
2017	65 nm CMOS	室温	3 THz	贴片 天线	526	73	—	—	扫描	[85]
2019	180 nm CMOS	室温	930 GHz	贴片 天线	218000	91@31 Hz	32×32	—	400	[86]
2020	350 nm CMOS	室温	200 GHz	蝶形 天线	19000	535	10×10	—	扫描	[87]
2020	90 nm CMOS	室温	300 GHz	缝隙 天线	55000	20.8	1	硅透镜	扫描	[88]
2021	130 nm CMOS	室温	460~ 750 GHz	矩形线 环天线	171000 @650 GHz	262 @653 GHz	32×32	硅透镜	25	[89]
2021	90 nm CMOS	室温	246.5 GHz	环形 天线	408	21	1	硅透镜	扫描	[90]
2023	180 nm CMOS	室温	3.08~ 3.86 THz	贴片 天线	753 @3.4 THz	203 @3.4 THz	128×128	—	130	[56]

自组装纳米结构技术的发展最近为各种半导体集成器件开辟了道路。基于半导体纳米线的 FET 是一种有前途的高灵敏度室温等离子体波宽带 THz 探测器^[59-60]。它可以在保持良好检测性能的同时缩小器件尺寸, 并提高运行频率^[61]。

具有带隙的层状二维材料最近引发了研究人员越来越多的兴趣。特定的能带结构使这些材料可以用于高效光检测。黑磷(Black Phosphorus, BP)由单层结构磷烯沿 z 轴堆叠而成, 其带隙可以通过改变堆叠在一起的层数来设计和调整。由于能隙介于无间隙石墨烯和较大能

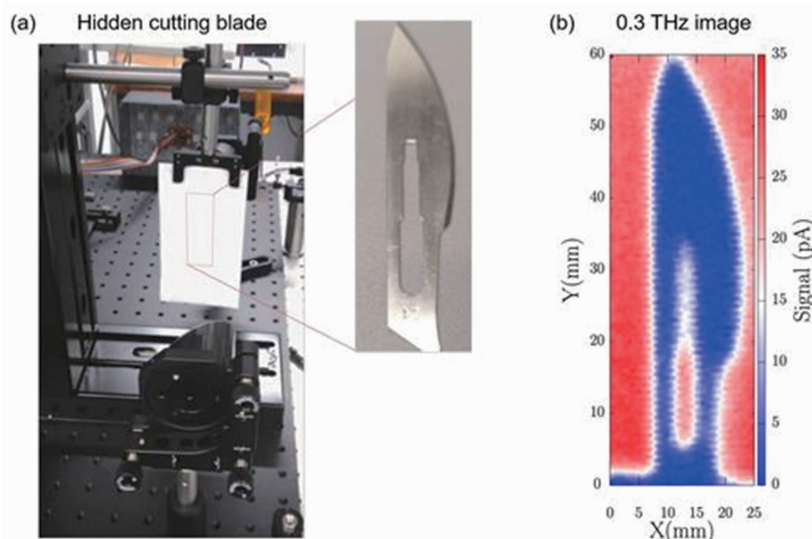


图 10 (a)隐藏在 THz 成像系统封套内的切割刀片的照片；(b)在室温下获得的 0.3 THz 图像^[58]

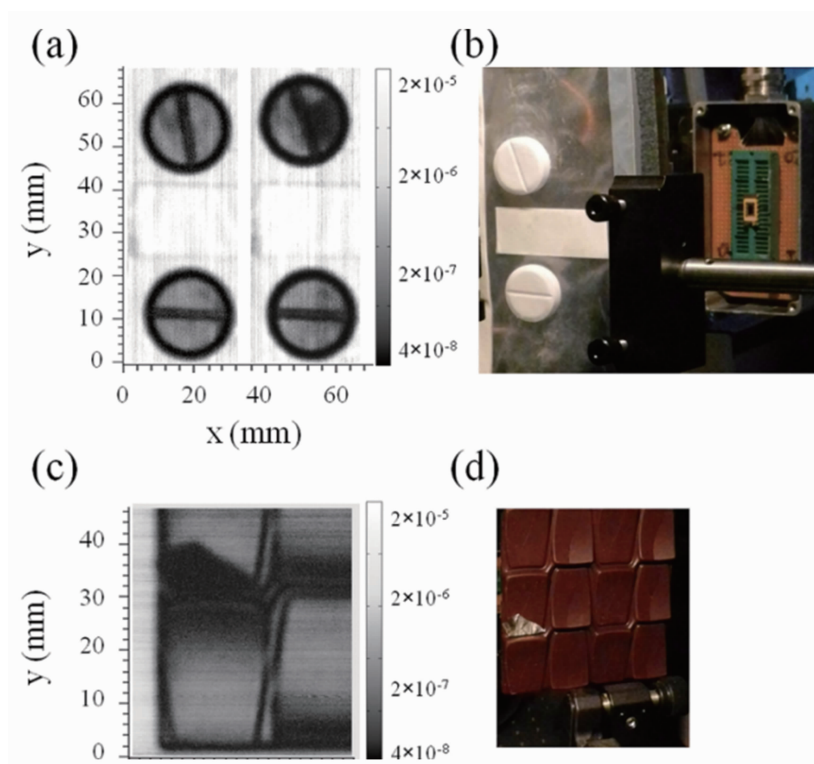


图 11 BP FET THz 成像^[62]

隙过渡金属二硫化物之间，它最近成为一种有前途的多功能光电检测材料。据报道，Viti L 等人已经利用柔性 BP 薄片固有的电/热平面内各向异性，设计了一种具有选择性和可控性等离子体波的 THz 探测器^[62]，并在制药和质量检测领域首次实现成像，如图 11 所示。

近几年用于 THz 成像领域的 THz 探测器

(新型低维材料)的详细性能比较见表 4。尽管这些探测器性能优异，具有很高的研究价值，但其制造困难、工艺不成熟、阵列化困难、运行频率低，短时间内很难转化成大规模的商业化产品。

3 存在的问题

经过十几年的发展，FET 探测器在 THz

表 4 基于新型二维材料的 THz 探测器的性能比较

年代	器件类型	工作温度	频率	天线	响应度/ ($\text{V}\cdot\text{W}^{-1}$)	NEP/ ($\text{pW}\cdot\text{Hz}^{-1/2}$)	像素	有无 透镜	帧率/ fps	引用
2012	SLG-FET, BLG-FET	室温	300 GHz	对数周期 圆齿天线	—	2×10^5 (SLG) 3×10^4 (BLG)	1	—	扫描	[91]
2013	InAs Nanowire-FET	室温	300 GHz	蝶形天线	100	1000	1	—	扫描	[61]
2016	BP-based FET	室温	300 GHz	蝶形天线	7.8	10000	1	—	扫描	[62]
2017	BLG-FET	室温	330 GHz	蝶形天线	30	51	1	—	扫描	[92]
2020	ADGG-GFET	室温	300 GHz	—	$1.96\ \mu\text{A}/\text{W}$	9×10^5	1	—	扫描	[58]

成像领域取得了长足的进步,但其产品性能与理论预期仍有差距,主要存在以下几个问题:

第一,受衬底效应的影响,探测器响应度降低。对于 FET THz 探测器,相当一部分 THz 辐射未被天线耦合,而是会耦合到衬底,极大影响天线的效率,导致探测器性能损失^[59,63-64]。该问题的解决方法之一是减薄衬底厚度。可以预见,在足够薄的衬底中,THz 辐射传播和损耗的影响将会减弱^[64]。但同时减薄衬底厚度又会带来芯片机械稳定性下降以及工艺可行性的新问题。采用 SOI 工艺可以有效减小衬底效应的影响,但成本也会随之上升。另一种方法是采用贴片天线。由于接地层的存在,可以有效消除衬底效应^[65-66]。

第二,天线的设计和制备方法仍有待完善。首先,FET THz 探测器的集成平面天线设计缺少合适的模型指导,并没有真正完善的公式能够直接反映天线尺寸与响应度的关系。天线在 FET THz 探测器中的应用涉及到以下两种理论:第一种是基于电磁场的天线理论,主要用来解释天线如何耦合和发射电磁波,这部分理论比较成熟;第二种是基于 FET 的等离子体波 THz 探测理论。目前依循这两种理论都可以指导天线设计并取得了不错的结果。但是两者如何有效结合,通过揭示天线与晶体管相互作用的底层物理机制来阐释天线设计的基本原则,这部分工作仍有待完善^[67]。其次,图像失真、伪影也与天线有关^[68]。为了消除此类伪影,需要采用新的天线设计来实现栅极下方 THz 场分布的强烈不对称性,同时保持

整个天线的辐射方向图更加对称。

第三,探测器的阵列化也存在许多问题。尽管人们通过不断努力来增大探测器阵列数,以增加一次可成像的像素数来缩短总成像时间,并提高成像的清晰度。但仍达不到其他波段的成像芯片的像素数,例如搭载在移动设备上的 CMOS 成像芯片已有上亿像素^[69]。制约阵列数增大的重要因素包括天线面积和像素间距,以至于每个像元的面积无法缩小。天线作为耦合 THz 波、增大器件响应度的重要部分,需要占据相当大的面积。以蝶形天线为例,天线金属部分面积增大,耦合效率越高,相应的谐振频率也会增大^[32]。缩小天线面积意味着减小谐振频率,而无法缩小天线面积无疑给阵列化带来了难题。像素间距也无法缩小,过小的间距带来大的串扰,影响器件的响应度。DGS 结构可以抑制相邻像素之间的干扰,有助于减小像素间距,增加阵列像素数^[56]。此外,相干探测器由于结构更复杂,阵列化难度也极高。同时,FPA 像素的均匀性也是一个重要问题。受探测器阵列工艺限制,同一芯片上的探测器之间的性能差异较大,令人无法接受^[29,70]。这就需要工艺的进一步优化。随着计算成像技术的发展,通过算法进行优化也是一种可行的方法^[17]。

4 总结与展望

过去二十年来,THz 成像技术取得了重大发展,实现了实时高分辨率 THz 成像技术。该技术正向可大规模生产、成本低、小型化、室温下工作、功耗低、成像速率快、响应度

高、阵列化的方向发展。基于 FET 的 THz 探测器以响应速度快、室温下工作、体积小等优势占据重要地位, 而且与 CMOS 技术兼容, 允许以更低的成本扩展到高分辨率阵列, 因此具有非常大的应用前景。

尽管 FET THz 探测器在 THz 成像领域取得了很大进展, 但其产品性能与理论预期仍存在差距。为实现高速成像而进行的阵列化面临很多困难。天线面积和像素间串扰的影响限制了像元的进一步缩小, 使大规模成像阵列难以实现; 现有的 FET THz 探测器的响应度仍然较低; 衬底效应、天线设计与制备工艺的不完善限制了器件性能的提高。新的 DGS 结构可以抑制相邻像素之间的干扰, 有助于减小像素间距, 增加阵列像素数; 结合机器学习的平面天线设计为天线设计和仿真提供了一种全新的方法; 进一步的物理机制探索和新型低维材料与器件的应用也将为进一步提高 THz 探测器的性能打开大门。

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